

FORMATION AND CHARACTERIZATION OF NITROGEN IMPLANTED SILICON-ON-INSULATOR STRUCTURE*

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Received June 27, 1989

Abstract

Silicon wafer has been implanted with 200 keV $^{14}\text{N}^+$ ions to a dose of $0.75 \times 10^{18}\text{N}^+/\text{cm}^2$ at a temperature of 600°C and has been annealed at 1300°C for 2 hours. During post-annealing rapid redistribution of the implanted nitrogen results in formation of buried polycrystalline nitride layer under the damage-free (except for few dislocations $< 10^5/\text{cm}^2$) single crystal silicon layer, which is characterized by n type conduction. The buried dielectric has a resistivity of approximately $10^8 \Omega\text{cm}$. P channel integrated circuit transistors have been fabricated in the buried nitrid area. The measurements of these transistor devices demonstrate the suitability of nitrogen implanted SOI structure for integrated circuit application.

Introduction

In recent years the fabrication of buried insulating layers in silicon has attracted increasing attention. Silicon-On-Insulator (SOI) structure are currently being evaluated for use in VLSI circuits (Lam, 1982, 1985). Potential advantages of SOI for advanced MOS devices are numerous. These include higher speed, lower dynamic power consumption, greater packing density, increased radiation hardness, a simple fabrication sequence in comparison with the bulk approach and for CMOS a freedom from latch-up (Patridge, 1986). Formation of buried layers by reactive ion (oxygen or nitrogen or both) implantation as the one of most attractive approaches are investigated intensively (Wilson, 1987). In spite of a several advantages of nitrogen implantation over oxygen implantation (50% less total dose required to form a buried insulator, thicker top silicon layer making an epitaxy sequence unnecessary, lower defect density in the top silicon layer, nitride is better barrier against contaminants . . .) there are much more investigations concerning on oxygen implantation (because of the better dielectric feature of the silicon dioxide) than on nitrogen ones (Wilson, 1987). Moreover, the results measured on integrated transistor devices fabricated on nitrogen implanted SOI have been only reported in few papers (Zimmer, 1983, Meyers, 1987).

In this note we report the formation of nitrogen implanted SOI structure consisting of buried layer of silicon nitride and low defect density top silicon

* Dedicated to Prof. J. Giber on the occasion of his 60th birthday.

layer, and the characterization of the parameters of the obtained structure (qualities of silicon single crystal and nitride, the thickness and the resistance of these layers, doping behavior of top silicon) and of the transistors fabricated on these samples (V_T , μ_p . . .), which may strongly influence the integrated circuits process, with different methods (Rutherford Backscattering Spectroscopy (RBS), Ellipsometry, Spreading Resistance . . .).

Experimental

Nitrogen ions ($^{14}\text{N}^+$) were implanted at 200 keV into $\langle 100 \rangle$ *p* type (12 Ωcm) single crystal silicon using the 500 kV ion implanter at the Central Research Institute for Physics, Budapest. To ensure hot implantation conditions a special heater sample holder was designed and manufactured. The substrate temperature was maintained at about 600°C during implantation and was measured by a chromel-alumel thermocouple. The sample was given a dose of $0.75 \times 10^{18} \text{N/cm}^2$ with a current density of 2 $\mu\text{A/cm}^2$ on a $2 \times 2 \text{cm}^2$ area. After implantation thermal annealing was performed at 1300°C for 2 hours in dry Ar. During annealing the sample was covered with an other piece of silicon (face to face arrangement). Both of the as-implanted and the annealed samples were examined by Rutherford Backscattering Spectroscopy (RBS) with 2 MeV $^4\text{He}^+$ ion and by ellipsometry (LEM-2 type) with He-Ne laser source ($\lambda = 632.8 \text{ nm}$) at five different angles of incidence (50, 55, 60, 65, 70°).

For the investigation of doping behavior of the top silicon layer the samples were implanted with doses of $6.25 \times 10^{12} \text{B}^+/\text{cm}^2$ to $3.12 \times 10^{14} \text{B}^+/\text{cm}^2$. After annealing the boron implanted samples at temperatures of 400 to 1000°C for 30 minutes the sheet resistance was measured by four point probe.

$I_D - V_G$ and $g_m - V_G$ characteristics of P channel aluminium gate enhancement mode MOS transistors ($L_p/W_p = 5 \mu\text{m}/25 \mu\text{m}$) fabricated on SOI wafers were measured to compare with transistors on bulk silicon.

Results and discussion

Structural characterization

The previous work (Khanh, 1988) shows that the aligned spectrum of the as-implanted sample can be divided into four regions labeled I—IV in Fig. 1. In region I due to external heating during implantation a partial self-annealing took place leaving a thin surface layer of silicon in form of a good single crystal. Region II still remains a single crystal but heavily damaged owing to the interaction between the ions slowed down and the host atoms.

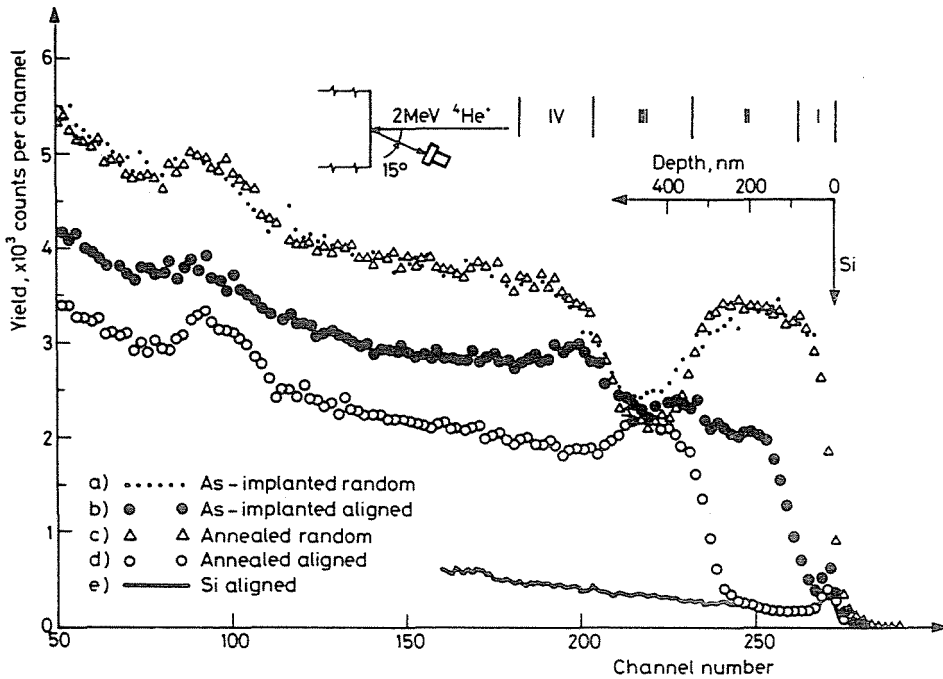


Fig. 1. RBS spectra with 2 MeV ${}^4\text{He}^+$ ions and 165° scattering angle: a) as-implanted random; b) as-implanted aligned; c) annealed random; d) annealed aligned; e) Virgin Si aligned

Next to it there is a nitrogen rich amorphous layer (region III) over the region IV similar to region II, and finally the substrate. After annealing at 1300°C for 2 hours the redistribution of implanted nitrogen has occurred. Both of the interfaces moved toward the nitrogen rich layer increasing the nitrogen concentration in this region to form a well defined nitrid layer with more abrupt interfaces and smoother bottom region (Fig. 1d). Regions II, IV have already disappeared meaning that most of defects created during implantation have been annealed out. The minimum yield of annealed one is 0.06 comparing with that of the perfect single crystal silicon of 0.057. The existence of well achieved top single crystal silicon after annealing is confirmed by the refractive index measured by ellipsometry ($3.89-j0.04$ for SOI and $3.88-j0.02$ for virgin silicon). More detailed information can be obtained from TEM examination (Fried, 1989), where no dislocations or other defects were observed in the top silicon layer even in a large region. The dislocation density is evaluated to be less than $10^5/\text{cm}^2$, which is better than the usual values ($10^7-10^9/\text{cm}^2$). Detailed analysis of cross-sectional specimens using a combination of bright and dark-field images shows that the buried nitride layer consists of several grains of perfect single crystals with grain-boundaries usually coming from surface to surface. Moreover, some silicon precipitates can be found inside

the buried layer near the interfaces as the spectroscopic ellipsometry showed in an earlier work (Fried, 1989). Both of nitride-silicon interfaces are rather rough, with the roughness of 15 nm (lower one) and 25 nm (upper one).

Generally the quality of the top silicon layer and the buried layer seem to depend strongly on the conditions of implantation and annealing process (Hemment, 1984). During high temperature annealing the formation of nitride starts in a nitrogen rich region. The nitride-silicon surface acts as a sink for unbonded nitrogen, that is why the implanted nitrogen moved to the buried layer leaving "free place" for silicon to regrow from the perfect single crystal surface layer (Belz, 1987). However, at the final state of redistribution of nitrogen there are some excess silicon islands captured in nitride because all the nitrogen in this regions went out to the surface surrounding it, and as the diffusion of nitrogen in nitride is very slow the captured silicon has no chance to get further nitrogen for formation of nitride (Chang, 1987). But the redistribution itself usually could only result in a top silicon layer with dislocation density of 10^7 – $10^9/\text{cm}^2$ (Hemment, 1985, Nesbit, 1985, Skorupa, 1986). Here, for our sample the formation of good quality single crystal silicon layer may be explained with the followings: a) Using of an external heating the first state occurring in the case of beam heating implantation can be avoided, when the target temperature is still low so most of the created point defects can not be annealed out but get together to an unannealable defect complex or dislocations (Wilson, 1987); b) Using lower ion flux one can keep the balance between the defect generation and recombination during implantation so the point defect density is not enough to generate dislocations (van Ommen, 1988); c) At the beginning of annealing a slight oxidation could be observed, which may getter the heavy metal contaminants knocked into the silicon during implantation to the thermal oxide so they may not disturb the regrowth of silicon (Wilson, 1987).

The thicknesses of the SOI layers which directly influence the operation of the SOI devices (Lim, 1983, Collinge, 1986) can be determined by SEM,

Table 1
Thicknesses of the SOI layers measured by different methods

Parameter	Measurement method		
	MAIE	RBS	TEM
Thickness of top silicon (nm)	355	350	380
Thickness of buried nitride (nm)	177		180
Complex refractive index of top silicon	3.89-j0.04		
Complex refractive index of nitride	2.03-j0.00		

TEM, RBS . . . but most conveniently by ellipsometry. Multiple-Angle-of-Incidence Ellipsometry can determine the thicknesses fast and non-destructively using a five-phase optical model with abrupt interfaces (air, native oxide, the top single crystal silicon, the buried nitride, and bulk silicon) (Khanh, 1988). The thicknesses of silicon and nitride layers measured by RBS and Ellipsometry are listed in Table 1, which is confirmed with the thicknesses given by TEM (Fried, 1989). We note that the determination of the exact thickness of the nitride layer by RBS is a problem due to the lack of an adequate atomic density value in the literature. There is a reasonable agreement between the thickness data obtained by different methods.

Electrical investigation

The hot probe revealed that in spite of the original *p*-type conduction of silicon wafers used for the experiment both of as-implanted and annealed samples had become *n*-type in top silicon layers. The changing in conduction type probably is caused by the doping effect of nitrogen but not as substitutional but rather as donor complex combination with defects (Stein, 1987).

For determination of the carrier concentration of the top silicon layer spreading resistance measurement was performed with a beveled angle of 0.25° on the annealed sample (Fig. 2). From the spreading resistance measurement the carrier concentration in the top silicon and the resistivity of the buried layer are estimated to be of $10^{14}/\text{cm}^3$ and $10^8 \Omega\text{cm}$, respectively.

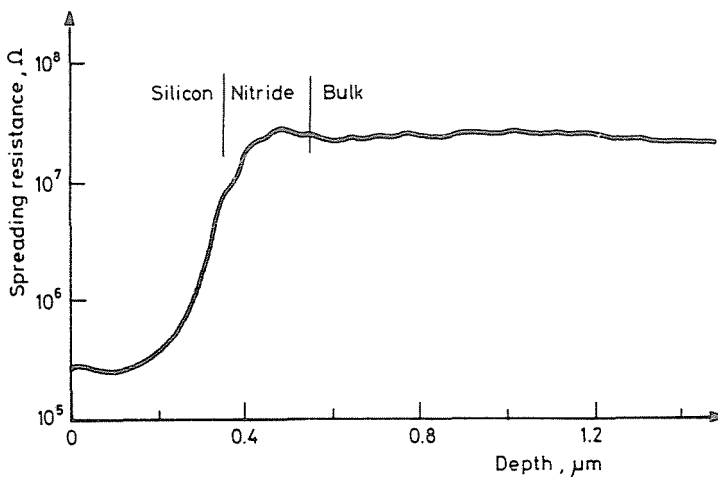


Fig. 2. Spreading resistance measured on the annealed sample. The beveled angle was 0.25°

The cause of low resistivity of nitride buried layer is the leakage current through the nitride grain boundaries (Dong, 1978) which is higher with orders of magnitude than that in single crystal nitride itself. Plus interesting phenomenon can be observed in this figure. After the nitride layer spreading resistance does not decrease to a bulk level. According to Skorupa (Skorupa, 1988) similar things always occur when nitrogen has implanted into *p*-type silicon. Explanation of this phenomenon observed here will require more detailed study.

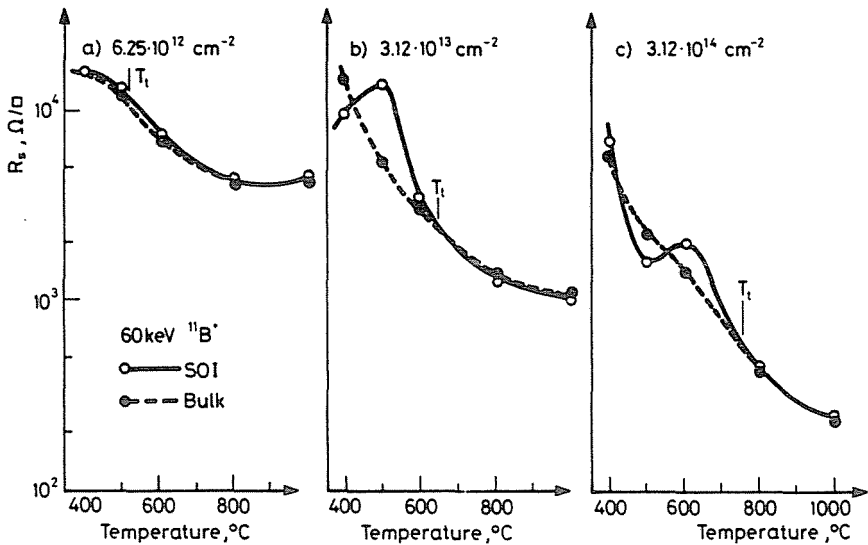


Fig. 3. Sheet resistances measured on the samples implanted with different doses of boron: a) $6.25 \times 10^{12}/\text{cm}^2$; b) $3.12 \times 10^{13}/\text{cm}^2$; c) $3.12 \times 10^{14}/\text{cm}^2$

Since implantation of acceptors into silicon is a very important step in the IC technology we compared the doping behaviour of implanted boron in bulk silicon and our SOI sample. In Fig. 3 the sheet resistivity curves measured on the implanted SOI, and bulk silicon implanted with doses of $6.25 \times 10^{12}\text{B}^+/\text{cm}^2$, $3.12 \times 10^{13}\text{B}^+/\text{cm}^2$, $3.12 \times 10^{14}\text{B}^+/\text{cm}^2$ and annealed at temperatures of 400 to 1000 $^{\circ}\text{C}$ for 1/2 hour in N_2 can be seen. One can observe that due to the higher dislocation density the so called reverse annealing effect is stronger on implanted SOI and the temperature for this effect might decrease if the dose decrease. After annealing at $T > T_i$ there is no difference between implanted SOI and bulk silicon meaning that the top silicon almost as good as bulk silicon except for few dislocations. T_i seems to depend on the dose the sample was implanted. The higher dose is implanted the higher T_i is observed.

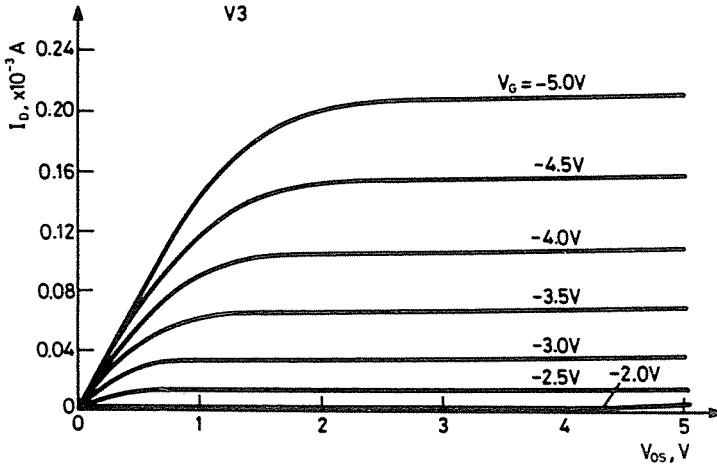


Fig. 4. $I_D - V_D$ characteristics of p channel Al gate enhancement mode SOI transistor

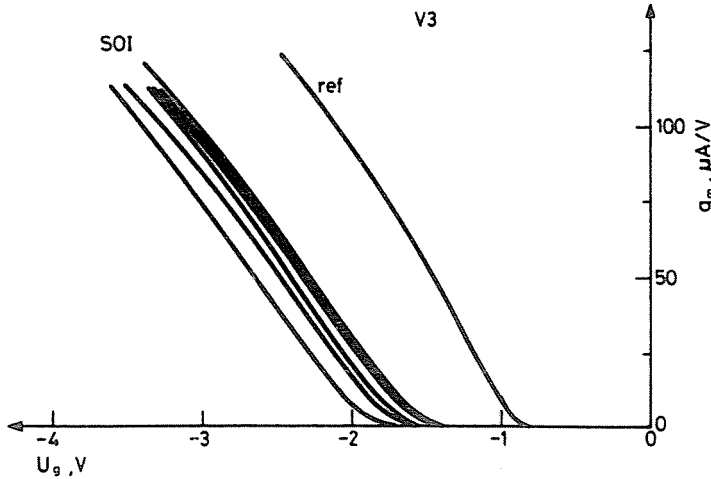


Fig. 5. $g_m - V_G$ characteristics of p channel Al gate enhancement mode SOI transistor

Figures 4 and 5 show the $I_D - V_G$ and $g_m - V_G$ characteristics of SOI MOS transistor. From the later one the threshold voltage (V_{TP}) and the channel mobility (hole mobility, μ_p) can be extracted by the following way (Sze):

$$I_D = A \left[(V_G - V_T)V_D - \frac{V_D^2}{2} \right] \quad \text{where} \quad A = \frac{\mu \cdot \epsilon_0 \cdot \epsilon_{SiO_2} \cdot W}{t_{SiO_2} L^2}$$

$$g_m = \frac{\delta I_D}{\delta V_D} = A(V_G - V_T - V_D)$$

$$(\epsilon_0 \cdot \epsilon_{SiO_2} = 3.4 \times 10^{13} \text{ F/cm})$$

For $V_D=0$

$$g_m(0) = \left. \frac{\delta I_D}{\delta V_D} \right|_{V_D=0} = A(V_G - V_T)$$

From the linear curve of $g_m(0) = f(V_G)$ function one can determine V_T and μ_p .

Table 2

The threshold voltage and the hole mobility of the MOS transistors fabricated on SOI and bulk wafer

	SOI MOS	BULK MOS
$V_{TP}(V)$	-1.7/-2	-1/-0.9
$\mu_p(\text{cm}^2/\text{Vs})$	406	510/550

The threshold voltage and hole mobility of SOI MOS and bulk MOS are listed in Table 2. The contamination and doping problem likely make the threshold voltage of SOI MOS twice of that of bulk MOS. The lower hole channel mobility of SOI MOS probably is caused by the remaining defects in top single crystal silicon layer.

Conclusions

This experiments prove that the nitrogen implanted SOI structures are very promising in IC technology. The electrical characteristics are comparable with the bulk silicon's. In spite of somewhat lower channel mobility SOI structure has many advantages (see Introduction). Moreover, we believe that further optimization can result better performance.

Acknowledgements

We gratefully acknowledge the assistance of Engs. J. Waizinger, C. Seres, F. Gazdaccka (CRIP), J. Gyimesi (Microelectronics Company, Budapest), and Dr. G. Vêgh (Technical University, Budapest).

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