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STUDY OF THE RELATION BETWEEN THE RELIABILITY AND THE NOISE OF DIGITAL SILICON INTEGRATED CIRCUITS

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Abstract

The conventional reliability tests give information about a quantity of the parts. Related to individual devices it means probability characteristics. In many cases – when the failure of the built-in parts can cause a great loss or injury – there is a need to screen out the parts of shorter lifetime of the lot. These ones can show the same perfect quality as the other ones at the beginning of their use. There are screening methods which are usable to find the parts containing hidden failures by some probability level. However, the commonly used screening methods are not without dangers for the faultless parts and their efficiency is limited.

The examination of the noise of the power supply current – as a new method – offers new dimensions to screen out the parts containing hidden failures.

Keywords: reliability screening, noise of power supply current, CMOS digital ICs, lifetime test.

Introduction

The development of the integrated circuit's technology reached great results during the latest decade in respect of the reduction of number of the outgoing defective parts and increase of reliability. The trends of change are shown suggestively on *Figs. 1* and *2*. The data are related to the firm ZILOG, however, they are similar to those of other great firms [1] [2].

The typical industrial levels valid today are as follows: the ratio of the outgoing parts with failure in a lot is less than 100 DPM (DPM = Defects Per Million), the failure rate during time is less than 100 FIT (FIT = Failure In Time, Failures per 10^9 Hours). However, we can find much better values in industry, too, e. g. the ratio of the outgoing parts with failure is less than 4 DPM at Motorola [3].

Nevertheless, the great achievements of the quality control experts led to new applications and possibilities, and to further growth of demands.

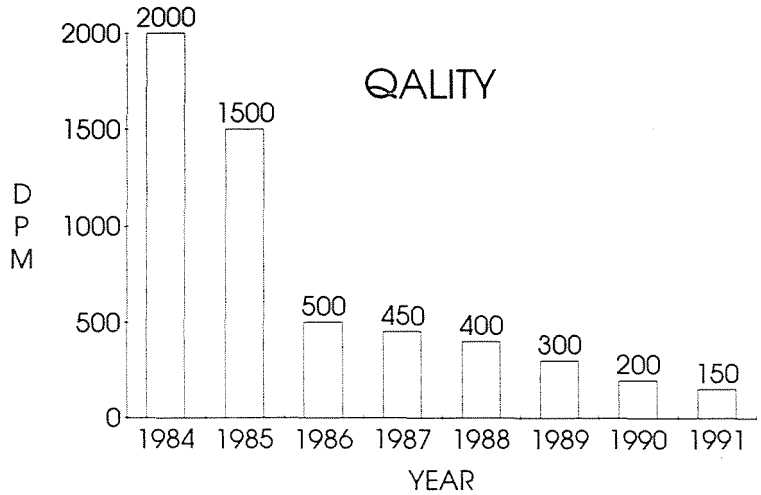


Fig. 1. Changes of the ratio of parts with defects in the outgoing lots at ZILOG Co.

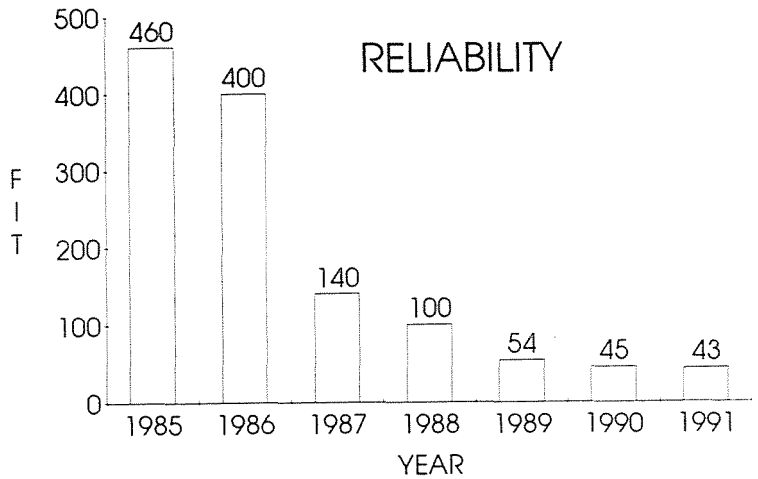


Fig. 2. Changes of the reliability of outgoing parts at ZILOG Co.

The strong competition among the semiconductor firms also drives the experts to continue the research.

There is a possibility to shorten the period of early failures — which is about 100–1000 hours in our case — by some burn-in methods, and after this period we can screen the parts susceptible to early failures. However,

there is no other conventional way by which we could find the devices of shorter lifetime in the lot. The members of the lot seem to be perfect in accordance with the specification and the lot has a nearly constant failure rate level in time at that moment.

However, there are some applications in which the failure of the device can cause very great financial or moral damage. E. g. we faced the problem originally at VEGA and PHOBOS space research projects when we had to screen out the devices of best and worst reliability of military-grade lots of numerous types.

The task is analogous in military applications, in industrial security systems, or in medical life-support equipment, etc. In these or similar cases it is rather harmful if the failure of one part causes damage of an important and/or precious system and, at the same time, the other — possibly some million — devices are working properly.

In other cases there is a demand for parts of increased reliability in the so-called commercial applications where high volumes of parts are used and the unit cost is an important aspect. A market segment exhibiting this cost vs. reliability concern most informatively is the automotive industry where one IC type can be used in some million pieces and the reliability requirements are very high considering the recent warranty and environmental conditions [4].

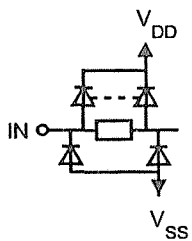
As a result there is a need for methods by which the devices of shorter lifetime can be screened out of the lot in the period of random failures. Unfortunately, the commonly used methods give only a partial solution.

Power Supply Current as a Carrier of Information

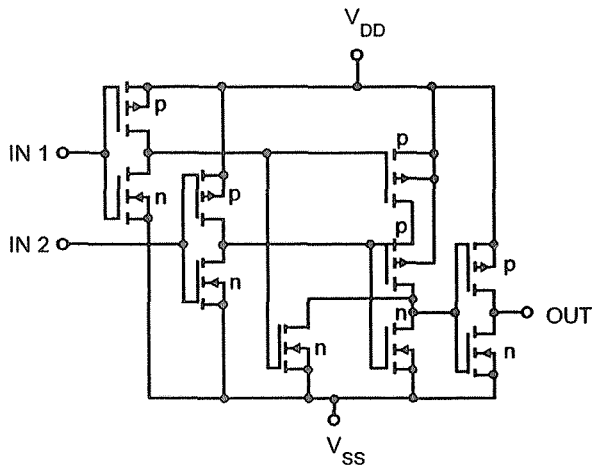
There is another form of the latter question: Is there any method by which we can examine a complete ready-made integrated circuit as a physical structure without destruction or acceleration of failure mechanisms which can cause defects later? By this method we should be able to uncover the hidden failures or the not quite perfect elements far from the input/output connections.

The answer and the train of ideas following it are simple from this phase if we have a look at the circuit schema of any digital IC; as an example a CMOS 2 input NAND gate is shown in *Fig. 3.*

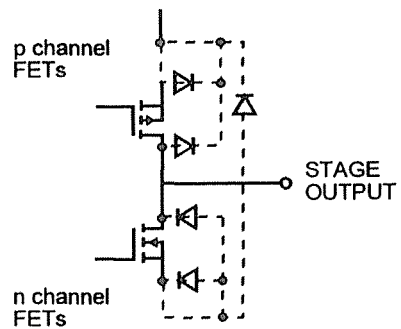
There are connections which are commonly very close to and are never too far from each element inside — the power supply connections. Under normal conditions the supply voltage is constant so the power supply current is carrying detailed and thorough information about the physical state of the system. However, the physical system inside depends on the exist-



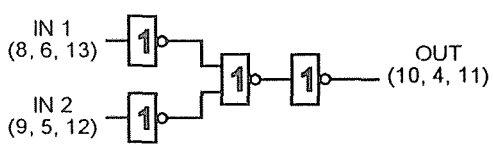
INPUT PROTECTION FOR EACH INPUT



FUNCTIONAL CIRCUIT



PARASITIC DIODES FOR EACH STAGE



LOGIC DIAGRAM

Fig. 3.

ing physical structure and, on the other hand, on the actual input signals, in the case of sequential networks, on the previous input signals, too, on the output loads, and the environmental conditions.

There is an old observation in nature: devices of a noise level above the average go wrong sooner, and before catastrophic failure, devices become more noisy in many cases [5]. In the case of digital integrated circuits the power supply current contains the signal of each element as a noise source inside. (It is obvious for CMOS ICs.)

So, the noise analysis of the power supply current allows to discover the devices of shorter lifetime.

Anyway, there are several other ways to examine an IC as a system; e.g. we can test the highest clock frequency at which the device can work properly, or measure the lowest level of supply voltage at which the device can operate. In the frame of this study we do not deal with these methods because they demand special and different considerations. However, they seem to be interesting for the research to be carried later.

Some Possibilities to Study the Supply Current as an Information Carrier

By the former idea the examination of the power supply current, or the noise content of the current gives a possibility to screen out the devices of short lifetime. However, there can be many ways and terms to study the current noise. In some cases the quantities measured are not real noises but they are similar to noise, mathematically they are random variables.

Let us see the main possibilities to study the supply current, their benefits and problems, and then specially considering the CMOS circuits used in our first experiments.

Static Current Test

The static supply current test measures the static supply current of the whole circuit with the device under unexercised, static conditions.

The big differences between the actual static current in various states following each other and the corresponding typical current reflect significant differences in the physical structure. The device showing such an effect is doubtful.

The question is how to determine the set of static test states and how to set the circuits to the states in order to find all possible defects which may cause excess current in a practical circuit?

To perform the measurement we need a current meter of high resolution. The measurement of static supply current can be a usual part of the conventional quality control.

Static Current Noise Test

The measurement is similar to the former one in some respects, however, now we should measure the noise content of the static current at the different predetermined states. The problem to determine the adequate test vectors and states is the same, too.

In principle, the test really based on the direct evidence that with increasing noise any device becomes of lower quality, damaged or less homogeneous. So, the devices having higher supply current noise than typical are doubtful. Nevertheless, the noise increase is very small in some cases, so it is not easy to detect it safely.

To perform the measurement we need a low-frequency noise spectrum analyser, which measures the noise current level versus frequency related to unit bandwidth in the low frequency range. This measurement is very time-consuming.

Transient Current Test

When a circuit is induced to change the state of the set of the internal gates, a consequent current pulse is produced, which shortly can be called transient current. Performing the transient current test, first we must determine the adequate set of test vectors.

The test vectors following each other given to the inputs force the device to execute state changes. In the course of the state changes a signal flow is running through the device which causes some well-observable current transients.

By measuring a lot of devices we can determine the average of the transient flow. The transients which are different in some aspects from the average indicate a doubtful device.

We can perform the measurement by a fast DSO (Digital Storage Oscilloscope). The sensitivity of the measurement depends on the resolution of the DSO. (The resolution is 8 bit in many cases, high quality DSOs have 10 bit or 12 bit resolution.)

Repeated Transient Current Test

The method is similar to the former one, but we get the reference transient current function from the former repeated transients of the same circuit. Later we compare every new transient to the average of the former transients. We get a series of differences with noise characteristics. The big differences and fluctuations indicate an unstable structure, in this case the device is doubtful.

To execute the measurement we need a DSO with good resolution.

Naturally, we must ask the question: Which method is the most advantageous in order to reach our goal?

The question is complex, and we can find the answer according to the next viewpoints:

- we can test the devices by the given method (circuit family, function, complexity, level of integration);
- detectable physical failures in accordance with the examinable circuit details;
- sensibility to the failures;
- problems of implementation in practice;
- measurement time/speed;
- cost of the measurement.

So, the answer is complex, too, we need some more studies to show each detail. However, we can summarise the main considerations.

Each method shown former is suitable to test all the different families of digital integrated circuits, but the practical problems and tasks to execute the measurement series and to evaluate the direct results are very different. The methods are usable for VLSI ICs, too, but we state again that it is a serious task to determine the suitable test vectors in order to get reliable results.

We must set up the failure models to determine the detectable defects and the sensibility of detection.

For practical applications there are some important viewpoints: the measurement series should be fast and of low cost level.

As a result, the noise measurements are not favourable.

Special Considerations Related to CMOS ICs

The CMOS technology, the CMOS logical families are in front of development nowadays. The presence of the low voltage logical families promises CMOS ICs a long cycle. The CMOS structure is relative simple and easy

to consider. Beginning the experiments with CMOS devices seems to be advantageous.

In the CMOS circuits the functional and the additional and parasitic elements are well separated. They have a special characteristic: the supply current — which has such a great importance for us — has very different levels in static and dynamic states.

If there is a serious failure in the device, then it is detectable by each method.

The Static Current Test shows a relative low sensibility to the hidden defects of the functional parts. In CMOS ICs the main part of the static current comes from the additional and parasitic elements in accordance with their relative large area on the chip while the functional parts have a smaller effect on it. Certainly, the share of the functional parts in the current contains information about them according to the input test vectors. The great differences related to the average level in some states show big differences in the physical structure, so the device is doubtful. However, for CMOS there can be relative high deviations in perfect devices, too. The temperature dependence of the current is also high.

The current to be measured is very small, it is of 10^{-10} A. *Fig. 4* shows the static current of a CMOS dual D flip-flop as an example.

Probably the static current noise test gives the most comprehensive information about the device. The statement that the failures causing problems later in CMOS devices bring on a growth of the noise seems to be true and this noise is well detectable. Some measurements verify the statement even if the original typical noise levels of the different elements — n and p channel FETs, several pn junctions, etc. — are not the same [6].

Execution of the measurement in practice is not an easy task because of the low level of the noise and the high value of the source impedance together with the high value of the transient currents during the state change. It needs a relative long time. The typical noise level to be measured is in the range of 10^{-29} A^2/Hz.

The transient current test seems to be especially sensitive to the failures of the functional elements. Studying the problem thoroughly, we can see that the measurement gives information about the other elements. During the switching these elements play smaller or bigger role in the supply current [7].

The peak level of the transient current is some mA.

The repeated transient current test is in practice similar to the transient current test. The resolution of the DSO is important, and usually we need a computer controlled measurement system to store and evaluate the results.

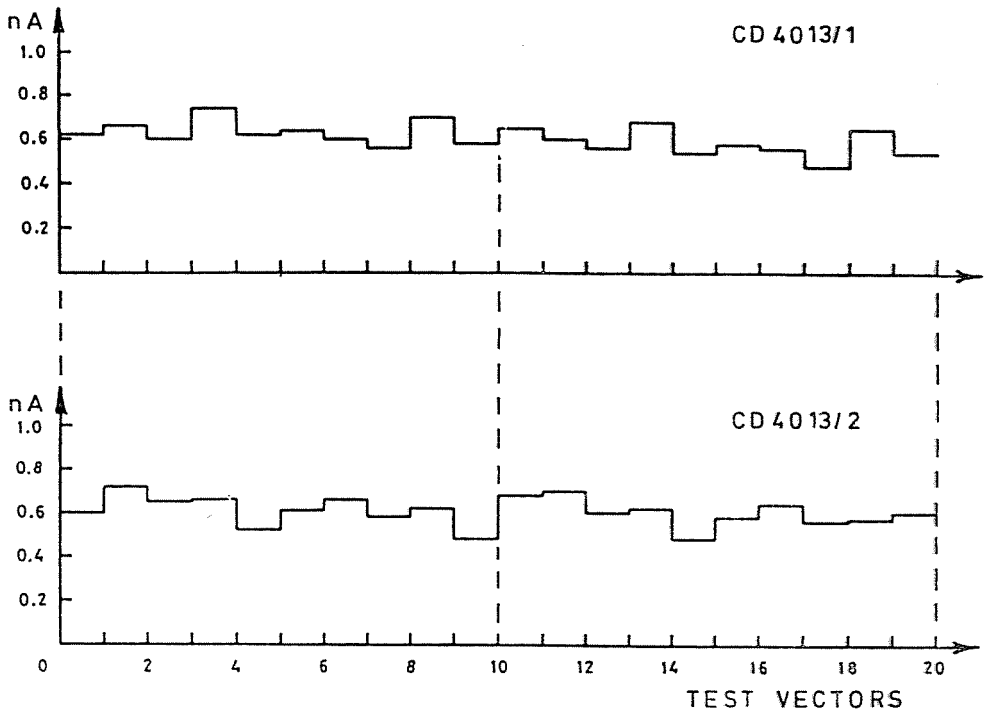


Fig. 4. Static current as a function of states in the case of a CMOS dual D flip-flop

Evaluating the methods we can state that the last two tests seem to be practical under industrial conditions for high volume automated measurements.

Experiments to Justify the Theory

We should not forget that the ideas written above form a test hypothesis so we must justify it as a whole and in detail, and work out its particulars. The results of the first experiments can support and direct our work.

Based on theoretical and practical considerations we set and executed the next steps:

1. We began our experiments with metal-gate CMOS ICs. This family is not out-dated yet, but it is the base of the later fast versions, and its speed is measurable with our equipment.

We performed the transient current test first, which was a relative simple task, and it could display many failures.

2. We set up a measuring system shown in *Fig. 5.*

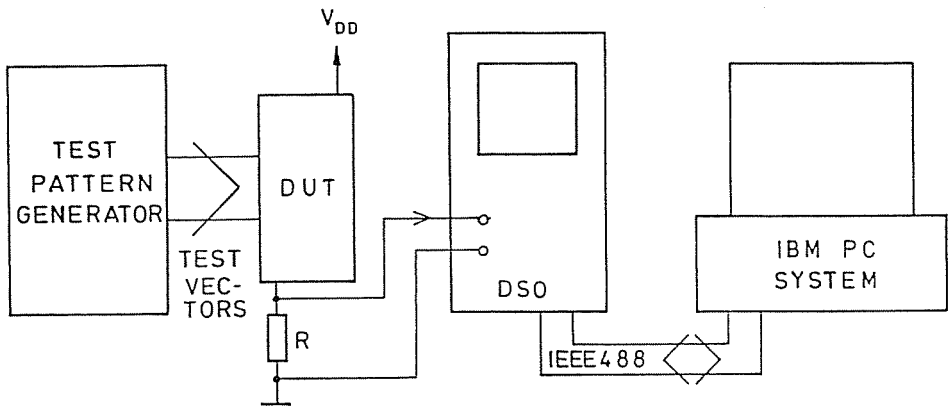


Fig. 5. Measuring system for Transient Current Test

In the course of the measurement the crystal controlled test pattern generator gives a series of test vectors to the input of the DUT (Device Under Test) and synchronises the DSO. The DSO (HITACHI Type VC 6065 in our case) measures the current on a watching resistor of 50 Ohm.

We receive the digitised results of the measurement through IEEE 488 bus by an IBM PC storing and evaluating them.

3. We have got the first results by measuring 2 input NAND gates. The results of the measurements are very interesting in the case of the same types of different manufacturers. There is an excellent possibility to observe the differences between structure of circuits or technology, despite of the similar data sheets.

The transient current of a NAND gate type MC 4011 BE is shown in *Fig. 6.*

For checking our hypothesis we have found practical to choose a not too complicated sequential circuit of a number of equivalent gates. We chose a dual JK flip-flop type HCF 4027 of SGS-Thomson (equivalent to RCA CD 4027). We examined a lot of 1000 pieces. The circuit schematic of the device is shown in *Fig. 7.*

4. We worked out the suitable series of test vectors for the given JK flip-flop. We made INTERBIP INVEST execute the full functional, static,

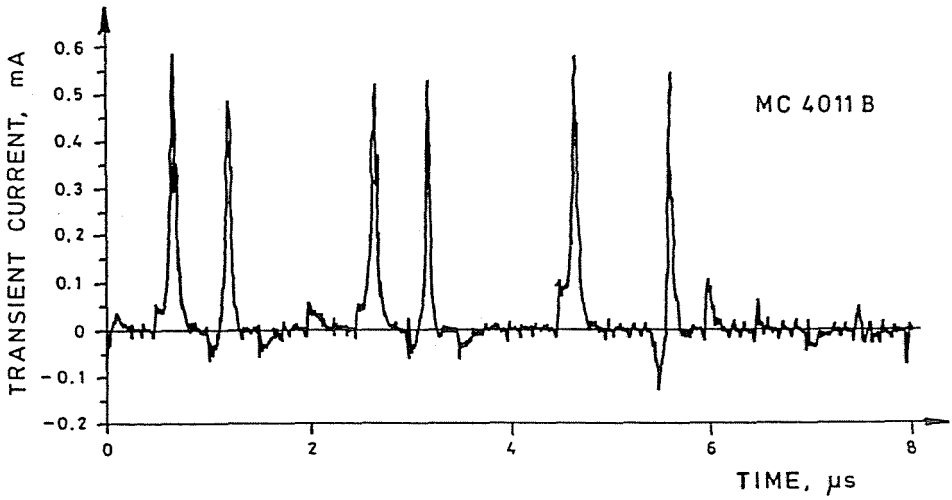


Fig. 6. Transient current of a 2 input CMOS NAND gate

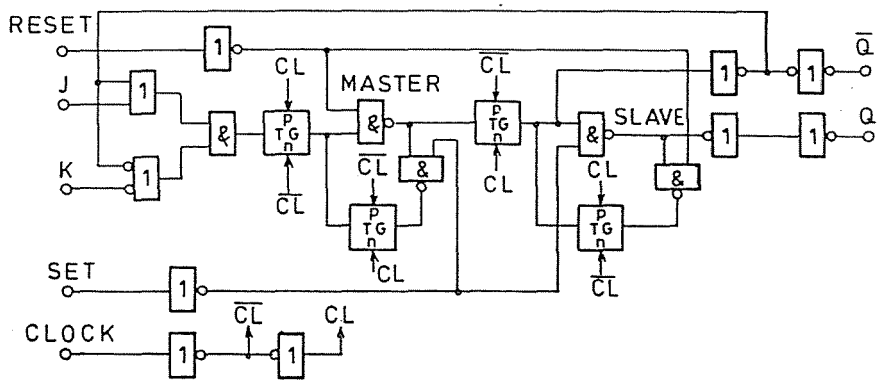


Fig. 7. Circuit schema of HEF 4027 dual JK flip-flop

and dynamic parametric tests. The results were supplied to the PC and we evaluated them. The lot seemed to be perfect in all respects.

We executed the transient current tests, too. Averaging the measurements we got the result shown in *Fig. 8.* (Each device consists of two flip-flops.)

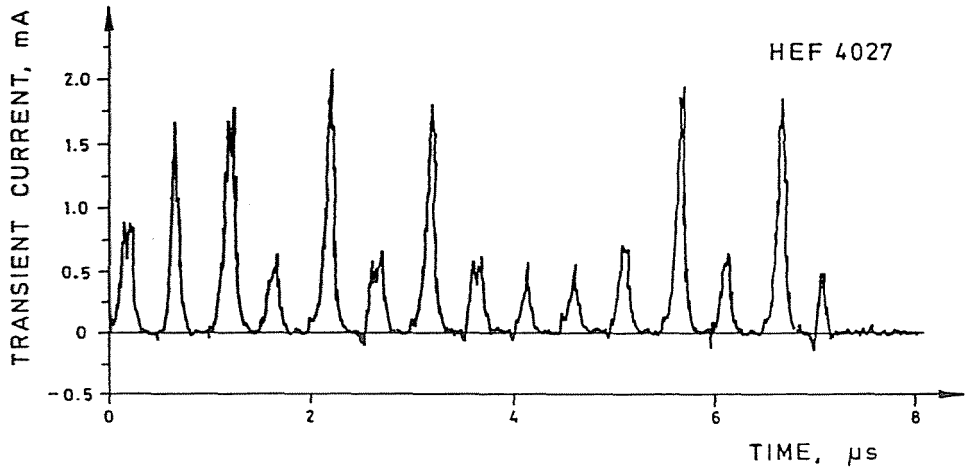


Fig. 8. Transient current of HEF 4027 — an average of 2000 measurements

In this work the next statistics were calculated:

a) The mass mean value and dispersion of the current at each time of the transient.
b) The mass mean value and dispersion of the power at each time of the transient.
c) The time mean value and dispersion of the current for each IC under test.
d) The time mean value and dispersion of the power for each IC under test.

The time mean values evaluated for the whole test cycle show that most ICs are nearly the same, only some of them are different. The mass mean values as a function of the time show it in detail.

Comparing the individual results to their average we can find two types of differences:

a) There is a significant difference in amplitude: there are higher or lower current spikes, as demonstrated in *Fig. 9.*
b) There is an irregular spike on a wrong place, shown in *Fig. 10.*

We had the devices with normal and abnormal results together, and took them to control remeasure. We got the same good results as before. The number of questionable parts was 14.

5. We put the whole lot in an oven for 2000 hours and stored them at the maximum storage temperature 150 °C.

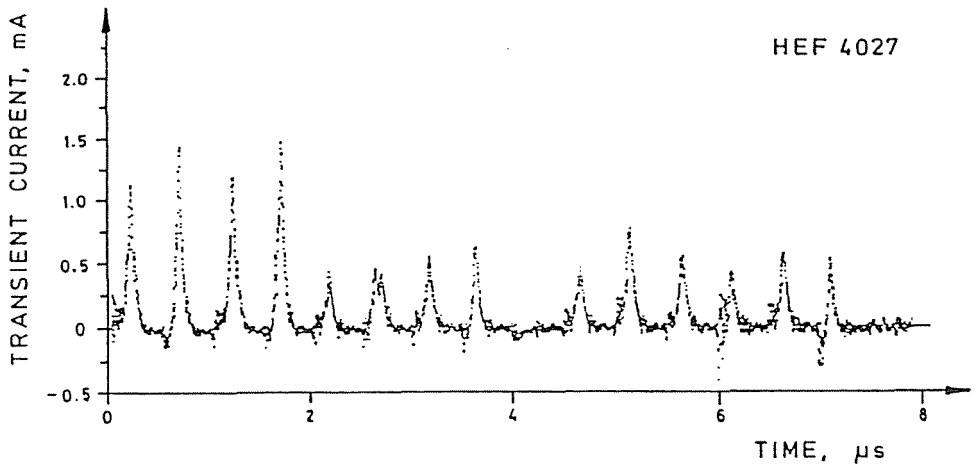


Fig. 9. Different current spikes of irregular amplitudes in the transient current diagram

By the Arrhenius equation in the case of thermally activated processes — most of the failure mechanisms in ICs belong to this category — the acceleration factor due to temperature is

$$a = t_2/t_1 = \exp\{(E_a/k)((1/T_1 - 1/T_2)\}\ , \qquad (1)$$

where T_1 = absolute temperature 1, deg. K
T_2 = absolute temperature 2, deg. K
t_1 = time to failure at T_1
t_2 = time to failure at T_2
E_a = activation energy
k = Boltzmann's constant

For the most important failure mechanisms the values of activation energy are shown in *Table 1* [8].

The storage at 150 °C for 2000 hours is equivalent about to 0.6 – 200×10^6 hours at 25 °C depending on the failure mechanism.

6. After the high temperature storage we repeated the functional and parametric tests.

The result of the measurement: two devices had functional defects, — and both belonged to the questionable group of 14 devices mentioned above.

The result of our experiments seems to justify our hypothesis.

We believe that the longer term of high temperature storage or another investigation (e. g. storage under supply power, work under higher

Table 1
Activation energy values for common failure mechanisms

Failure mechanism	Temperature activation energy (eV)
Silicon junction defect	0.8
Masking (poly, diff., etc.) defect	0.5
Metallization defect	0.5
Contamination (surface and bulk)	1.0
Charge loss (EPROM's)	0.9
Assembly (bond, die att., etc.)	0.5

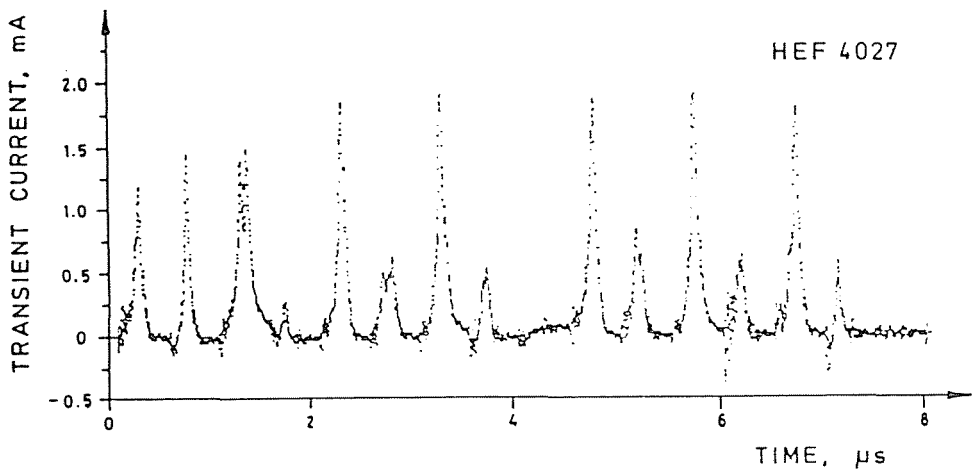


Fig. 10. Different current spikes at wrong places in the transient current diagram

supply voltage etc. or their combination) would give closer correlation between the estimated and the obtained results.

Conclusions

The theoretical and experimental study of the power supply current indicate a relation between the irregular current characteristics, the hidden failures and, as a consequence, the lifetime of the device. Determination

of the laws of the relation requires further deep and long research at every level — elaboration of the common theory, and specification of the methods for circuit families and types.

We should answer some more questions: What level of differences in current characteristics does really show a failure? Is there a usable estimation method between the current anomalies and the lifetime.

In any case, the first results are promising and there is a serious demand for further results in practice.

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