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MOULDED, PLASTIC PGA PACKAGES

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Abstract

The increase of the size of IC chips and the numbers of the pins made it necessary to develop a new kind of package a couple of years ago. PGA packages have appeared and have been used. The authors of this article present a new type of plastic PGA construction. The technology of the package combines the advantages of the production of moulding technologies of packages with PWB. The new plastic PGA package has good electrical and thermal properties and it is cheap. The construction and technology used allow to meet the demands of individual consumers as well – by shortening the time from design to manufacturing. The article describes in detail the testing of the thermal properties of the plastic PGA package.

Keywords: package, PGA, heat flow.

1. Requirements for IC Packages

The packages have to provide undisturbed working conditions for ICs, protecting against mechanical and climate effects determining the external dimension of the circuit and makeing its mounting on the PW board possible.

When choosing the package, the developer and the manufacturer of the IC have to consider the following points of view carefully:

- Does the reliable working of the circuit require dense (e.g. DIL) or air cushion (e.g. CCC) packaging. The latter permits a hermetic seal but the increase of the expenses is significant.
- The package has to conduct the heat resulting from the operation of IC to prevent harmful overheating.
- The size, material and form of the package and the position, form and size, etc. of the pins should contribute to providing optimum electrical parameters required from the IC (e.g. power dissipation, frequency, etc.).

- The IC chip should be mounted easily and automatically into the package. Between the chip and the package pins a reliable wire bounding of high stability should be realized.
- During the packaging steps (e.g. sealing), the chip must not be damaged.
- Packages should have a proper number of pins for VLSI chips, too.
- Packages should be cheap, of small size and can be produced in mass.
- Packaged IC should be simply measured.
- Packaged IC should meet the demands of up-to-date mountability.
- Packages must not be damaged during transport, mounting and use.

In the future the construction and technology of IC packages must adjust to the chips solving more and more complicated and complex tasks. In the first table the characteristics of some typical semiconductor chips can be seen that made planning of new packages necessary in the past years [10].

Table 1
IC chip parameters trends

	Logic		Memory	Micro-	Linear
	ECL	CMOS	MOS	processors	
Pins	300	400	28	100	< 50
Die size [mm]	10 × 10	10 × 10	5 × 10	10 × 10	5 × 5
Power [Watts]	12	< 1	1	2	3
Speed-Rise-Time [ns]	<1	2	2–5	5–10	2

2. The Construction and Technology of Moulded PPGA Package

The body of the moulded PPGA (Plastic Pin Grid Array) is produced by moulding while the main inner assemblies of the package are produced by manufacture of printed wiring board. The package is prefabricated and after the chip-attachment only the sealing operation must be performed. In the package there is a cavity down for the chip (*Fig. 1*). It allows improvement of the power dissipation on the chip in the package, as shown in *Fig. 1* (constructions *b* and *c*). Naturally, in the case of the construction 'c' (*Fig. 1*) other dissipators can be bounded on the cooling block.

The Department of Electronics Technology of the Technical University of Budapest has produced the PPGA package in a variety of 48 and 64 pins.

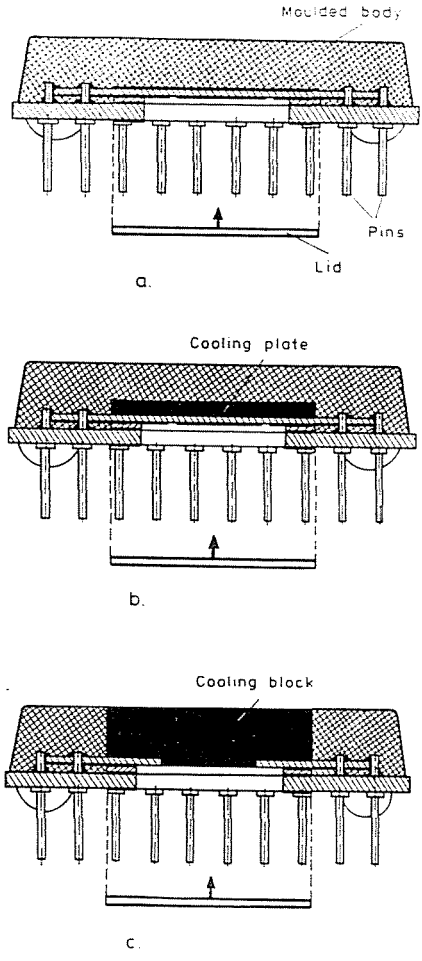


Fig. 1. The choice of the PPGA packages:
a. package without a dissipator;
b. package with a cooling plate;
c. package with a cooling block

In the following, we present the construction of PPGA-64 package as an example.

The PPGA-64 package consists of three main parts:

1. inner assembly,
2. moulded body,
3. lid.

The body is formed by moulding the inner package assembly.

The inner assembly consists of the following parts:

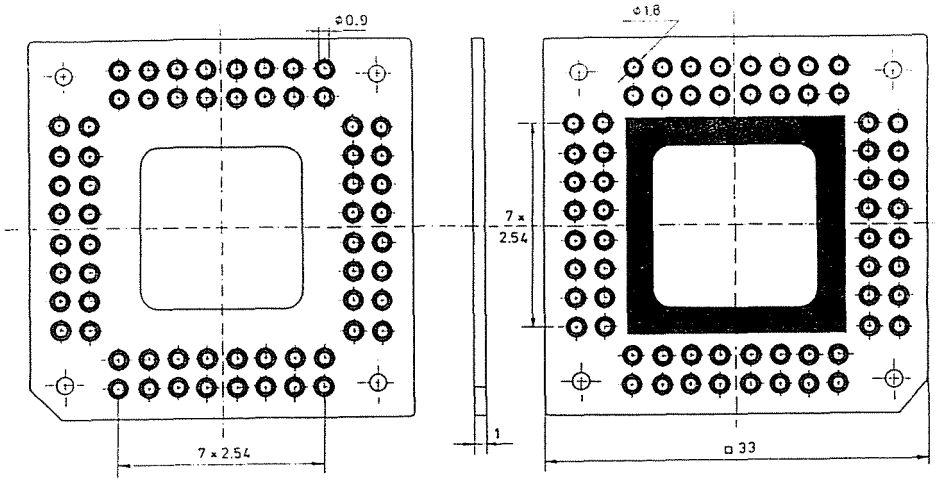


Fig. 2. Ground plate of the PPGA-64 package

- basic plate (PWB),
- distant-keeping plastic frame,
- pins (64 pieces),
- mounting plate (PWB),
- chip holder (metal plated ceramic substrate).

The basic plate is black, double sided (Cu = 2 × 12 μm) PWB; the thickness of PWB is 1 mm (*Fig. 2*). The manufacturer of the basic material is Schweizerische Isola Werke. On four edges of the basic plate made by cutting, size square 33 mm, in 2-2 rows on the grid 0.1" there are total 64 pieces 0.9 mm diameter hole plated through hole solder pad.

In the middle of the basic plate there is a square 14 mm window for the encaseing of distant keeping frame *(Fig. 3)*. Around the window on one side of the plate, there is a galvanic Sn plated metal frame, its width is 2.5 mm, patterned from Cu layer, its thickness is 10 μm. The lid of the package can be bounded to this metal frame by gluing or soldering.

When moulding the packaging material flows through the 1.5 mm diameter holes, being on the four corners of the basic plate, forming spherical segments, that are keeping distance between the package and the PWB (*Fig. 8*).

The distant-keeping plastic frame (*Fig. 3*) can be pressed into the window of the basic plate. The distant-keeping frame is produced by moulding from an identical material with that of the body. The distant-keeper has a double function:

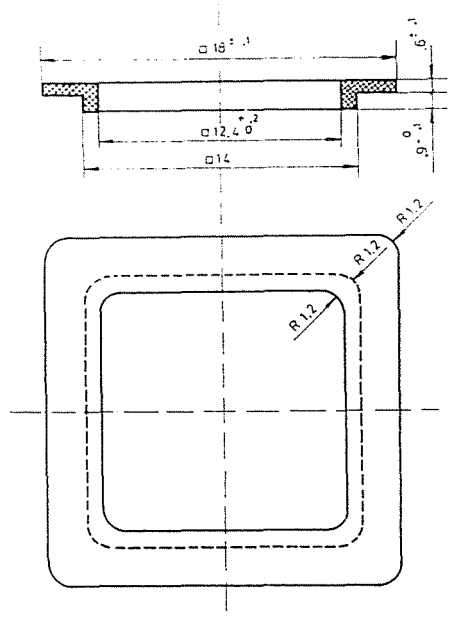


Fig. 3. Moulded distant-keeping plastic frame

- to produce a cavity of proper depth for the chip without increasing the thickness of the basic plate,
- to cover the jagged edges of the window produced by cutting in the basic plate.

The pins are soldered into the basic plate containing the distant-keeper frame. The pins are collared cylindrical studs (*Fig. 4*), their material is an alloy of CuZn 37 and F 45; 2.5 μm Ni +5...8 μm Sn. The pins are perpendicular to the basic plate, their stretching length is 5.1 mm. From this their mounting length is 3.5±0.1 mm because the size of the spherical segments – produced on the lower plane of the package to keep the distance – must be subtracted from their stretching length.

The 2.8 mm part of the pin (see *Fig. 4*) is mounted partly to the basic plate (on the inner side) and partly to the mounting plate by soldering (*Fig. 7*). The stretching strength of the pins is increased by soldering them to the solder pads produced on the basic plate. It also serves to prevent the plastic flowing in the leak between the pins and the metal plated holes on the basic plate during moulding.

The *mounting plate* is a black PWB (typ. FR4), containing Au plated through holes and conductors. Its thickness is 0.4 mm, its size is square

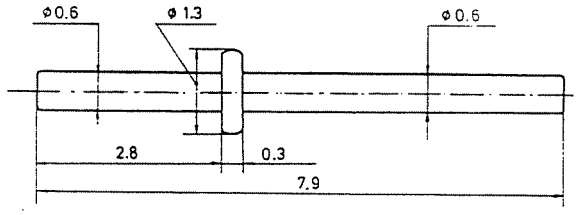


Fig. 4. Pin of the PPGA-64 package

28.28 mm (*Fig. 5*). The board is manufactured by the ISOLA Düren company.

The four corners of the mounting plate are cut 3 mm ×45° in order to make encapsulating material flow easier.

In the middle of the mounting plate there is a window for the chip square 8.1 mm. It is covered by the chip holder (*Fig. 6*).

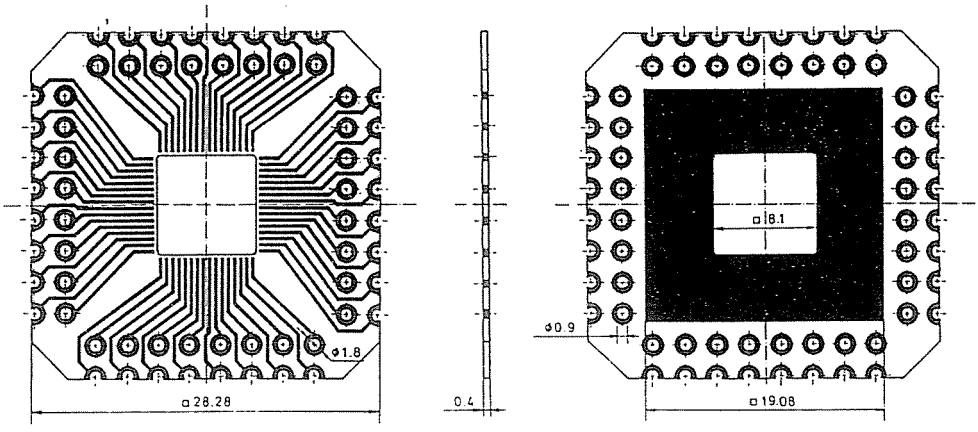


Fig. 5. Mounting plate of the PPGA-64 package

The mounting plate has conductors on the surface; these start from the solder pads (their width is 0.3 mm, near the window 0.2 mm) and approach to the window up to 0.25 mm. On all the four sides of the window of the mounting plate there are 16 pieces of gilt pads, their grid is 0.5 mm, width is 0.3 mm and their length is 1.7 mm.

On the back side of the mounting plate there are 1.8 mm diameter Au plated solder pads belonging to the metal plated holes on the four edges of the sheet in 2 rows each, totalling 64. It can be seen well in the figure that

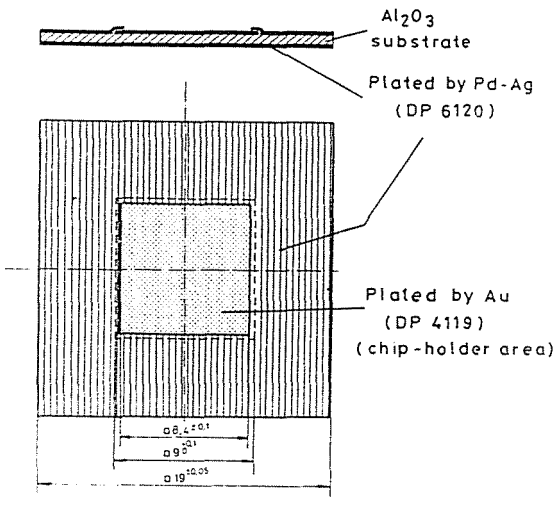


Fig. 6. Chip holder of the PPGA-64 package

a part of the external hole row must have been cut to keep a proper stand off between the package and the mounting plate during moulding.

On the back side of the mounting plate the chip holder can be mounted (by soldering our gluing) to the frame surrounding the window.

According to the customer's demand, the mounting plate can be produced from a multilayer PWB with a small surplus cost. Co-ordination of the layout of multilayer PWB and the bonding strategy of IC chip mounted into the package can favourably influence the utility of the package.

The chip holder, that is square 19 mm ceramic (Al_2O_3; AlN or BeO), is covered with thick film layers on both sides (*Fig. 6*). Instead of the materials visible in the figure some others can be used as well. For example, on the back side a Cv thick film layer fired in N_2 gas, can be applied.

From the material choice mentioned earlier the usage of AlN substrate having a good thermal conductivity (140...170 W/mK) is recommended.

For plating ceramic chip holder thick film technology has been used. The chip holders have been produced on a substrate square 4" (16 pieces could be placed) and then we cut them with laser into small units.

The technology of the inner assembly of PPGA-64 package is (*Fig. 7*):

- pressing the distant-keeping frame into the basic plate,
- soldering 64 pins into the basic plate with a solder of high melting point,
- mounting the chip holder on the mounting plate (e.g. by reflow soldering),

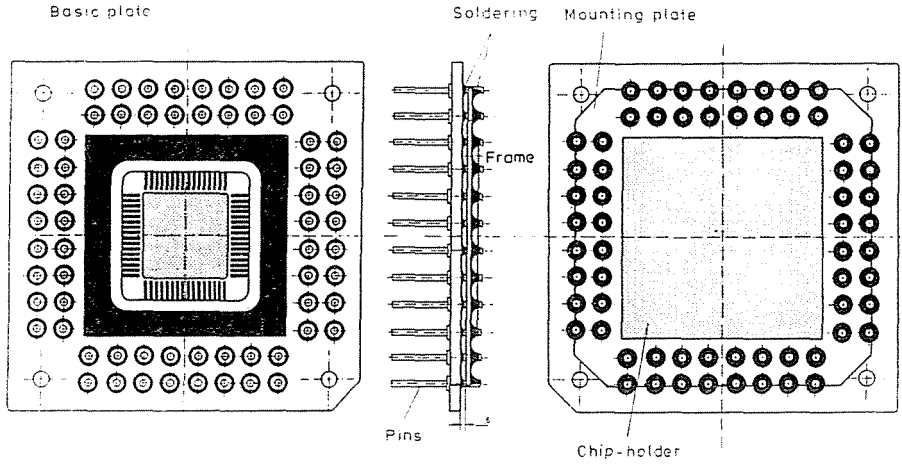


Fig. 7. Inner assembly of the PPGA-64 package

– pulling-over the mounting plate on the pins mounted in the basic plate and interconnecting the pins and the solder pads of the mounting plate by soldering.

The *body* is produced by transfer moulding techniques of the inner assembly of the package (*Fig. 8*).

Multi-cavity packaging tools have been used for moulding. The tool was operated by a moulding press having double (lower and upper) hydraulics. The operation of the machine is hydrostatic, it has an electro-hydraulic control.

When the tool is in open position, the inner assembly of the package must be placed into the bottom mould cavities so that the pins stand perpendicularly upwards to the tool lid. A recessed place has been formed in the bottom mould cavity for the basic plate of the assembly. The basic plate is set onto the edge of the recessed place (frame square 0. 5 mm).

In this way the lid of the moulding tool coincides with the upper plane of the basic plate of the package assembly, placed at the bottom part of the tool.

At the top of the moulding tool only the holes suitable for housing of pins and the cavities forming the distant-keeping spherical segments can be found (*Fig. 8*).

The pouring space formed at the bottom part of the moulding tool is connected with the mould cavities by runners and gates. By proper choice of the place, size and form of the gate of the mould cavity a faultless and dense body of package can be reached.

The characteristics of the moulding material are as follows:

- manufacturer: Plaskon Electronic Materials
- Type number: PS 440
- moulding temperature: 175...185 °C
- moulding pressure: 520–690 N/cm^2
- time of the moulding cycles: 60...90 s
- thermal conductivity: 0.62 W/mK.

The PPGA-64 packages have been exposed to a 8...10 hour annealing. In this way a dense homogeneous plastic package can be obtained.

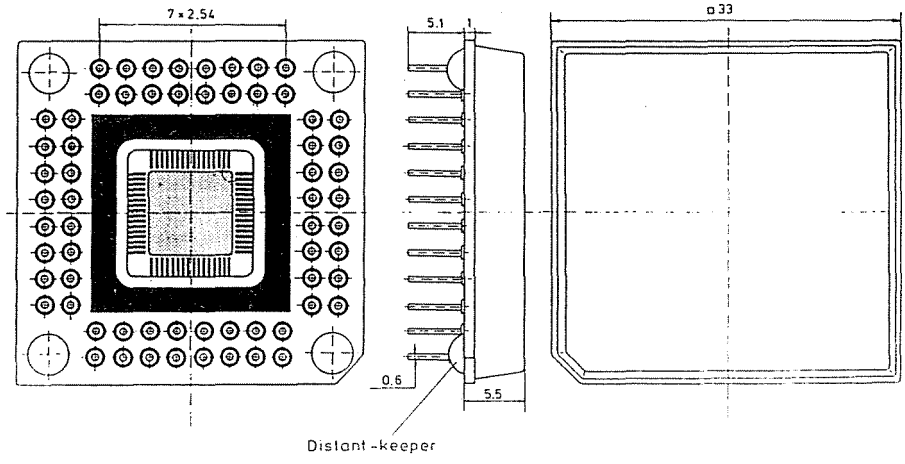


Fig. 8. PPGA-64 package without lid

Into the PPGA-64 package the IC chip has been bounded by gluing on ceramic chip holder. Pads on the IC chip and the Au plated pads formed on the mounting plate have been interconnected by microbounding with wires (e.g. thermosonic bounding). The cavity at the bottom of the package has been filled by silicone gel manufactured by Dow Corning. (Several binds of encapsulation material have been tried [11]).

After chip bounding and protection the PPGA-64 package has been sealed with a lid (*Fig. 9*). The lid can be fixed in two ways:

1. By gluing (the lid is a black 0.4 mm PW board without a Cu coat)
2. By soldering (the material of the lid is an FBZ 0.2 mm thick metal plate coated with a 10 μm thick Sn layer).

The thermal properties of the PPGA-64 package described above can be improved with metal inserts pressed into the body and dissipators placed in them (*Fig. 10*). We deal with this question in detail in the 4th chapter.

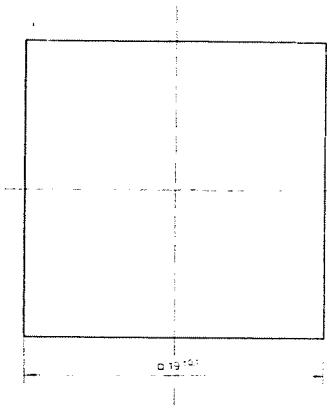


Fig. 9. The lid of the PPGA-64 package

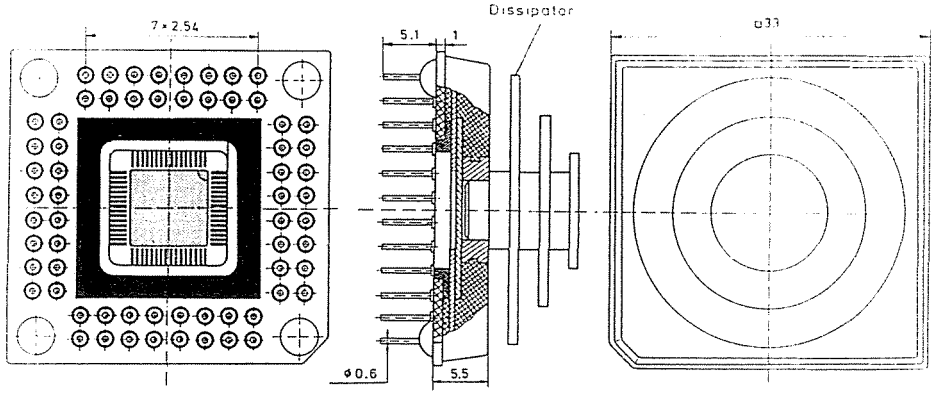


Fig. 10. PPGA-64 package with dissipators

3. Main Characteristics of the PPGA-64 Package

The main characteristics of the PPGA-64 package are the following:

- body size: 33 × 33 × 5.5 mm (meeting the JEDEC standard);
- pin counts: 64;
- arrangement of the pins: along the edges of the lower plane of the package in double rows in the intersections of a 2.54 mm grid array;
- pins:
  - form: cylindrical stud
  - mounting length: 3.5 ±0.1 mm

  - diameter: 0.6 ±0.025 mm
  - the maximum size of the IC chip: square 8 mm
- the chip holder is thick film coated (Al_2O_3, AlN or BeO) ceramic substrate;
- size of the cavity formed for the chip in the mounting plate: 8.1 × 8.1 × 0.4 mm;
- size of the cavity formed for the 'dropping' plastic conform coating of the chip in the package: 12 × 12.4 × 1.6 mm;
- sizes of the pads for the microbounding on the mounting plate:
  - width: 0.3 mm,
  - length: 1.7 mm,
  - pitch: 0.5 mm;
- 1.6 mm stand-off of the package from the PWB is provided by the spherical segments moulded on the basic plate.

4. Measurement and Identification of Heat-Flow in the PPGA-64 Package

4.1. The Measurement Method[1]

To measure the chip-to-ambient or chip-to-package static thermal resistance is a usual method for thermal characterization of the package, but this gives only single-value rating without more information about the heat flow details.

A more complete way is to measure the thermal step-response function (often called the transient thermal impedance). Different regions of this function refer to corresponding regions of the mount structure. Some works [1], [2] deal with the problem of constructing (approximately, at least) the thermal step-response function by splitting the mount structure into regions and joining the individual responses of these regions. Work [2] shows the possibility of recognizing some details of the mount structure from the step-response function. A weakness of this procedure is that it involves a manual and intuitive step: the splitting of step-response into regions.

The method developed at the Technical University of Budapest, Department of Electron Devices is also based on measuring the thermal step-response function [3], [4]. However, during the subsequent mathematical processing an automatic and exact method is used to give finally the ther-

[1]This work is supported by the OTKA project No. 759 of the National Research Found of Hungary.

mal resistance and capacitance map of the mount structure. A detailed discovery of the fine structure of heat flow path becomes possible, with a resolution of 50-100 points along the path. An easy separation of different regions of the mount structure becomes possible (chip, bond, header, cap), together with the calculation of their thermal resistance and capacitance values (or even their geometrical dimensions). The detection and localization of heat transport irregularities is also possible.

Principle of the Method

Here we want to give a very brief summary of the principle of the method. Detailed description can be found in Refs. [4] and [5].

The measured function $a(t)$ is the step-function response of the thermal one-port represented by the device and its mount. The device is excited by a step of the dissipating power and its temperature rise function is measured [4], [7].

One of the simplest $a(t)$ response function is that of the single time constant system. It has the mathematical form of $(1 - \exp(-t/\tau))$. The response of more complex thermal structures can be considered as the sum of many such individual exponential terms with different τ_i time constants and different magnitudes:

$$a(t) = \sum_{i=1}^{n} a_i(1 - \exp(-t/\tau_i)). \tag{1}$$

Thus, it is possible to characterise a thermal system by the (discrete or continuous) distribution of time constants occurring in its response, and by the related magnitudes.

Let's introduce the logarithmic time variable z as

$$z = \ln t \tag{2}$$

and the logarithmic *time-constant distribution* of the response:

$$R(\zeta) = \lim_{\Delta\zeta \to 0} \frac{\text{magnitude related to the time constants between } \zeta \text{ and } \zeta + \Delta\zeta}{\Delta\zeta}. \tag{3}$$

Now the $a(t)$ response can be expressed as

$$a(z) = \int_{-\infty}^{\infty} R(\zeta)(1 - \exp(z - \zeta))d\zeta, \tag{4}$$

where the logarithmic time variable is used. This is a convolution-type differential equation for the unknown $R(\zeta)$ function.

After some mathematical operations we obtain

$$\frac{d}{dz}a(z) = R(z) \otimes W(z), \tag{5}$$

where

$$W(z) = \exp(z - \exp(z)) \tag{6}$$

and $\otimes$ is the symbol of the convolution operation.

The first step of identification is based on *Eq* . (5). Transforming the response function to the logarithmic time variable, differentiating it and finally deconvolving it by the fixed function (6) gives the $R(z)$ time-constant spectrum of the investigated thermal one-port.

The second step is simply the transformation from the Foster normal form of rc networks to the Cauer form. From the time-constant spectrum to the lumped-element Foster equivalent we have a direct way (*Fig. 11a*), involving only some discretisation considerations.

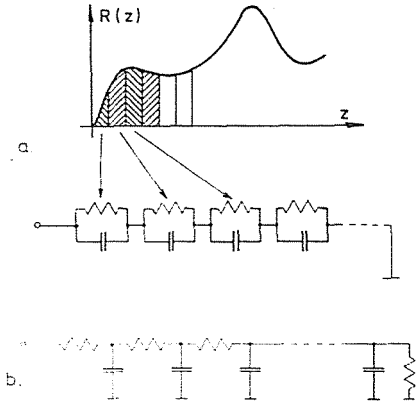


Fig. 11. Foster and Cauer equivalents

However, the Foster network cannot be considered as a direct image of a thermal structure. It is suitable to transform the Foster network into the Cauer equivalent. The latter includes only node-to-ground capacitances (*Fig. 11b*) and, thus, it can be regarded as a discretised image of a real heat flow structure.

Practical Considerations

For thermal characterisation of the package, a chip was encapsulated into it containing only one bipolar transistor. This transistor has worked as a

probe. A step-wise change of its collector voltage means a step-function power excitation. Measuring the V_{BE} voltage whilst the emitter voltage is kept at a constant value gives the junction temperature.

The measuring procedure is controlled by a microcomputer. The arrangement is shown in *Fig. 12.* The measuring circuit is connected to the microcomputer by a D/A and an A/D converter, both are of 10-bit accuracy. The first is devoted to control the dissipation step while the second is to measure the V_{BE} voltage.

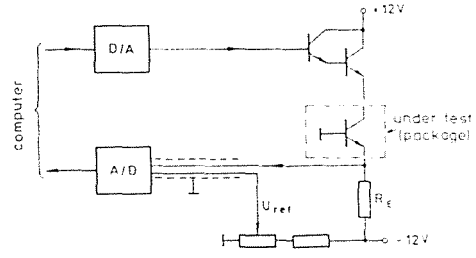


Fig. 12. The measurement arrangement

Since before processing the response function is transformed according to *Eq.* (2), it is suitable to control the sampling rate in a quasi-logarithmic way – in order to obtain a quasi-equidistant sampling on a logarithmic time scale. We have reached good results with changing the sampling rate from 6 μs to 3.5 seconds. The total number of samples is about 2000 while the resolution of the temperature sensing was 0.05 °C.

For the deconvolution we have used an iterative algorithm based on the Bayes's postulate of the probability theory [8]. Although the procedure is rather time-consuming (500 iterations as a mean number), it fairly matches to the given problem.

The Structure Function

If the one-dimensional heat flow model is a reasonable approximation for a given structure, then the different sections of the Cauer network correspond to the different parts of the physical structure well. 'One-dimensional' means here not only the heat propagation in bar-shaped regions but in cylindrical and spherical propagation sections as well, thus, the above restriction is not a serious one. Many packages of ICs satisfy the quasi-one-dimensional condition for the heat flow.

The heat flow equation for a one-dimensional structure is

$$\frac{\partial T}{\partial t} = \frac{1}{c(x)} \frac{\partial}{\partial x} \left(\frac{1}{r(x)} \frac{\partial T}{\partial x} \right), \tag{7}$$

where $r(x)$ is the heat resistance per unit length, $c(x)$ is the heat capacitance per unit length. Substituting the x co-ordinate by the $\rho(x)$ heat resistance between the heat source and the point in question (as introduced by [9]) yields

$$\rho(x) = \int_0^x r(\xi)\, d\xi, \qquad r(x) = \frac{d\rho}{dx}. \tag{8}$$

With this

$$\frac{\partial T}{\partial t} = \frac{1}{K(\rho)} \frac{\partial^2 T}{\partial \rho^2}, \tag{9}$$

where

$$K(x) = \frac{c(x)}{r(x)}. \tag{10}$$

The latter quantity is proportional to the squared cross-section area of the heat flow path for a given material. For example, in the case of silicon

$$K_{\mathrm{Si}} = 2.58 \cdot 10^8 A^2, \qquad W^2 s/^\circ C^2, \tag{11}$$

where A is the cross-sectional area.

Let us draw the K-values as a function of the source-to-point heat resistance. This $K(\rho)$ function properly represents the physical heat flow structure – this is the *structure function* introduced in [4].

4.2. Investigations on the PPGA-64 Package

Evaluation of Results, Structure Identification

The evaluation process is presented on some measuring results of the investigated pin-grid array package. At first we have to separate the distinct regions of the heat flow path (*Fig. 13*).

First we have to note that the horizontal axis of the function corresponds to the $\rho(x)$ heat resistance referring to the dissipating source. The origin is related to the dissipating element (e.g. the transistor within the probe-chip), while the right-hand end of the axis corresponds to the ambience. So the data value on the right-hand end is always the whole R_{thja} junction-ambient heat resistance (38.9 K/W in this case).

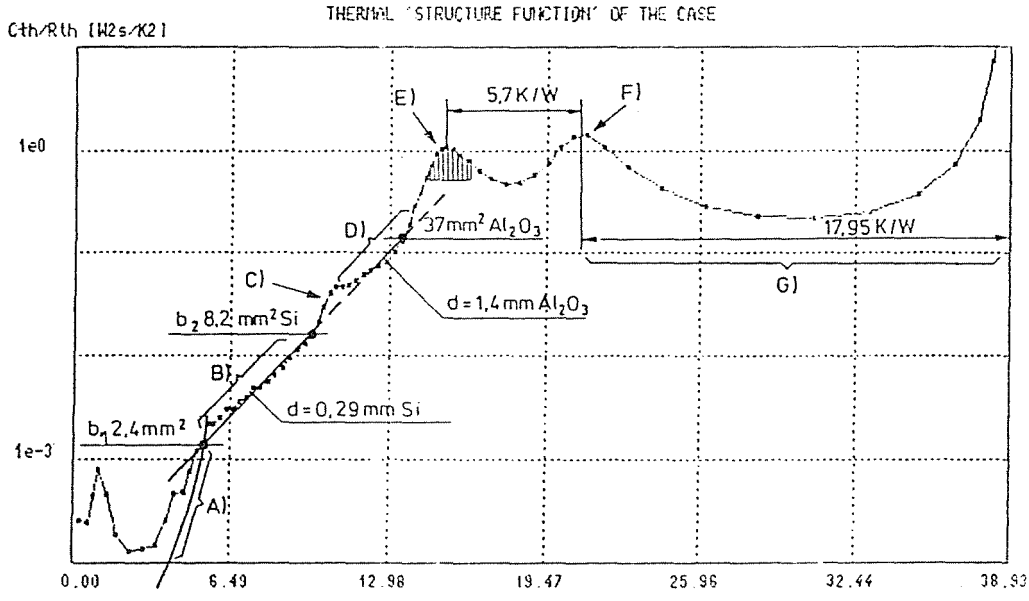


Fig. 13. Structure function of a pin-grid array package

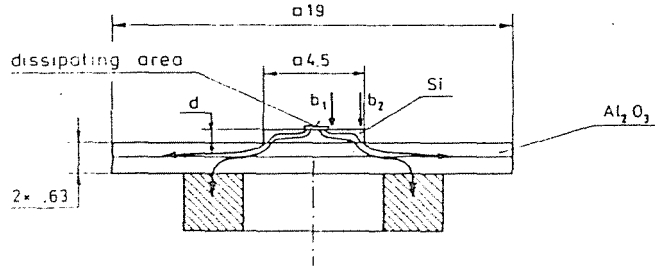


Fig. 14. The chip and the ceramic header

The left-third part of the function can be identified as the mapping of heat flow path within the chip. To explain this, let us consider the chip and its ambience with real geometric data (*Fig. 14*).

Considering that heat conductivity of the silicon is about 5-times greater than that of the Al_2O_3 ceramics, we can suppose that (if and where possible) the heat flows in the silicon. Thus the heat path:

A. Shows spherical symmetry immediately below the heat source,

B. Within the chip a radial spreading dominates with cylindrical symmetry,

C. At the border of the chip the heat traverses to the ceramics.

The radial spreading of B can be easily recognized from the fact that these regions appear in the logarithmic structure function as straight lines. This line is shown in *Fig. 13.* The slope of this line is directly related to the thickness of the silicon chip [4]. In this case, the calculated chip thickness is $d = 0.29$ mm, which is a quite realistic result.

The vertical axis of the structure function is closely related to the area of the heat flow cross-section. Calculating the cross-sectional area for the two limits of section B yields 2.38 mm^2 and 8.2 mm^2, which reasonably correspond to the cross-sections of the real structure marked by **b1** and **b2.**

A small local peak is appearing on the C region of the structure function. Considering that the vertical axis is proportional to the heat capacitance, this can be identified as the excess heat capacitance of the solder accumulated at the border of the chip.

As conclusion we can state that the structure function region between the origin and point C is the mapping of the chip itself; thus, the part characterising the case is lying on the right of C.

In the region of the function corresponding to the case two striking peaks (marked by E and F) can be distinguished and on the right side a wide minimum can be seen. On the left side of peak E a gradually rising region appears.

D. Since the Al_2O_3 ceramics is a better heat conductor than the moulding material, the heat spreads laterally in the ceramics. The thickness of the Al_2O_3 plate can be obtained from the slope of region D. The calculated value is 1.4 mm, while the real one was 1.26 mm.

E. This peak is the effect of the relatively concentrated heat capacitance of the ceramics plate and the metal ring soldered to it. This can be proved by calculating the heat capacitance of them and by comparing this value to the area under the function in the region E.

F. This maximum corresponds to the capacitance of the whole case (including moulding material, pins, etc.).

G. It is conspicuous that along this region the heat capacitance is much lower than at the former peaks. This region corresponds to the heat transport by convection between the package and the ambience, characterised by the very low heat capacitance of the air. A thermal resistance of 18 K/W can be identified between the outer surface of the package and the ambience.

Further Results for the PPGA-64 Package

We have investigated a great number of packages under various circumstances. In all packages the structure function was analysed. The most important conclusions are as follows.

Thermal resistance between the ceramics plate and the whole body of the case. The mean value calculated from the measuring results of seven samples was 5.87 K/W (note that these samples were not provided with a dissipator).

Effect of soldering into a PW board. Three samples were measured both in free position and soldered into a PW board. In the latter case the thermal resistance is evidently smaller. The average value of the difference was 3.45 K/W. In the thermal equivalent circuit the heat removal through the pins of the case towards the ambience can be modelled with a parallel thermal resistance between the package and the ambience. If we calculate that value, about 70 K/W is obtained.

Effect of dissipator mountings. Numerous measurements were carried out on packages mounted with different dissipators. The dissipators were made from aluminium and have one or more disc-shaped fins (see *Fig. 10*). Their surfaces are either untreated or blackened. We must conclude that the present form of the dissipators is rather inefficient. The dissipator with two fins and with untreated surface diminishes the junction-ambient thermal resistance only by 7 % while a blackened one gives an improvement of 18 %.

Effect of the mounting method of the chip. We have investigated two possibilities. In the first case the chip was glowed into the package, while in the second one soldering was used. The glue caused an excess thermal resistance, which is considerable; its average value was 3.1 K/W. Thus, the glowing of the chip is disadvantageous; rather soldering is recommended.

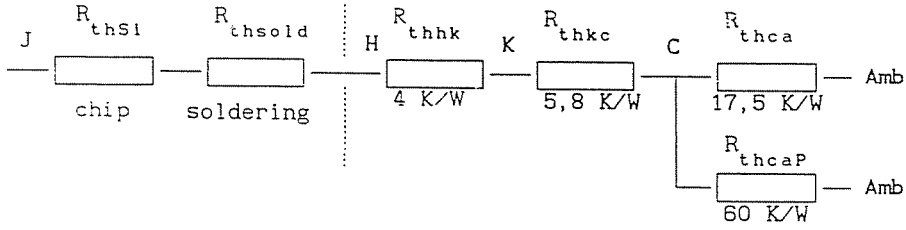
Based on the above considerations a steady-state thermal equivalent network can be constructed for the case as shown in *Fig. 15.*

R_{thSi} is the thermal resistance of the silicon chip itself. If the dimensions of the chip are e.g. $5 \times 5 \times 0.4$ mm and the heat sources are uniformly distributed on the surface, this resistance is about 0.1 K/W. A guess for the soldering is about 1 K/W. Thus, the whole thermal resistance of the case (soldered into a PW board) is

$$R_{thja} = 24.4 \text{ K/W}.$$

If the case is mounted with a finned dissipator, the equivalent circuit of *Fig. 16* is valid. In this latter case the whole thermal resistance is (again for the package soldered in PWB)

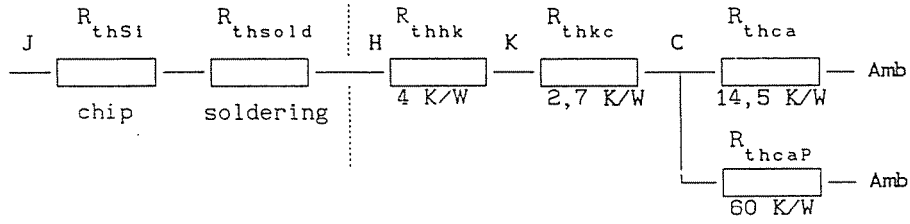
$$R_{thja} = 19.4 \text{ K/W}.$$



J = junction
H = ceramics plate, center
K = ceramics plate, periphery
C = whole case

If not soldered to PCB, R_{thcaP} must be left out.

Fig. 15. Thermal equivalent circuit of a package (without finned dissipator)



J = junction
H = ceramics plate, center
K = ceramics plate, at the contact of the dissipator
C = whole case

If not soldered to PCB, R_{thcaP} must be left out.

Fig. 16. Thermal equivalent circuit of a package (with dissipator)

Note that this thermal resistance can be remarkably reduced by using a forced air cooling on the dissipator mount.

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