PERIODICA POLYTECHNICA SER. EL. ENG. VOL. 36, NO. 1, PP. 19-37 (1992)

SWITCHED-CAPACITOR CIRCUITS WITH REDUCED INFLUENCES OF PARASITIC CAPACITANCES, SWITCH RESISTANCES AND AMPLIFIER NON-IDEALITIES

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Received: April 11, 1992.

Abstract

Two design techniques are described for decreasing and possibly eliminating the effects of element imperfections in switched-capacitor (SC) circuits. The first technique is devoted to the operational amplifier non-idealities. It is centered on decreasing the number of amplifiers in the circuits by multiplexing their use. The second approach is based on the minimization of the sum of the square of the differences between the time (or the frequency) response of the circuit with and without non-idealities. This technique can be used to control over the effects of finite switch resistances, finite gain-bandwidth product of the amplifiers as well as parasitic capacitances. Computer results have revealed that the responses of the optimized circuits are nearly the same as that of the ideal ones. Illustrative examples are given illustrating the efficiency of the proposed techniques.

Keywords: Non-ideal effects in SC circuits, analysis of non-ideal SC circuits, compensation of non-idealities in SC circuits, multiplexed operational amplifiers.

Introduction

The most important reason for the development of analog MOS integrated circuits is the need to fabricate fully integrated high-quality analog circuits. In this respect switched-capacitor realization of such circuits seems to be one of the up- to -date powerful techniques. It is known that by using SC technique all passive elements and active building blocks can be realized by capacitors, MOS switches and operational amplifiers. The main advantages of this realization are:

1) results in circuits whose time constants depend on capacitor ratios that are well controlled on an integrated circuit fabrication,
2) allows large area resistors to be replaced by smaller SC equivalents.

However, there are some imperfections of SC circuits that may limit their use specially at high frequencies. Namely these are:

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1) parasitic capacitances,
2) on- and off-resistances of the switches,
3) low input and high output impedances of operational amplifiers together with their finite gain-bandwidth products.

Trials have been done to decrease the effect of parasitics through the development of stray insensitive structures [1]. However, such circuits are only free from bottom plate stray capacitances and contain, in general, a large number of switches and/or operational amplifiers that have great influences due to their non-idealities. Amplifier non-idealities may be decreased through the use of unity gain buffer structures [2]. However, in the buffer-based circuits the relatively large buffer dc offset voltage, the buffer gain error and the sensitivity to the parasitic capacitance at the buffer input may limit their use. In [3] a method has been presented for the design of unity-gain buffer based switched-capacitor biquads in which both the offset voltage and the gain error are compensated and the sensitivity of the parasitic capacitance is low. In fact, the compensation of offset voltage and the non-linear effects (such as slewing rate) are not included. These will be the subject of a further publication.

This paper presents two methods for controlling the effects of finite switch resistances, operational amplifier non- idealities as well as parasitic capacitances. The first method is devoted for the operational amplifier non- idealities; and it is centered on decreasing the number of amplifiers by multiplexing their use. For small and moderated circuits, this method is powerful. However, for big circuits, the multiplexing process may complicate the clocking scheme and may raise the operating frequency. The second approach is developed to overcome the above mentioned problems by minimizing the square of the differences between the time (or frequency) responses of the circuit with and without the imperfections. Capacitor values of the circuit are used as free parameters. During minimizations process capacitances of the ideal circuit are used as initial values. The resistances of the switches and the amplifier resistances, gain and bandwidth can be considered as on the data sheets. Also, the maximum expected values of the parasitic capacitances at all the nodes of the circuit are assumed. The results of this process are new values of the capacitances of the non-ideal circuit at which it has nearly the same transfer function (either time or frequency response) of the ideal one. For these purposes, a computer program for analyzing general multi-phase SC circuits has been developed.

Compensation on Non-idealities in SC Circuits

In switched-capacitor circuits, the frequency characteristics of the operational amplifier is the primary limiting factor in the circuit performance. There are several well-known passive compensation techniques which make use of additional passive components to introduce a controlled amount of phase lead that cancels the excess phase lag resulting due to the amplifier's limited bandwidth [4] – [5]. The main difficulty with the passive compensation is that the additional compensating elements must be individually adjusted at specific ambient conditions of temperature and power supply voltage. Consequently, under changing ambient conditions the compensation is no longer satisfactory.

Active compensation techniques, used successfully in active RC filters, have been tried in switched-capacitor filters also, but the reported circuits [6] – [7] need additional operational amplifiers. In [8], an active compensation scheme proposed by BRACKETT and SEDRA [9] for active RC filters had been used in the conventional switched-capacitor double-integrator biquad where no additional operational amplifiers are needed. Unfortunately, this technique is suitable only for small circuits.

First Approach: Multiplexing of Amplifiers

Operational amplifier is conventionally used in the realization of most switched-capacitor circuits. Thus, the performance of the amplifier is an important parameter in the implementation of such circuits. The slew rate, the open-loop gain, the gain bandwidth product, the low input impedance, the high output impedance and the thermal noise are characterizing parameters of the amplifier; and hence the designed circuit. Most of these parameters are frequency dependent and their effect increases with the increase of the operating frequency. The straightforward approach for decreasing the amplifier imperfections is the decrease of their numbers. Multiplexing technique is proposed for the operation of the operational amplifiers that reduces their number significantly. This results in circuits that can work efficiently at high frequencies.

To clarify how the multiplexing technique can be used in decreasing the number of amplifiers, consider the case of seventh-order unit element switched-capacitor filter based on the voltage inversion (VIS) concept [1]. *Fig. 1* shows the prototype unit element realization of this filter. Its design parameters and element values are:

- sampling frequency 24 KHz
- passband cutoff frequency 3.4 KHz

- maximum passband loss 0.2 dB
- stopband edge 5.5 KHz
- minimum stopband loss 45 dB
- element values; $R_0 = 1.0 \quad R_1 = R_7 = 3.1847 R_2 = R_6 = 0.3387$
$R_4 = 0.3046 \quad R_3 = R_5 = 4.9631$

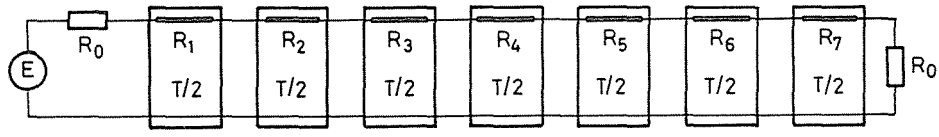

Fig. 1. Seventh-order unit element filter

The conventional method [10], uses 4 operational amplifiers. *Fig. 2* shows an alternative realization where only one operational amplifier is used. Multiplexing the op-amps is based on the fact that one VIS can serve several capacitance loops through using an appropriate clocking scheme, as shown in *Fig. 3.* In *Fig. 2,* switches having the clock pulses $\overline{T}_1$, $\overline{T}_2$, $\overline{T}_3$, $\overline{T}_4$ and $\overline{A}$ are operated in complementary with those having T_1, T_2, T_3, T_4 and A respectively. Computer simulation of each network is obtained through the evaluation of its output response sampled at node (2) due to an impulse input at node (1). It has been shown that for ideal switches and operational amplifiers, the passband and stopband loss responses match exactly the theoretical responses obtained from the transfer function. Also, due to the use of integrator voltage inverting switches and the suggested clocking scheme, the resulting structure is completely insensitive to the bottom plate parasitics. Considering the case of non-ideal switches and amplifiers, the circuit given in [10] and the multiplexed circuit of *Fig. 2* are analyzed using the method given in [11]. *Fig. 4* shows the loss responses of the two circuits together with the ideal circuit. The following non-idealities are considered:

1) for the amplifiers: 500 KΩ input resistance, 100 Ω output resistance, 500 KHz gain-bandwidth product.
2) for the switches: 100 Ω switch-on resistance.

From *Fig. 4* it is clear that decreasing the number of the operational amplifiers (by multiplexing their use) decreases the effect of non-idealities of the elements.

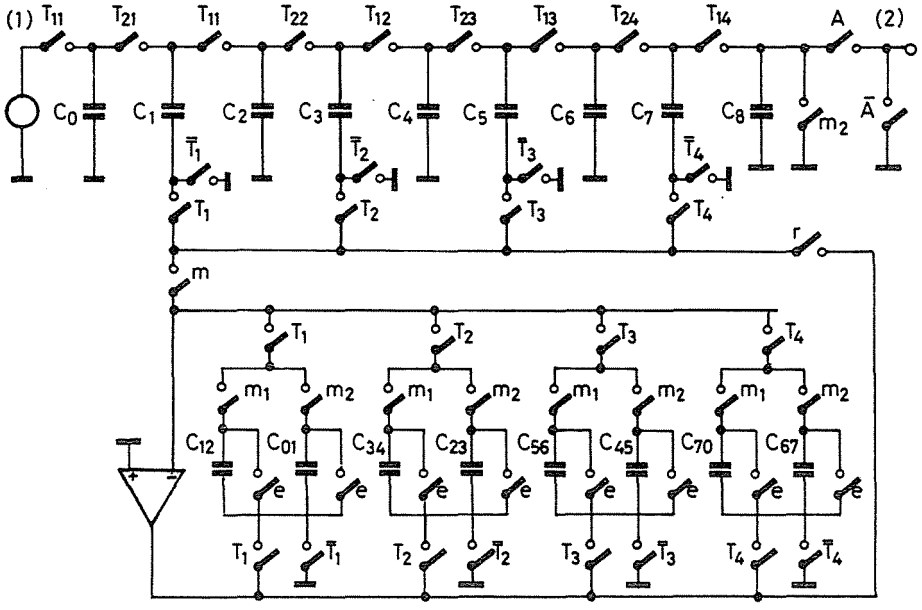

Fig. 2. Switched-capacitor realization of the 7th order UE filter

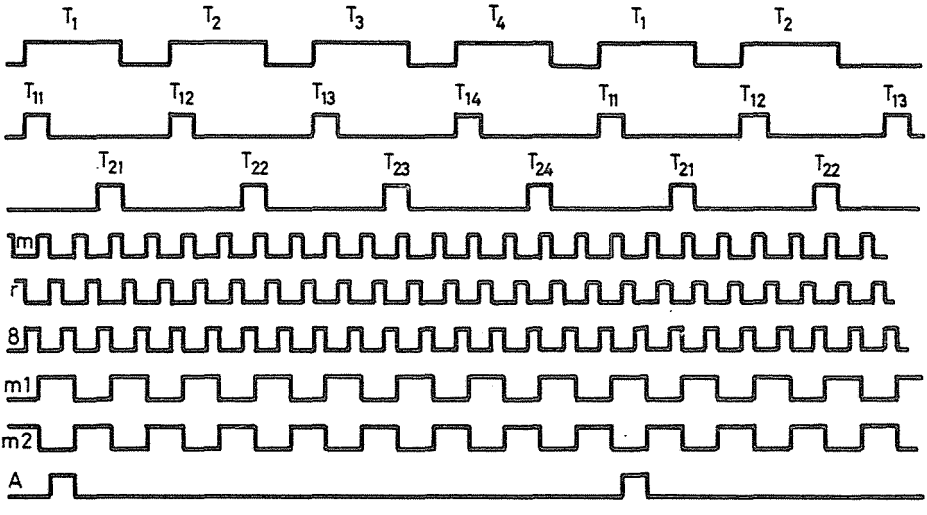

Fig. 3. Timing diagram

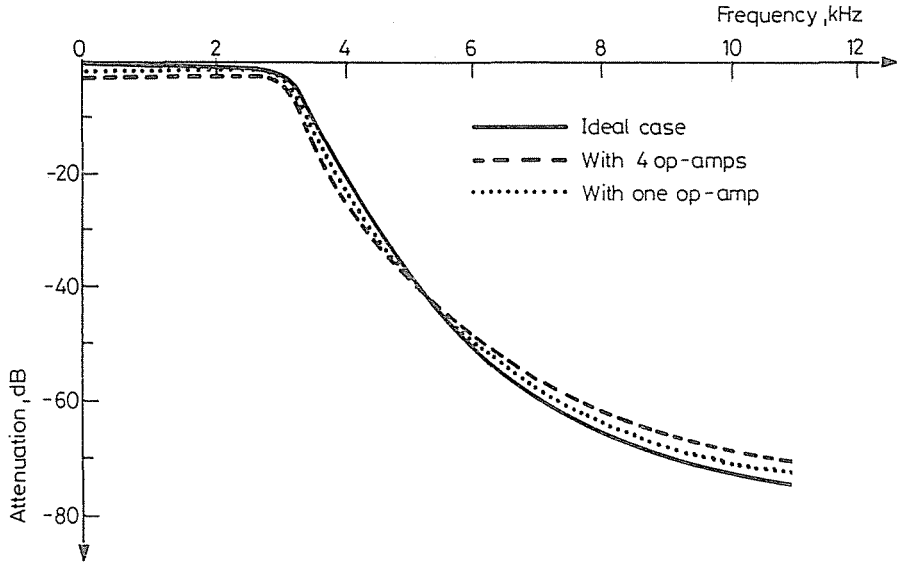

Fig. 4. Frequency response of 7th order UE low-pass filter

Second Approach: The Optimization Method

The method described here compensates the deviation in the frequency response of switched-capacitor circuits applying finite switch-on resistances and non-ideal operational amplifiers. The non-idealities of the amplifier include: the finite gain-bandwidth product, finite input and output resistances. It is worth to be noted that no additional compensation elements are required.

Analysis of Switched-Capacitor Circuits Having Non-Ideal Elements

For the purpose of the optimization method used for the compensation of non-idealities presented in this paper, a method for the analysis of general multi-phase non-ideal switched-capacitor circuits is introduced. This method is developed to take into consideration the combined influence of the operational amplifier non-idealities and the finite switch-on resistances. Also, it can be used for the analysis of lossy switched-capacitor circuits when the presence of real resistors is permitted. The method depends on reducing the modified nodal admittance matrix in each phase to its state space form; where the number of states depends on the number of capac-

itors in action at that phase. Then for a unit impulse input at any phase k, the resulting time response at any node l can easily be evaluated. Consequently, the frequency domain response can be obtained. The proposed approach is implemented in a computer programme that is capable of analyzing large circuits with complicated clocking schemes [11]. The main features of this approach can be summarized in the following:

i) The indefinite admittance matrix, as in traditional network theory, is written at each phase by applying KCL at every node. Residual charge on each capacitor results from the previous phase (or phases) is represented as a charge source connected in parallel with that capacitor. Two indefinite admittance matrices are constructed. Elements having frequency dependent impedances (capacitors and non-ideal amplifiers) are considered in the first matrix ($\mathbf{A}$), whereas the effects of switches represented by their resistances, real resistors, ideal operational amplifiers together with dependent and independent sources are considered in the three dimensional matrix ($\mathbf{B}$).

ii) A state space representation of the circuit is evaluated from its modified nodal admittance formulation. In this formulation state variables representing node voltages, operational amplifier output currents and the currents of dependent and independent sources are considered. Unfortunately, not all these are variables since states and the voltages across the capacitors are the only real state variables. Also, it is known that the values of the output currents of amplifiers and the currents passing through the voltage sources are not of importance. Dropping these variables and taking into consideration their effects is a great help in getting the state space representation from the modified nodal one.

iii) The time domain solution of the state equations is straightforward. The Runge-Kutta-Merson method is used to solve the resulting system of first order differential equations. Throughout this process, it is assumed that the sampling period is normalized to the unity. It contains N equal time slots, where N is the number of phases. Moreover, the analyzed circuit is assumed to be initially at rest $V(0) = 0$. So, to obtain the impulse response, let an impulse function be applied at node i in the first phase at the beginning of the first sampling period. Then, the output is sampled at the node j during the k-th phase.

iv) A fast Fourier transform approach (FFT) may be used to find the frequency response of the circuit from its time domain response. Since the time response is time varying, each phase period is divided into M equal time slots. The accuracy of the frequency response increases by increasing M. Also, during the time domain evaluations, the state values at the end of each time slot are considered as initial values of

the next one. If the non-idealities are not severe, the time response during each phase period is approximately constant. In this case M can be taken to be one and the method described in [12] can be used to find the frequency response from the impulse response.

Optimization Method for Compensation of Non-Idealities

The method is based on the minimization of deviations in the coefficients of both numerator and denominator of non-ideal circuit transfer function from the ideal ones. For this purpose let the rational transfer function of the ideal network to be written in the form:

$$H_i(z) = \frac{a_0 + a_1 z^{-1} + a_2 z^{-2} + \ldots + a_n z^{-n}}{1 + b_1 z^{-1} + b_2 z^{-2} + \ldots + b_n z^{-n}} . \tag{1}$$

The distorted transfer function may be expressed as:

$$H_i(z) = \frac{a_0^d + a_1^d z^{-1} + a_2^d z^{-2} + \ldots + a_m^d z^{-m}}{1 + b_1^d z^{-1} + b_2^d z^{-2} + \ldots + b_m^d z^{-m}} , \tag{2}$$

where d in the coefficients a_i^d and b_i^d, denotes the distortion due to the non-ideality in the elements and m is the degree of the transfer function of the non-ideal circuit before compensation; $m \geq n$. These coefficients are nonline functions of the capacitor values in the circuit, the switch resistances, the operational amplifier resistances and gain bandwidths. From the last two equations the following error functions can be defined.

$$\left.\begin{aligned} F_i(C_1, C_2, \ldots, C_N) &= \left(a_i^d - a_i\right); & i &= 0, 1, 2, \ldots, n \\ F_j(C_1, C_2, \ldots, C_N) &= \left(a_j^d\right)^2; & j &= n+1, n+2, \ldots, m \\ F_k(C_1, C_2, \ldots, C_N) &= \left(b_k^d - b_k\right); & k &= 1, 2, 3, \ldots, n \\ F_l(C_1, C_2, \ldots, C_N) &= \left(b_l^d\right)^2; & l &= n+1, n+2, \ldots, m \end{aligned}\right\} , \tag{3}$$

where C_i is the i-th capacitance in the circuit and N is the number of these capacitances. To decrease the effect of non-idealities, possibly eliminate these effects, the sum of the functions, F_i, F_j, F_k and F_l is minimized by using any minimization routine. Through the minimization process, the gradient is evaluated with respect to the capacitances of the switched-capacitor circuit. This is because these parameters are the only available parameters. The initial guesses of the capacitance values are taken to be that of the ideal circuit. An iterative procedure based on Newton–Raphson method has been used for solving the resulting non-linear equations [13].

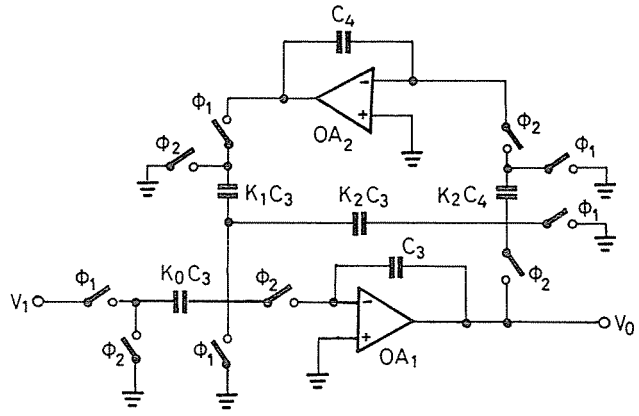

Fig. 5. Switched-capacitor realization of second order bandpass biquad

Illustrative Examples

To illustrate how the compensation approach can work properly, consider the following two examples:

Example 1: Consider the bandpass biquad of *Fig. 5.* In [14], it has been shown that its transfer function is given by:

$$H(z) = \frac{K_0 z^{-1}\left(1 - z^{-1}\right)}{(1 + K_3) + (K_1 K_2 - K_3 - 2)\, z^{-1} + z^{-2}}. \tag{4}$$

This circuit has been analyzed using the method given in [11]; with the following element values:

$$K_0 = 0.021\,, \qquad K_1 = K_2 = 0.5204\,, \qquad K_3 = 0.0217$$

and

$$C_3 = C_4 = 1.0\,.$$

Computer results show that the circuit with ideal elements has the rational transfer function given by:

$$H(z) = \frac{0.0255398\; z^{-1}\left(1 - z^{-1}\right)}{1.0 - 1.713697\; z^{-1} + 0.978761\; z^{-2}}.$$

For the case of switches having conductances $G = 5.0$, the rational transfer function of the circuit is given by:

$$H(z) = \frac{0.0178690\ z^{-1} - 0.019706\ z^{-2} + 0.001452\ z^{-3}}{1.0 - 1.991678\ z^{-1} + 1.190304\ z^{-2} - 0.093682\ z^{-3}}.$$

Applying the compensation technique, described before, the capacitance rations are changed to:

$$K_0 = 0.027525, \quad K_1 = 0.138454, \quad K_2 = 0.119856,$$
$$K_3 = 0.028978, \quad C_1 = 1.299903 \quad \text{and} \quad C_2 = 0.047732.$$

The circuit with the above capacitance ratios has the following transfer function which is very close to the ideal one.

$$H(z) = \frac{0.020530\ z^{-1} - 0.020533\ z^{-2}}{1.0 - 1.725431\ z^{-1} + 0.979031\ z^{-2} - 0.000018\ z^{-3}}.$$

Now, consider the case of ideal switches with operational amplifiers having gain-bandwidth product equal 4.0. In this case the operational amplifiers are modelled by their macro model [11]. It has been shown that the rational transfer function of the circuit is given by:

$$H(z) = \frac{0.018119\ z^{-1} - 0.018553\ z^{-2} + 0.000430\ z^{-3}}{1.0 - 1.876633 z^{-1} + 1.133952\ z^{-2} - 0,051538\ z^{-3} + 0.000556\ z^{-4}}.$$

Also the compensated circuit can be described by:

$$H(z) = \frac{0.021550\ z^{-1} - 0.021656\ z^{-2}}{1.0 - 1.733099\ z^{-1} + 0.987841\ z^{-2} - 0.000062\ z^{-3}}.$$

The capacitance ratios of the compensated network are given by:

$$K_0 = 0.024256, \quad K_1 = 0.490435, \quad K_2 = 0.630594,$$
$$K_3 = 0.026847, \quad C_1 = 1.044072 \quad \text{and} \quad C_2 = 0.778897.$$

Finally consider the combined effects of both switch on-resistances and finite gain-bandwidth products. The values of the switch conductances and the gain-bandwidth products of the amplifiers are assumed to be 5.0 and 4.0, respectively. The rational transfer function can be deduced to be:

$$H(z) = \frac{0.017754\ z^{-1} - 0.018203\ z^{-2} + 0.000372\ z^{-3}}{1.0 - 1.899650\ z^{-1} + 1.144747\ z^{-2} - 0.049981 z^{-3} + 0.000513\ z^{-4}}.$$

By applying the compensation technique to the circuit given is this case, the following capacitance ratios result:

$$K_0 = 0.018026, \quad K_1 = 0.289108, \quad K_2 = 0.595395,$$
$$K_3 = 0.105050, \quad C_1 = 0.675635 \quad \text{and} \quad C_2 = 0.593391.$$

The biquad rational transfer function is improved to be:

$$H(z) = \frac{0.020849\, z^{-1} - 0.021377\, z^{-2} + 0.000457\, z^{-3}}{1.0 - 1.757976\, z^{-1} + 1.055465\, z^{-2} - 0.044792 z^{-3} + 0.000460\, z^{-4}}.$$

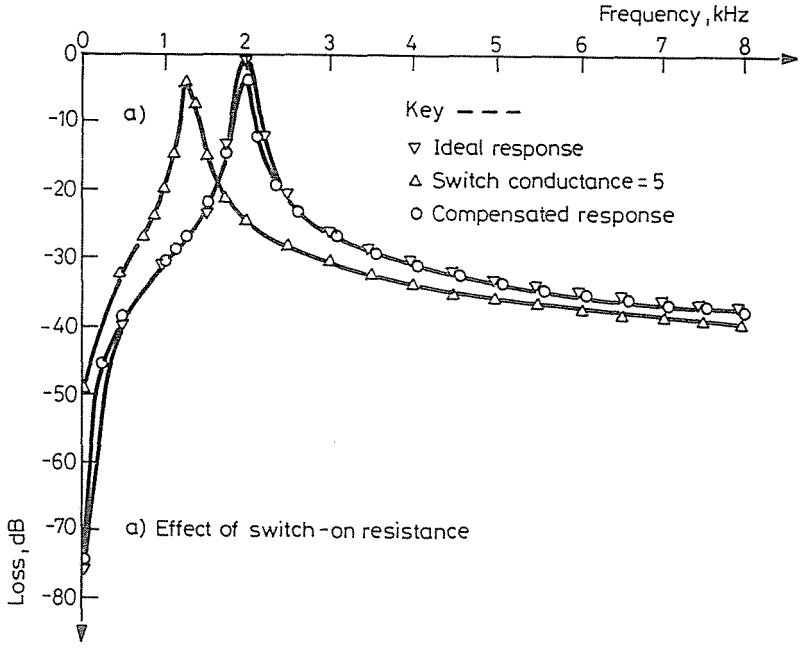

Fig. 6. Compensation of the effect of non- idealities of a second order bandpass biquad. a) Effect of finite switch on-resistance

Fig. 6 illustrates the frequency responses for the biquad for all of the cases described above.

Example 2: This example illustrates the compensation of non-idealities in circuits exhibiting a large number of switching intervals (phases). *Fig. 7* shows the circuit and the timing diagram of a third order Chebyshev low-pass filter. It is designed according to the IVIS principle [15]. From this figure, it is evident that the circuit has 11 nodes and operates with 12 phases. We will consider four different cases. These are the circuit with

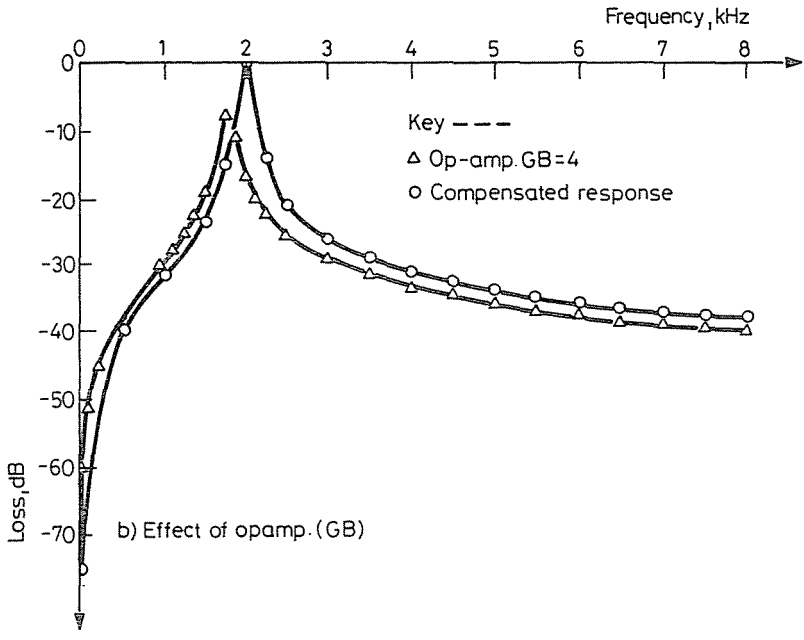

Fig. 6. Compensation of the effect of non-idealities of a second order bandpass biquad. b) Effect of finite op-amp gain bandwidth product

ideal elements, with ideal operational amplifiers and non-ideal switches ($G=250$), with ideal switches and amplifiers having finite gain-bandwidths product $GB=100$ and with non-ideal switches and amplifiers ($G=250$ and $GB=100$). In all of the cases, the output impulse response is sampled at the 6-th phase due to an impulse input applied at the first phase. The corresponding rational transfer functions are given in *Table 1*. *Table 2* illustrates the transfer functions for the non-ideal cases after applying the compensation technique. The element values for ideal and compensated circuits are given in *Table 3*. *Figs. 8* and *9* illustrate the responses before and after compensation.

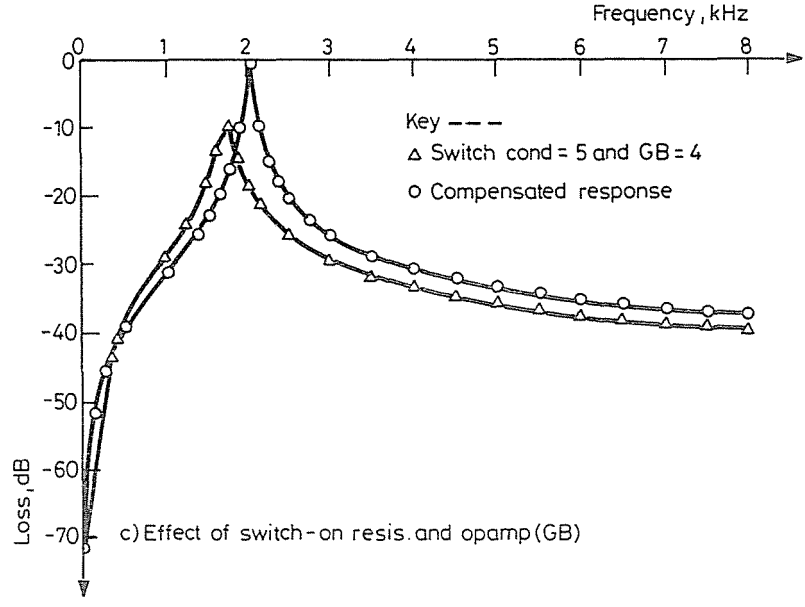

Fig. 6. Compensation of the effect of non-idealities of a second order bandpass biquad. c) Combined effect of both switch on-resistance and gain bandwidth product of the amplifiers

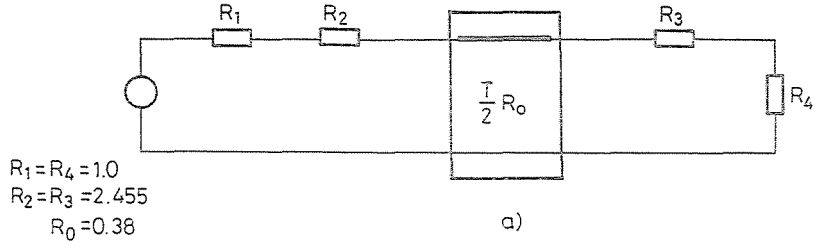

Fig. 7. a) Prototype circuit of a third order low-pass filter

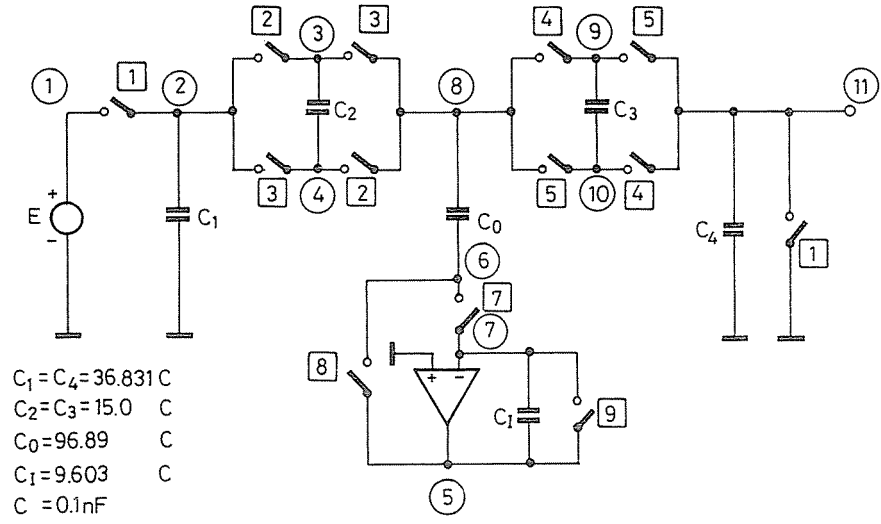

Fig. 7. b) SC circuit of a third order low-pass filter

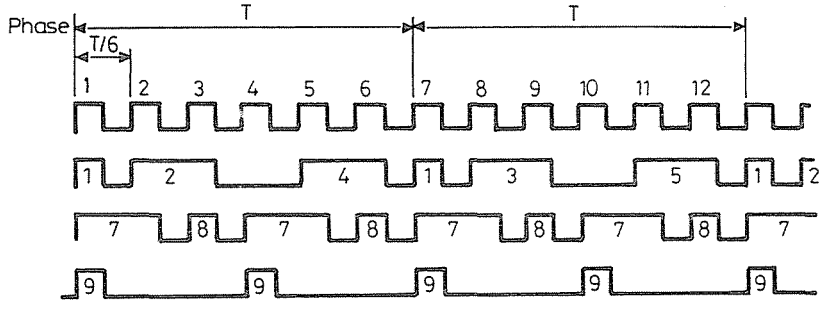

Fig. 7. c) Timing diagram

Table 1
Transfer functions of 3-rd order Chebyshev low-pass filter with ideal and non-ideal elements

1) *Ideal case*

$$H_0(z) = \frac{0.103354 + 0.206708\ z^{-1} + 0.103354\ z^{-2}}{1.0 - 1.203472\ z^{-1} + 0.845902\ z^{-2} - 0.228974\ z^{-3}}.$$

2) *Switches with conductances* $G = 250$

$$H_1(z) = \frac{0.102844 + 0.206192\ z^{-1} + 0.103855\ z^{-2} + 0.000508\ z^{-3} + 0.000002\ z^{-4}}{1.0 - 1.200292\ z^{-1} + 0.846017\ z^{-2} - 0.231900\ z^{-3} + 0.002204\ z^{-4}},$$

3) *Operational amplifiers with gain-bandwidths* $GB = 100$

$$H_2(z) = \frac{0.102133 + 0.204267\ z^{-1} + 0.102134\ z^{-2} + 0.000001\ z^{-3}}{1.0 - 1.190195\ z^{-1} + 0.828777\ z^{-2} - 0.220673\ z^{-3}},$$

4) *Switches with conductances* $G = 250$ *and amplifiers with* $GB = 100$

$$H_3(z) = \frac{0.099317 + 0.199133\ z^{-1} + 0.100317\ z^{-2} + 0.000503\ z^{-3} + 0.000002\ z^{-4}}{1.0 - 1.161525\ z^{-1} + 0.796160\ z^{-2} - 0.207968\ z^{-3} + 0.002013\ z^{-4}},$$

Table 2
Transfer functions of 3-rd order Chebyshev low-pass filter with non-ideal elements after applying the compensation technique

2) *Switches with conductances* $G = 250$

$$H_1^c(z) = \frac{0.103313 + 0.206626\ z^{-1} = 0.103307\ z^{-2}}{1.0 - 1.203682\ z^{-1} + 0.846119\ z^{-2} - 0.229010\ z^{-3}},$$

3) *Operational amplifiers with gain-bandwidths* $GB = 100$

$$H_2^c(z) = \frac{0.103306 + 0.206612\ z^{-1} + 0.103307\ z^{-2}}{1.0 - 1.202978\ z^{-1} + 0.845306\ z^{-2} - 0.228691\ z^{-3}},$$

4) *Switches with conductances* $G = 250$ *and amplifiers with* $GB = 100$

$$H_3^c(z) = \frac{0.103039 + 0.206095\ z^{-1} + 0.103073\ z^{-2} + 0.000017\ z^{-3}}{1.0 - 1.204604\ z^{-1} + 0.847133\ z^{-2} - 0.229969\ z^{-3} + 0.000266\ z^{-4}},$$

Table 3
Element values of 3-rd order Chebyshev low-pass filter under ideal and compensated conditions

Element (nF)	Ideal case	$G = 250$	$GB = 100$	$G = 250$ and $GB = 100$
C_1	3.683100	1.253080	2.551961	1.370637
C_2	1.500000	2.545782	0.672606	0.506171
C_3	1.500000	0.252804	0.802784	5.300025
C_4	3.683100	1.187345	1.827576	2.392658
C_0	9.689000	8.601220	4.685976	17.845432
C_I	0.960300	0.268135	0.522532	0.363851

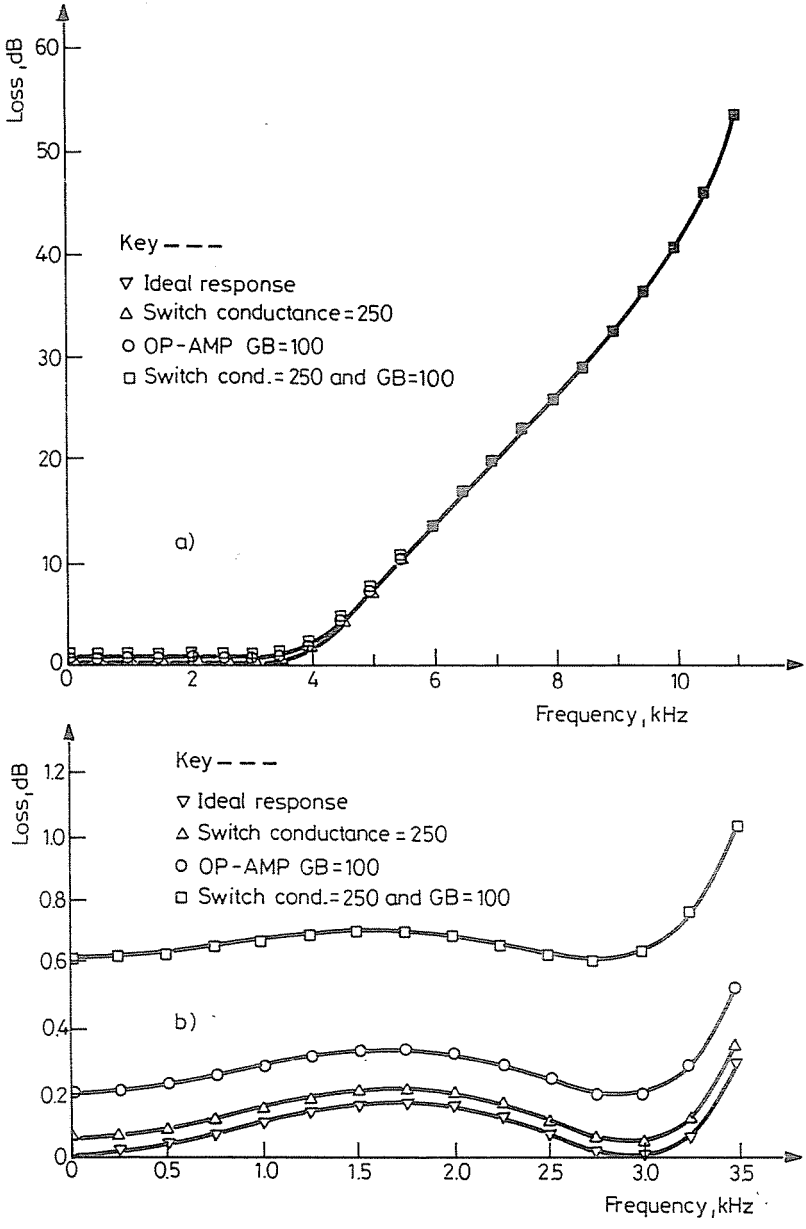

Fig. 8. Effect of switch on-resistance and op-amp gain bandwidth
a) Frequency response of 3rd order low-pass filter
b) Expanded passband loss

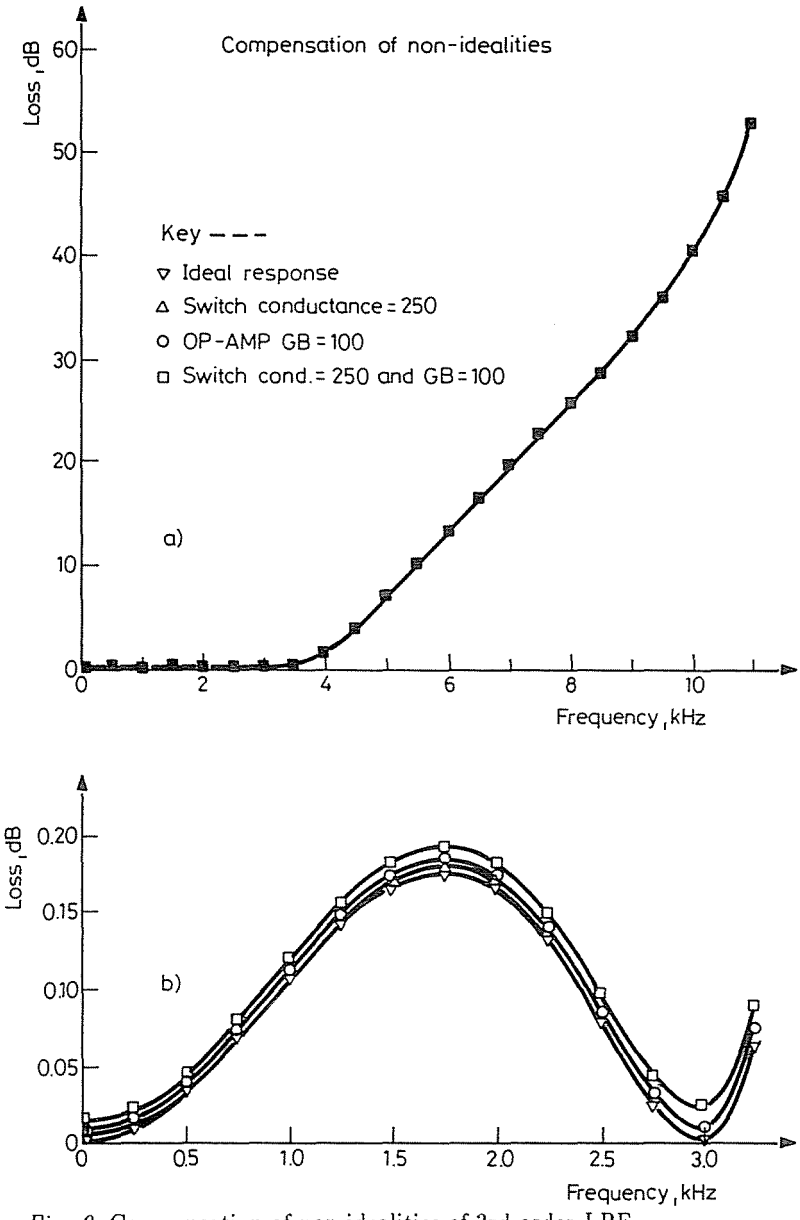

Fig. 9. Compensation of non-idealities of 3rd order LPF
a) Frequency response
b) Expanded passband loss

Conclusion

Two design techniques are described for decreasing and possibly eliminating the effects of element imperfections in switched-capacitor circuits. In the first technique the operational amplifier non-idealities are considered. Computer simulation shows that decreasing the number of amplifiers by multiplexing their use leads to circuits with better performances and operating at higher frequencies. The second approach is based on the minimization of the sum of the square of the differences between the time (or the frequency) response of the circuit with and without non-idealities. This technique can be used to control over the effects of finite switch resistances, finite gain-bandwidth product of the amplifiers as well as parasitic capacitances. Computer results have revealed that the responses of the optimized circuits are nearly the same as that of the ideal ones.

Acknowledgements

The author is grateful to Professor M.F.Fahmy of the University of Assiut, Assiut, Egypt, and Dr.T.Henk of the Department of Telecommunications and Telematics, Technical University of Budapest, Hungary, for their interests in the subject of the paper.

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