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POWER LINES AS LOCAL AREA NETWORKS FOR MEASURING AND CONTROL SIGNAL TRANSMISSION

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Abstract

Electrical power distribution networks represent the most attractive medium for digital communication purposes due to an ever increasing demand for environmental management of buildings, security monitoring, office automation or remote control of customer appliances and remote meter reading. Power lines are, however, heavily stressed with interference from various sources. Both interference and attenuation are time-variant and frequency-selective in an arbitrary way. The prospective user has to overcome the impairments with a severely restricted level of transmission power, e.g. 5 mW in Germany; the transmission bandwidth, however, exceeds 100 kHz. Obviously simple and inexpensive modulation schemes for digital data transmission such as amplitude shift keying (ASK) or frequency shift keying (FSK) are ruled out. A significant success of band-spreading techniques has been demonstrated by several field trials and extended measurements at different power line networks.

Application of spread spectrum techniques generally involves high effort; this is especially true for frequency hopping, which proved advantageous in practical applications. Exploiting the possibilities of modern microelectronics, including design and production of ASICs, recently led to a break-through. A five-year research project based on frequency hopping spread spectrum signaling opened up power lines as local area networks e.g. for office automation or remote meter reading. Transmitter and receiver prototypes were constructed for evaluation of the proposed ideas at various power line networks. Transmitters are based on standard microcontrollers, whereas an application specific integrated circuit (ASIC) with a complexity of about 5000 gates is the heart of the receiver. Due to completely digital signal processing, the prototypes are useful as a base for series production.

Keywords: power line communications, frequency hopping.

Introduction

Modern dwelling houses as well as office and factory buildings are equipped with numerous sensors and measuring instruments, e.g. for temperature, humidity or consumption of electrical energy, water or gas. Various control and supervision tasks can be performed automatically, e.g. by centrally lo-

cated personal computers, if appropriate physical links are accessible. Electrical power distribution circuits represent a reasonably universal network for communication purposes. Analyzing power lines as data channels with information theory reveals that there is a considerable amount of channel capacity; however, exploitation is not easy due to extreme time-variance of the channel properties. Obviously conventional and inexpensive modulation schemes for digital data transmission such as amplitude shift keying (ASK) or frequency shift keying (FSK) are not applicable. This statement has been confirmed by numerous scientists and research groups involved in power line communications [3, 5, 13, 14, 16, 17]. Experimental and theoretical approaches led to the following conclusion: The restrictions of transmission power call for full exploitation of the spectral resources. Information must be distributed as widely as possible within the available transmission bandwidth, in order to lower the vulnerability against unpredictable variations of attenuation and interference. A significant success of spread spectrum techniques has been demonstrated by several field trials and extended measurements at different power line networks [3, 5, 14, 17]. Obviously severe attenuation effects and sudden occurrence of heavy interference are typically restricted to relatively narrow portions of the transmission band [2, 11, 12, 16]. When the transmission band is only partially affected by hostile channel behaviour, spread spectrum techniques are well-kown as effective instruments to provide reliable communications [4, 5, 13]. A variety of spread spectrum techniques is known, preferably from the field of wireless communications. When dealing with power line networks, selecting and developing an appropriate and cost-effective spread spectrum signaling scheme is not easy, as information must be widely distributed into each section of the transmission band. On the other hand, the transmitted spectrum should not be contiguous, as frequency-selective interference and attenuation normally affect considerable portions of bandwidth. Spectral gaps of several kilohertz proved to be advantageous in practice [13, 14, 16, 17].

Power Line Channel Properties

The layout of electric power distribution networks never involved communication aspects. As a result the transmission properties severely complicate their use as data links. Furthermore, bandwidth as well as transmission power are restricted. According to the rules of the Deutsche Bundespost [1, 6] a frequency range from 30 kHz to 146 kHz is allowed for communication purposes, with the transmitted power generally limited to 5 mW — which corresponds to a transmission voltage $V_s \approx 0.35 V_{rms}$ — for in-

door use. Exceptions include industrial power line networks with their own transformers, where the power limit is 150 mW. No general rules for outdoor systems do exist at this time but new European regulations are under way [7].

Attenuation in power line networks significantly depends on network load and is partially selective exhibiting extreme variance with time [2]. *Fig. 1* shows some characteristic indoor and outdoor records of attenuation. Trace 1 represents the unattenuated transmission signal with $V_s = 0.35V_{rms}$. Trace 2 is recorded in a one-family house. The mean attenuation is about 15 dB. From trace 3 the typical attenuation along a 1 km electric power cable supplying 40 buildings in an urban dwelling environment can be seen. Attenuation is considerably higher, compared with indoor power lines and exhibits a mean value of about 50 dB. Due to the low transmission voltage of only $0.35V_{rms}$, interference partially exceeds the transmission signal.

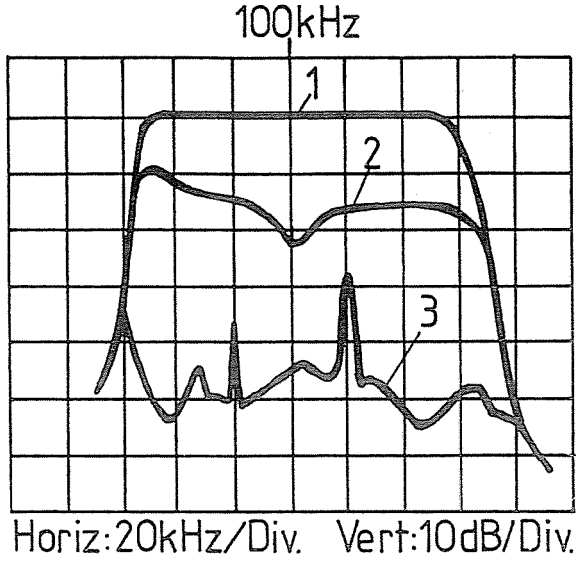

Fig. 1. Attenuation measured at power line networks
Trace 1: transmission signal $V_s = 0.35V_{rms}$.
Trace 2: record in a one-family house
Trace 3: record at a 1 km power cable

Generally, electric power distribution networks are heavily stressed with time-variant interference from various sources. Interference power density e.g. in one-family houses significantly differs from the levels in factories or laboratory buildings. In *Fig. 2* two characteristic spectra are recorded. Trace 1 corresponds to the transmission voltage $0.35V_{rms}$ for

comparison. Trace 2 shows a typical interference spectrum to be found in one-family houses in a rural environment. Compared with trace 1 we have a signal to interference ratio of about 50 dB, so obviously no problems are expected.

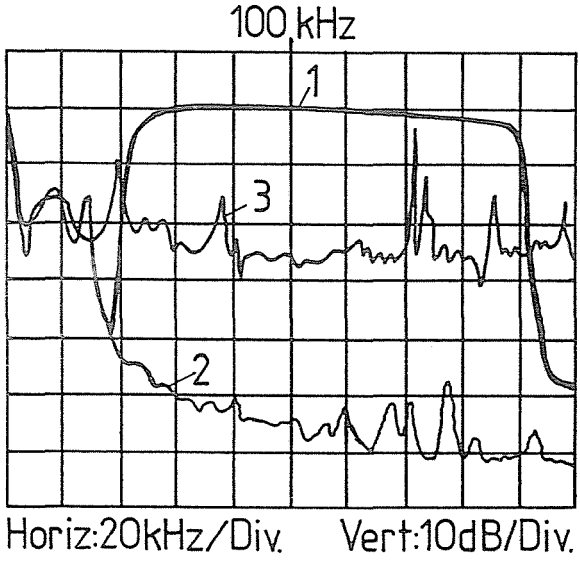

Fig. 2. Interference spectra recorded at indoor power lines
Trace 1: transmission signal $V_s = 0.35V_{rms}$.
Trace 2: record in a one-family house
Trace 3: record in a factory building

A quite different situation, however, is documented by trace 3, which was recorded in a factory building. The signal to interference ratio is below 20 dB now, and severe detection problems may occur, if the transmitted signal is attenuated more than 10 dB.

Fig. 3 shows typical conditions which are found at the receiver input in the above mentioned factory building. Trace 1 represents the attenuated transmission signal recorded during an idle time of the factory machinery, and trace 2 is the interference spectrum from *Fig. 2*, recorded with a spectrum analyzer filter bandwidth of 1 kHz. The mean signal to noise ratio is approximately 10 dB with variations of about ±2 dB.

In *Fig. 4* the typical conditions found at a receiver for remote meter reading are recorded. Trace 1 which corresponds to trace 3 in *Fig. 1* represents the received signal spectrum — plus interference of course which cannot be switched off here. Trace 2 represents the pure interference spectrum, and is only slightly below trace 1. In this case the signal to noise

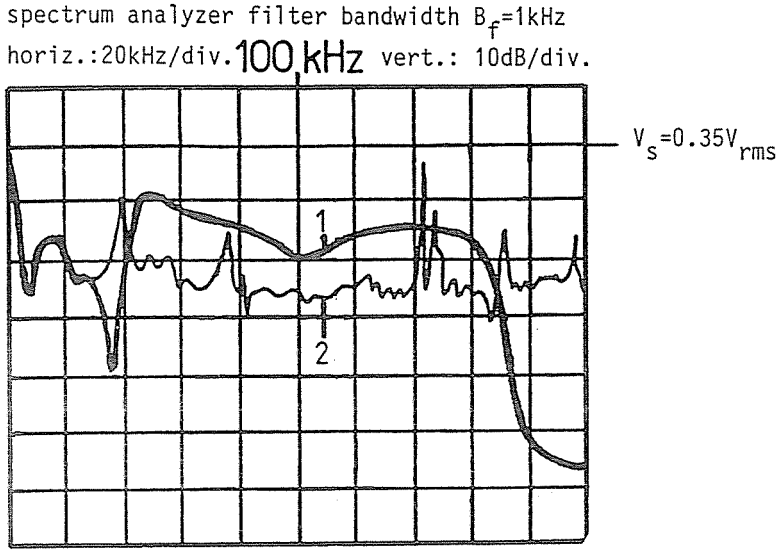

Fig. 3. Spectra recorded in a factory building
Trace 1: attenuated transmission signal
Trace 2: Interference spectrum

ratio is close to 0 dB. For 0 dB, trace 1 would have to run approximately 3 dB above trace 2. Bit error probability simulations which will be discussed later in this paper are based on *Fig. 4*, with a signal to noise ratio of 0 dB and variations of ±2 dB.

Figs. 1–4 impressively demonstrate that power lines generally represent a rather hostile medium for data transmission purposes, and that narrowband modulation techniques will normally fail, or at least cannot provide reliable data links.

Choice of a Spread Spectrum Modulation Scheme

In spread spectrum systems receiver synchronization is generally a major factor of cost. To open up power lines as local area networks, a low-cost approach is paramount. A low-cost solution of the synchronization problem calls for global synchronization based on the power line voltage as reference [3, 9, 10, 14, 16, 17]. This approach significantly influences the selection of an appropriate spread spectrum modulation scheme. Pseudonoise phase hopping for example is ruled out by the fact that limited precision of synchronization restricts the bandwidth which can be exploited to less than one third of the available spectrum [3, 17]. Global synchronization based

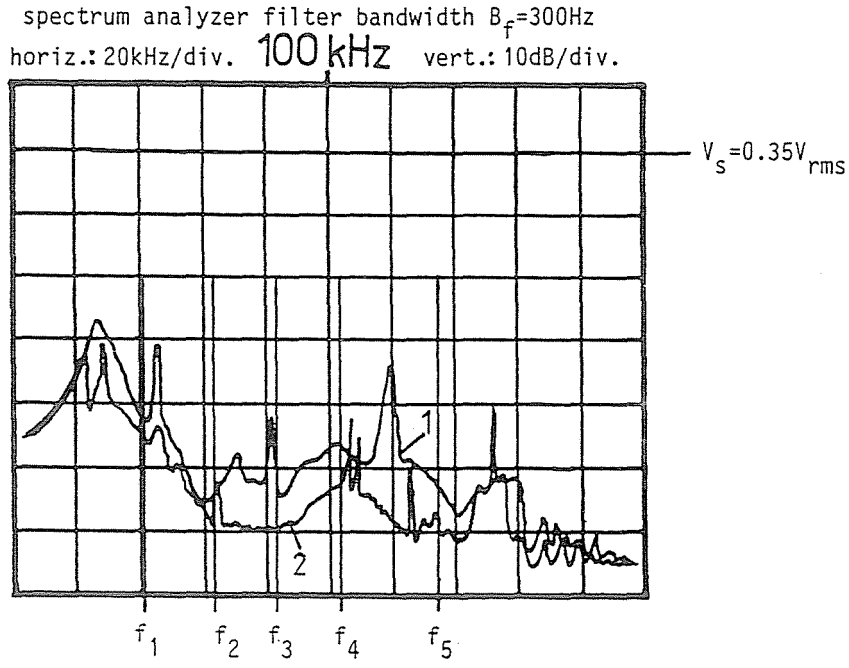

Fig. 4. Spectra recorded at a power cable of 1 km
Trace 1: received signal plus interference
Trace 2: interference alone

on the power line voltage suffers from jitter, delay effects and unwanted phase shifts, e.g. in three-phase power supply systems, which are typical for Europe.

Considering frequency hopping opens an interesting way to maintain the proposed low-cost synchronization scheme, and at the same time to provide the necessary spreading of information. For digital data transmission with frequency hopping, a data bit of the duration T_B is typically distributed to an odd number n of carriers with different frequencies $f_1 \ldots f_n$ [9]. Each carrier is transmitted in a time interval $T_c = T_B/n$ (also named chip in the following). In practice, $n = 5$ turned out to be a good choice. HIGH and LOW bits are assigned to different sets of frequencies. The hop rate h equals the reciprocal value of T_c. It is not useful to choose n even; a proof for this statement can be found in [10]. The bandwidth occupied by a chip is $\sin(x)/x$-shaped around each transmitted frequency f_i, with the zeroes of the main lobe located at $f_i \pm h$. Spacing the frequencies at intervals Δf according to the hop rate h leads to orthogonality, and yields maximum spectral efficiency, which is illustrated in *Fig. 5a*. Receivers equipped with matched filters are able to separate the transmitted

waveforms perfectly, as long as synchronization is perfect and no collisions occur. Global synchronization and proper frequency allocation can prevent collisions. Synchronization reference accuracy, however, limits the degree of spectrum exploitation due to loss of orthogonality [9].

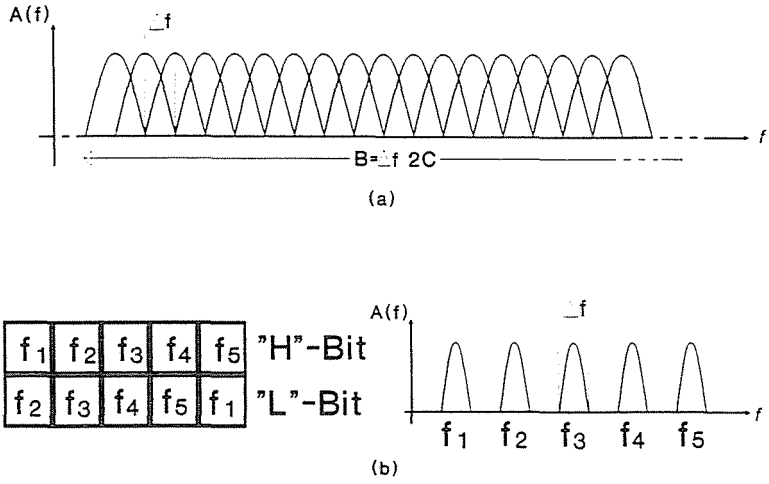

Fig. 5. a) Spectrum exploitation with orthogonal waveforms (shematically)
b) Example of one channel with 5 frequencies per bit

Aspects of Global Synchronization

The power line network provides a voltage with relatively high stability of frequency and moderate corruption by interference. The zero-crossings of the power line voltage represent basic synchronization reference instants. Most power line networks, however, incorporate a three-phase operation with a 120-degree phase shift between the phases. So ambiguities arise which have to be eliminated. This may be done e.g. by an inexpensive microcontroller, which — by means of an internal timer — divides each interval between two zero-crossings into three parts of equal duration. Assigning a chip with a duration T_c to each of these parts leads to an advantageous solution which was successfully evaluated in practice. The frequency hop rate $h = 1/T_c$ is fixed to six times the power line frequency, i.e. $h = 300\ s^{-1}$ for 50 Hz. Including n carriers per data bit, a timing scheme according to

Fig. 6 results. For $n = 5$, we have the data rate $r_d = 60$ bits/s. For a transmission bandwidth B the maximum number C of possible transmission channels requiring $N = 2Cn$ distinct frequencies can be calculated now:

$$C = \mathrm{INT}\{\frac{B}{2 \cdot h}\}. \tag{1}$$

With $B = 116$ kHz, $h = 300\ \mathrm{s}^{-1}$ and $n = 5$, $C = 38$ channels can simultaneously be operated collision-free, involving $N = 386$ frequencies. *Fig. 5b* illustrates the typical frequency allocation of one channel as an example.

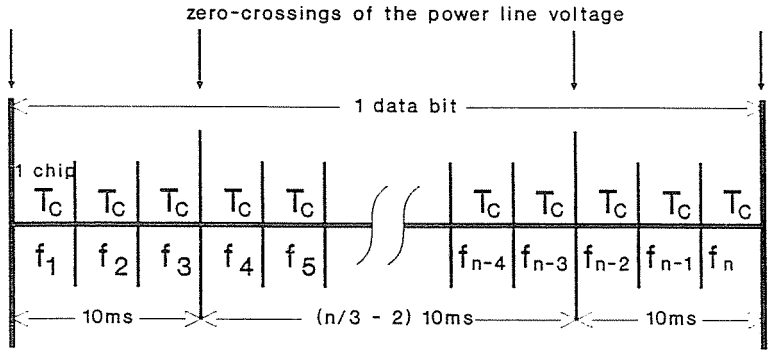

Fig. 6. Timing scheme based on the power line voltage as reference

A closer look at (1) reveals the flexibility to achieve trade-offs between number of channels C, data rate $r_d = h/n$, and interference immunity represented by n — the number of frequencies per bit. Increasing n at a fixed data rate r_d will raise the hop rate h, which will lead to a lower number of channels C, as channel spacing grows.

Some basic attempts for synchronization error analysis in mainsborne frequency hopping multiple access systems are made in [9]. Here the impact of synchronization errors will be considered for single user systems only. In this case a loss of signal power S at the receiver matched filter output due to the synchronization error τ must be taken into account. With [9] we have

$$S = T_c^2 \left[1 - \frac{\tau}{T_c}\right]^2. \tag{2}$$

Measurements of the synchronization error at indoor three-phase power line networks revealed a worst case mean value of 35 μs and a standard deviation

of 25 μs. The relatively high mean value results from unsymmetrical load in three-phase networks. In extended networks propagation delay must be additionally considered. With signal and energy flow being opposite, we have a delay of about 12 μs/km for a typical power supply cable. With $T_c = 3.33$ ms a worst case signal power loss of only 0.19 dB over 1 km arises due to synchronization errors. This result is obtained by setting $\tau = (35 + 25 + 12)\mu s = 72$ μs in (2), i.e. the sum of all errors mentioned above.

The frequency hopping spread spectrum signaling is obviously an effective means for bandwidth exploitation with very moderate requirements concerning precision of synchronization.

The Frequency Hopping Signaling Scheme

Spread spectrum systems can be designed to be insensitive to selective attenuation and to provide resistance against various kinds of jammers or interference [4]. Additionally multiple access and selective calling features become available. To apply spread spectrum techniques for digital data transmission over power line networks the following tasks must be performed:

- global synchronization based on the power line voltage,
- effective exploitation of bandwith,
- precise and cost-effective generation of a sufficient number N of orthogonal spread spectrum waveforms,
- matched filter reception of the desired wave-forms.

The solution outlined in the following is based on frequency hopping and exhibits the essential features listed below:

- effective use of bandwidth (wide spreading of information),
- high tolerance to synchronization reference jitter and delay effects,
- capability to achieve collision-free multiple access based on global synchronization and proper frequency allocation.

Disadvantages of frequency hopping compared e.g. with phase hopping systems include higher effort for waveform generation and receiver matched filtering [3, 4, 17]. P.K. van der Gracht and R.W. Donaldson [3], and J.O. Onunga and R.W. Donaldson [8] have published some interesting work on pseudonoise phase hopping spread spectrum modulation for indoor applications, which led to remarkable results at minimum costs. The proposed modems rely on a relatively high transmitted power of 1W and occupy on the other hand only 1/3 of the available bandwidth. Due to the mentioned transmission power restrictions [1, 6], application of such modems in Germany and most other European countries would not be permitted.

An essential drawback of phase hopping as proposed in [3] is that the resulting spectrum is continuous. So a high chip rate is required to cover an extended bandwidth. However, distributing the information over an extended spectral range is of special interest. A continuous transmission spectrum is normally unwanted — see e.g. *Figs. 1–4*. Such requirements cannot be satisfactorily met by phase hopping due to the lack of synchronization reference accuracy. So the work reported here concentrates on frequency hopping spread spectrum signaling.

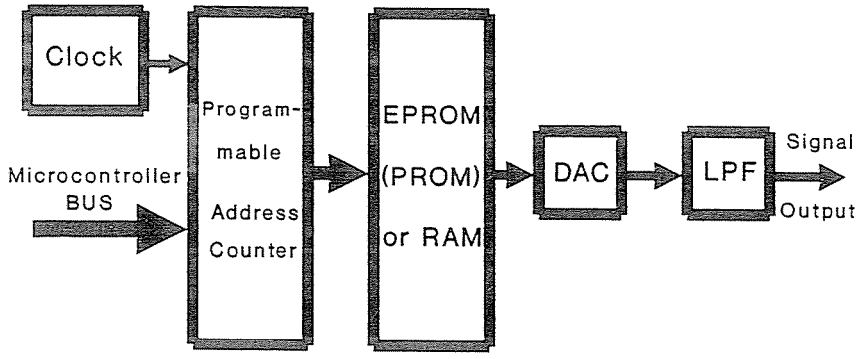

Fig. 7. Digital frequency synthesizer block diagram

Waveform Synthesis

When in a frequency hopping spread spectrum system with the hop rate $h = 300\ s^{-1}$ a bandwidth $B = 116$ kHz has to be completely covered, 386 distinct frequencies have to be precisely generated and must be rapidly changeable. These requirements practically rule out all kinds of analog signal generation. A new approach led to the development of microprocessor-controlled digital frequency synthesizers. The block diagram in *Fig. 7* illustrates the principle: Appropriate samples stored in a read-only-memory are clocked out by a fixed quartz-controlled clock and are fed to a digital to analog converter (DAC). Then, after low-pass filtering (LPF), the desired analog signal is present. Frequency precision solely depends on the quality of the embedded quartz crystal. Frequency hopping is performed by changing the memory read address space, i.e. programming the address counter appropriately via a microcontroller bus. The specified address

space is repetitively read, as long as the selected frequency is needed. In practice an eight-bit resolution of samples proved to be sufficient. A major problem in designing a synthesizer according to *Fig. 7* is to minimize the number of samples which have to be stored. A practical solution of this problem is outlined in [13]: A Turbo Pascal program was written, which, after entering the number N of desired frequencies, the hop rate h, and a range for the starting frequency f_0, performs an optimization procedure. After defining the desired frequencies and the number of samples required for each of them, the program calculates the sample values as 8 bit hexadecimal numbers (two's complement if wanted) and stores them into a file using Intel Hex Format for easy PROM or EPROM programming.

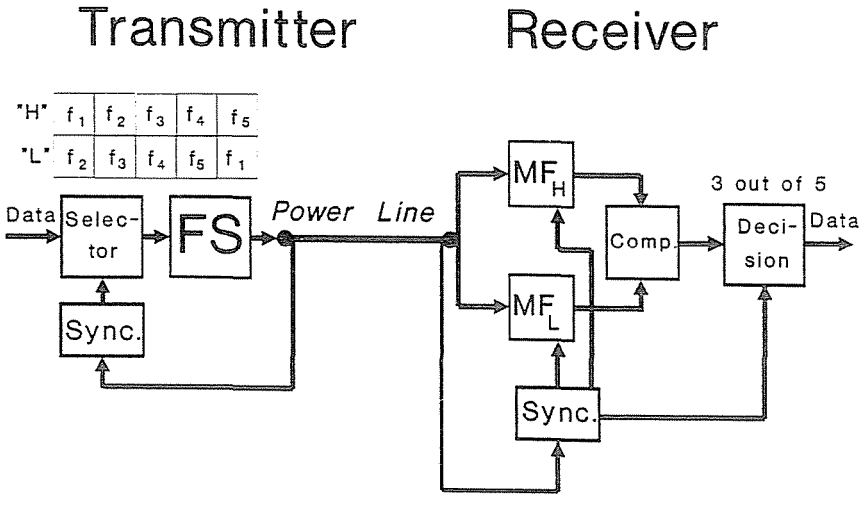

Fig. 8. Block diagram of a frequency hopping spread spectrum system

Receiver Signal Processing

A typical FH spread spectrum system as previously outlined is shown in *Fig. 8* as a base for the following considerations. The transmitter section needs no further discussion. At the receiver, two matched filters MF_H for the HIGH, and MF_L for the LOW bit branch are implemented. A receiver cannot immediately detect the beginning of a data bit; a preamble [13, 14,

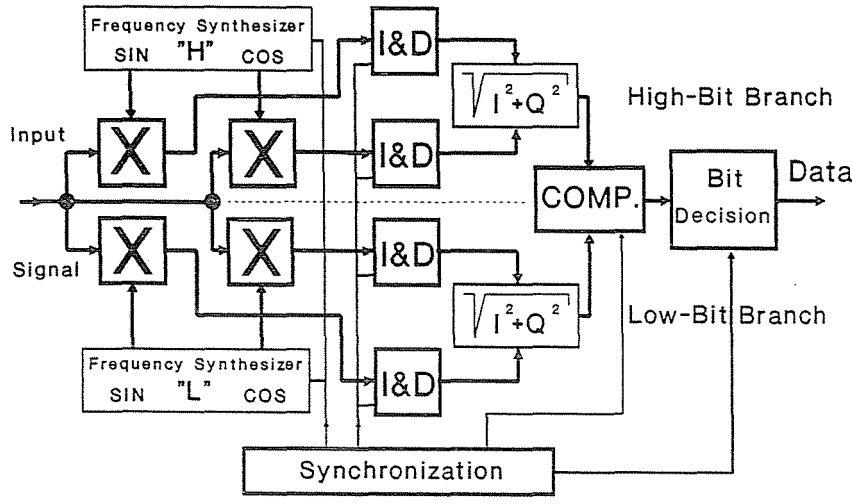

Fig. 9. Incoherent analog FH receiver principle

16] has to be transmitted for bit synchronization before the data stream starts.

After each reception of a chip (with the duration $T_c = 1/h$) a comparator decides whether the chip belonged to a HIGH or to a LOW data bit. The 'bit decision' block puts out the data bit for which at least three of five chips were detected. Due to incoherence matched filter construction causes some additional efforts. *Fig. 9* illustrates the principle: The received signal is fed to an inphase and a quadrature channel in HIGH and LOW bit branch, respectively. After the mixing procedure the mixer output signals are integrated for the duration T_c of a chip; at the beginning of each chip interval the integrators are dumped. These tasks are performed by the integrate & dump (I & D) circuits in *Fig. 9*. At the end of each chip interval inphase and quadrature I & D output signals of each bit branch are geometrically combined and compared. The comparison results are accumulated for bit decision.

Realizing the outlined receiver using e.g. analog mixers and integrate & dump circuits turned out to be uneconomic and inadequate for series production. A completely digital solution based on an application specific integrated circuit (ASIC) led to very promising results.

In *Fig. 10* the digital receiver concept is outlined: The received signal is sampled at time instants $k \cdot T_s$ (with $f_s = 1/T_s$ being the sampling frequency) and converted from analog to digital. Then each digitized sam-

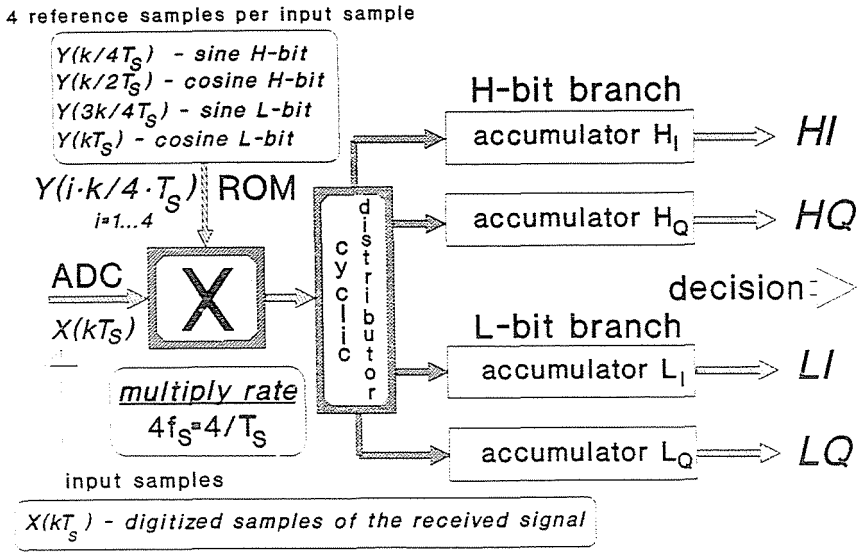

Fig. 10. Basic functions of a digital FH receiver matched filter

ple $X(kT_s)$ is consecutively multiplied with four digital reference values $Y(ik/4T_s)$ from the synthesizer ROM. These four values represent samples of sine and cosine waveforms corresponding to the desired HIGH- and LOW-bit frequencies. The cyclic distributor distributes the multiplication results correctly to the four accumulators (H_I corresponds to the accumulator HIGH bit inphase ... L_Q corresponds to the accumulator LOW bit quadrature), where they are summed up during one chip interval T_c. At the end of each chip the accumulator contents are latched and the accumulators are cleared for a new interval. Meanwhile the contents of the latches for the HIGH-bit and the LOW-bit branch are geometrically added. The two results are compared digitally and the comparator decisions are stored. After reception of n chips the final decision for that data bit (HIGH or LOW) is made, for which a majority — at least INT $\{n/2\} + 1$ — of the corresponding n waveforms were detected.

Implementation of the Receiver Functions into an ASIC

The essential task to be performed by digital circuitry to provide the functions outlined in *Fig. 10* can be described by the following formula [15]:

$$S_n = XY + S_0, \tag{3}$$

where S_0 denotes the accumulated sum, X and Y are the digitized samples of received signal and reference. S_n represents the new updated sum after an accumulation step. X and Y are represented as two's complement signed integers. S_0 and S_n include 28 bits. For fast parallel multiplication various concepts and algorithms are known. It is of special interest to involve the accumulation — that is addition or subtraction of a multiplication result $(X \cdot Y)$ to or from the contents of the selected accumulator — into the final steps of multiplication. Digital hardware should be designed to perform a task corresponding to the following algorithm: For a selected accumulator we get the new contents S_n represented by the 28 bits $s_{n0} \ldots s_{n27}$ (index 0 denotes the LSB) by adding the product $X \cdot Y$ to the old accumulator contents S_o.X is represented by the 8 bits $x_0 \ldots x_7$, Y by the 8 bits $y_0 \ldots y_7$ and S_o by the 28 bits $s_{o0} \ldots s_{o27}$. Finally we have:

$$\begin{aligned} S_n = &-2^{27} + \sum_{i=15}^{26} 2^i + x_7 y_7 \cdot 2^{14} + \sum_{i=0}^{6} \cdot \sum_{j=0}^{6} x_i y_j \cdot 2^{i+j} \\ &+ 2^8 + \sum_{i=0}^{6} x_7 y_i \cdot 2^{7+i} + \sum_{i=0}^{6} x_7 y_i \cdot 2^{7+i} \\ &- s_{o27} \cdot 2^{27} + \sum_{i=0}^{26} s_{oi} \cdot 2^i. \end{aligned} \tag{4}$$

Eq. (4) can be written in form of a matrix. This matrix has to be reduced step by step, e.g. by means of carry-save-adder arrays, carry look ahead adders and ripple carry adders [15, 17]. A block diagram of the hardware realization is given in *Fig. 11*. It is interesting to note that the hardware which executes (4) is distributed between four 'pipelining' registers in *Fig. 11*. The structure of the circuit in *Fig. 11* is sometimes called systolic, because a result must propagate through several distributed parts of hardware and is only complete after reaching the rightmost register. An ASIC according to *Fig. 11* was fabricated in May 1991 in form of a CMOS gate array. The ASIC was produced at LASARRAY Company Biel/Switzerland by laser direct writing on an XLD5000 wafer based on a 1.5 μm CMOS process. 4031 of 5000 available equivalent gates were used. Testing revealed a maximum clock frequency of 25 MHz.

Digital half-duplex modems for measuring and control signal transmission over power lines were builtd according to the block diagram in *Fig. 12*. Besides the described ASIC an inexpensive standard microcontroller (INTEL 80C31) and an 8 bit analog to digital converter are the main parts of the modem. Furthermore, a coupling transformer and an automatic gain control (AGC) amplifier are needed in the signal paths to

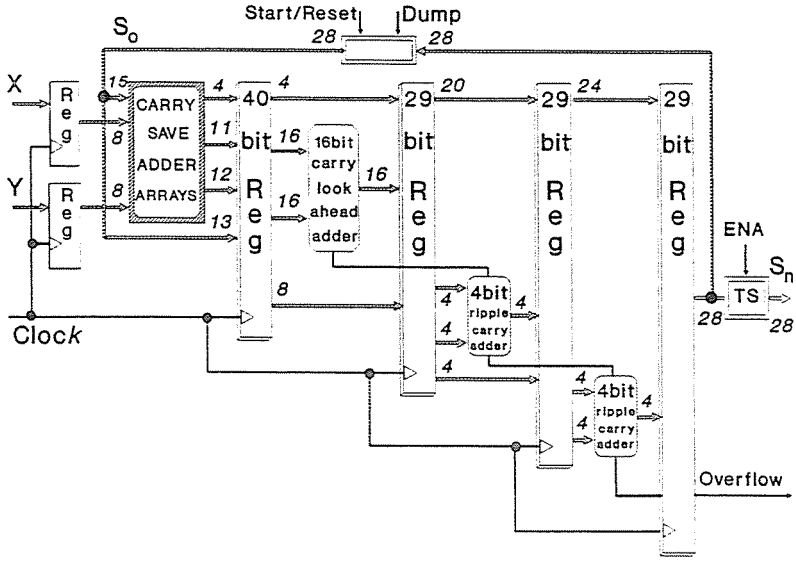

Fig. 11. Realized 'systolic' processor as FH matched filter (CMOS gate array)

the power supply network. A zero-detector (ZD) feeds the synchronization reference instants to the microcontroller. An EPROM addressed by a counter is the heart of the frequency synthesizer which is used in receive mode as well as in transmit mode. Special components for transmit mode incorporate an 8 bit digital to analog converter (D/A), a low-pass filter (LPF) and a power amplifier stage. All other transmitter functions are provided by the microcontroller and the frequency synthesizer block.

Bit Error Probability Considerations

Simplifying an FH spread spectrum system finally leads to frequency shift keying (FSK), where a fixed frequency is assigned to HIGH and LOW bit, respectively. For incoherent reception and corruption of the desired signal by white Gaussian noise with the spectral power density No, the bit error probability is given by:

$$P_e = \frac{1}{2} \cdot e^{\frac{E}{2N_0}}, \tag{5}$$

where E represents the useful signal energy, when a matched filter is implemented. Examining real world conditions present at power lines — as shown in *Figs. 3* and *4* — reveals that noise is far away from being white. Signal as well as noise levels exhibit considerable frequency and time depen-

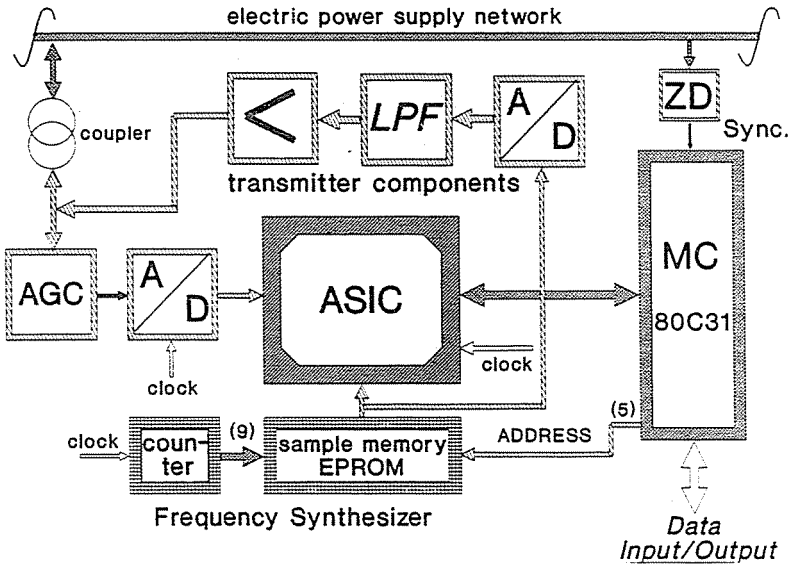

Fig. 12. FH modem prototype with ASIC and microcontroller

dent variations. Significant work examining noise on intrabuilding power line networks is described in [11] and [12] by CHAN and DONALDSON, and VINES et al., respectively. [11] provides an insight into impulse noise statistics of both industrial and residential building power lines within the spectrum of interest. [12] examines the noise spectra generated by a variety of appliances on residential power distribution circuits in a frequency range from 5 to 100 kHz. Besides impulse noise and different kinds of periodic noise there is a background noise which is typically Gaussian. This is due to the fact that noise on power lines stems from a variety of different sources which are statistically independent. Whiteness of that noise can be approximatively assumed locally in a narrow frequency range, e.g. around a transmitted frequency in case of frequency hopping waveforms. From [11] it can be seen, that the typical width of noise impulses is in the range from 1 to 120 μs. This is about 1/30 of a chip duration when worst situations are considered. Interval time between noise impulses is typically in the range of several milliseconds for impulses of high amplitude. So the probability that a waveform is hit by noise impulses twice or even more frequently is low.

For the following considerations five transmitted frequencies $f_1 \ldots f_5$ are marked in *Fig. 4*. As already outlined, the signal to noise ratio (SNR) is 0 ± 2 dB for a transmission voltage of $V_s = 0.35 V_{rms}$; this level is marked in *Fig. 4*.

At a matched filter output the signal to noise ratio — i.e. E/N_0 — at the sampling instant is given by the input SNR multiplied with the time-bandwidth-product $T_c \cdot B_f$ [4], provided that the input noise is white and Gaussian at least within the bandwidth $B_f \cdot T_c = 3.3$ms is the chip duration of the FH spread spectrum waveforms. $B_f = 300$ Hz represents the spectrum analyzer filter bandwidth for recording the noise trace; so $T_c \cdot B_f \approx 1$. As a result a 'chip error probability' P_{ci} can be calculated with (5), if for each marked frequency f_i in *Fig. 4* the appropriate SNR_i-value is introduced in (5) for E/N_0, i.e.

$$P_{ci} = \frac{1}{2} \cdot e^{-\frac{\mathrm{SNR}_i}{2}}. \tag{6}$$

When n distinct frequencies per data bit are involved, we yield the bit error probabilty in case of hard decision [10]

$$BEP_{n\mathrm{H}} = \sum_{i=\mathrm{INT}\{\frac{n}{2}\}+1}^{n} \binom{n}{i} \cdot (P_{ci})^i \cdot (1 - P_{ci})^{n-i}. \tag{7}$$

Although various attempts for modelling power lines as digital data transmission channels are known from literature, see e.g. [2, 3, 14, 16], there is a lack of universal applicability. Universal models tend towards high complexity, making the handling almost impracticable or at least difficult and time-consuming. So the author decided to perform computer simulations to determine bit error probability (BEP) approximatively. The simulations are based on data gathered at a link with properties according to *Fig. 4*. The basic idea is to perform random variations of SNR_i — values within the specified range (0 dB ± 2 dB — as previously outlined) and to calculate the corresponding BEP-values using (6) and (7). From a high number of samples — i.e. numerous different BEP-values — a mean value is calculated for comparison with measurement data. The impact of synchronization errors is included.

Computer simulations based on the measurement results of *Fig. 4* are proposed in the following. As already mentioned, for $V_s = 0.353 V_{\mathrm{rms}}$, we have a mean signal to noise ratio $\mathrm{SNR}_1 \approx 0$ dB, exhibiting ±2 dB variations. Then for $V_s = 0.707 V_{\mathrm{rms}}$ we have $SNR_2 \approx 6$ dB ± 2 dB, and for $V_s = 1.06 V_{\mathrm{rms}}$ we have $SNR_3 \approx 9.5$ dB ± 2 dB. The synchronization error τ is involved in the simulations with the above mentioned worst case value $\tau = 72\mu$s, leading to a degradation of about 0.19 dB, as previously calculated. In *Fig. 13* simulation results are plotted in form of three traces of 500 samples of $BEP_{n\mathrm{H}}$ for each of the three transmission voltage values: 0.353 V, 0.707 V, 1.06 V. The index n (at $BEP_{n\mathrm{H}}$) stands for $n = 5$

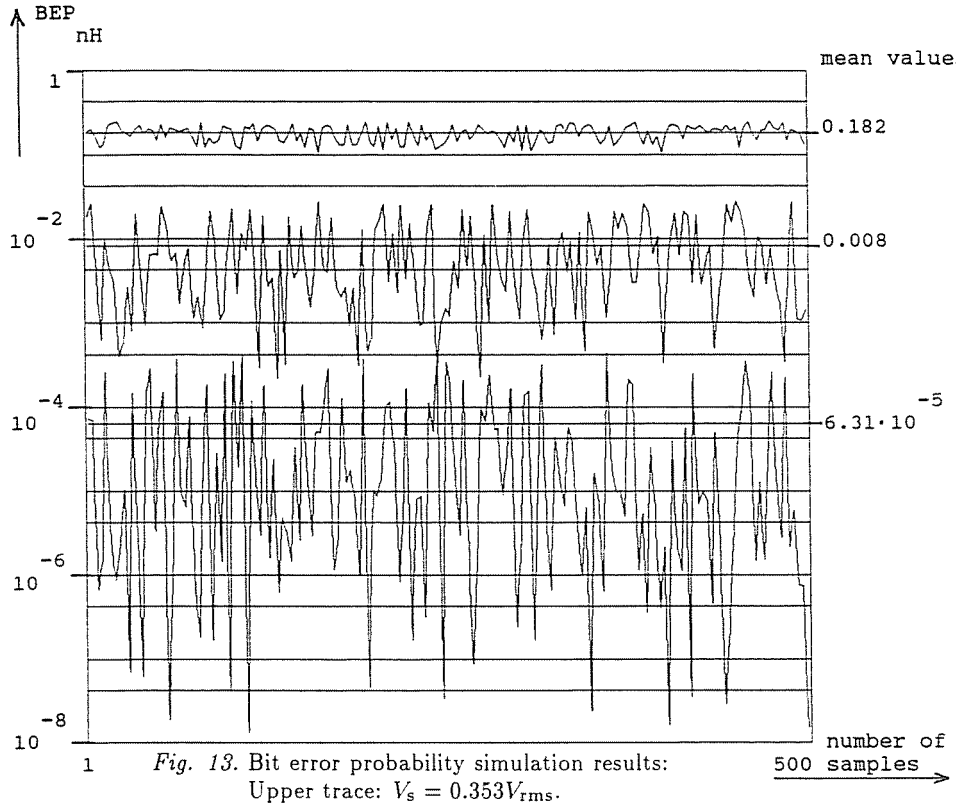

Fig. 13. Bit error probability simulation results:
Upper trace: $V_S = 0.353 V_{rms}$.
Medimum trace: $V_S = 0.707 V_{rms}$.
Lower trace: $V_S = 1.06 V_{rms}$.
(V_S is the transmission voltage)

frequencies per bit and H stands for hard decision, according to (7). The resulting mean values of bit error probability — 0.182, 0.008, $6.31 \cdot 10^{-5}$ — are marked and written at the left margin of *Fig. 13*.

For measurements a transmitter with three selectable values of the transmission voltage V_S was placed in a one-family house, transmitting test data — a 127 bit maximum length shift register sequence — over a power supply cable of about 1 km to a transformer station. At a data rate $r_d = 60$bits/s, and with the hop rate $h = 300\text{s}^{-1}$, $n = 5$ frequencies per data bit were involved. In the transformer station phases were coupled by three 0.1 μF capacitors. Measurements have been continuously performed over one year. The transmission voltage V_S was switched between three levels: $V_S = 0.353$ V, 0.707 V and 1.06 V (rms values). Switching always took place at the beginning of a week.

In *Fig. 14* the mean values of $BEP_{n\text{H}}$ gained by the described simulation are plotted together with measurement results for comparison. The

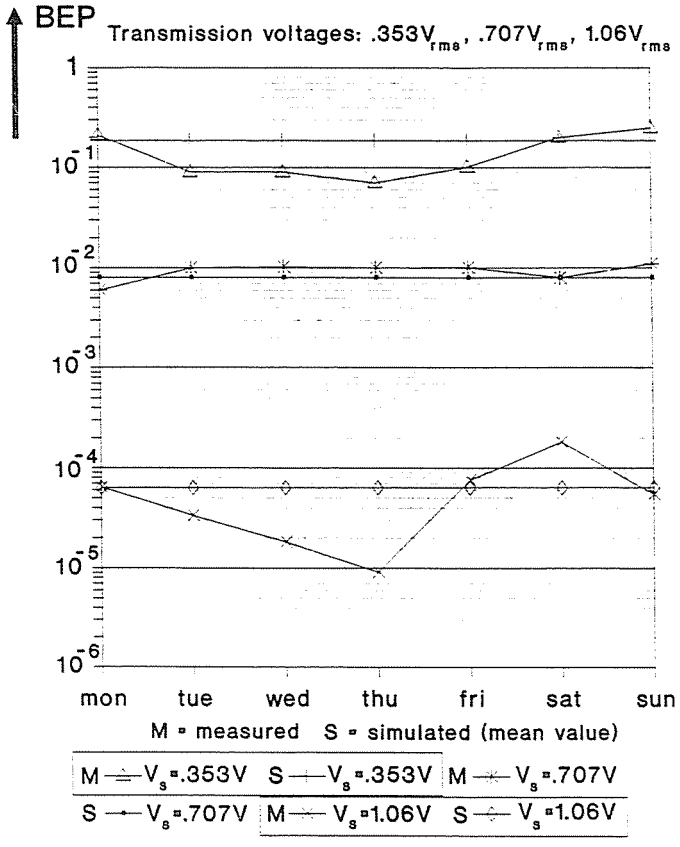

Fig. 14. Comparison of measured and simulated bit error probabilities for three different transmission voltages V_S

measured points of bit error probability (BEP) indicated in *Fig. 14* for each day of the week are mean values gathered within a time span of a year. Due to the weekly change of transmission voltage, each measured point for a day in *Fig. 14* represents actually a mean value of BEP over about 17 days with three week intervals between them. *Fig. 14* demonstrates good accordance of simulation and measurement results, confirming the validity of the outlined simulation procedure.

Impact of the Decision Strategy

A hard decision strategy according to (7) leads to the bit (L or H), for which at least three of five chips were detected. A previous decision is made for each chip in this case. A different strategy, i.e. soft decision, does not perform decisions after each chip, but sums up the matched filter outputs for the duration of a complete bit and makes one final decision. It is known that for constant amplitude of the received signal corrupted by white Gaussian noise, soft decision exhibits approximately a 3 dB enhancement of performance compared with hard decision. In many cases, however, soft decision is not applicable because of high efforts. Fortunately soft decision can be easily implemented into the outlined FH system because a microcontroller is used for bit decision. For channels with properties according to *Figs. 1–4* the performance gain through soft decision compared with hard decision depends on the chip and data rates. That means, if a certain kind of impulse noise is present, the performance of soft decision may be inferior to hard decision. The reason for this is, that a single large-energy impulse can override the soft decision process, whereas in case of hard decision typically only one chip is damaged. For the outlined FH system the chip duration $T_c = 3.3$ ms is relatively long compared with typical noise impulses on power lines [11]. Obviously, impulse noise is not a dominant source of errors here. As a result superiority of soft decision is expected. In fact, the implementation of soft decision brought the bit error probability at the 1 km power supply cable down to $BEP_1 \approx 4 10^{-5}$ for $V_s = 0.353 V_{\mathrm{rms}}$, $BEP_2 \approx 6.25 \cdot 10^{-6}$ for $V_s = 0.707 V_{\mathrm{rms}}$, and for $V_s = 1.06 V_{\mathrm{rms}} BEP = 3.9 10^{-7}$ was measured. The latter case represents indeed a rather reliable data link for a variety of interesting applications.

Conclusions and Further Work

The exploitation of electric power distribution networks as reliable links for measuring and control signal transmission at relatively low data rates appears under completely new aspects, when spread spectrum techniques are involved. It has been shown that frequency hopping provides satisfying performance even under severe transmission power restrictions. A benefit of frequency hopping is the ability to spread information over a wide frequency range, involving low chip rates. So global synchronization based on the power line voltage as reference is feasible. Starting from the synchronization timing scheme, an FH spread spectrum system was developed, built, and tested in real world environments. It has been shown that a completely digitally functioning FH system is superior to analog

solutions under various aspects. For digital receiver construction the implementation of an ASIC as matched filter proved to be advantageous. For factory and office building automation, e.g., the availability of modems with half-duplex capability is important. Such modems have been completed recently. A higher level of integration including the microcontroller functions into a new ASIC, which will be realized as a cell array, is currently in the design phase. The goal to be reached in the near future is to make a digitally operating FH spread spectrum modem according to the concept outlined in *Fig. 12* fit into the housing of a standard wall-socket with a power consumption in the range of some hundred milliwatts.

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