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ELECTRON TRAPS INVESTIGATION IN ION IMPLANTED MESFETS

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Abstract

Capacitance and conductance Deep-Level Transient Spectroscopy has been performed in n^- ion implanted MESFET channel layers prepared on semi-insulating Cr-doped LEC GaAs substrates together with the investigation of their electrical properties. Experimental results achieved by both methods have been compared and used for deep-level identification. Six significant electron traps have been detected. Important defect and recombination parameters such as density profiles and energy level of electron traps, thermal emission rates and capture cross section were deduced from these measurements.

Keywords: deep-levels, deep-level transient spectroscopy, ion implantation, GaAs, MESFET

Introduction

Channel layers of GaAs MESFETs are commonly formed by selective ion implantation into semi-insulating substrates. It is necessary to achieve a high degree of threshold voltage reproducibility and high free electron mobility for integrated circuits applications. Therefore a tight control of ion implantation and activation process is indispensable.

In a typical application, low dose ($< 10^{13}$ ions/cm^{-2}) 50–200 keV silicon ions are implanted into semi-insulating GaAs and subsequently the implanted wafer is furnace annealed at 800°C to 900°C for 10 to 20 minutes. Variation of parameters, such as beam energy, encapsulant layer thickness, annealing temperature and time, implant dose and nature of the semi-insulating GaAs wafer affects the electrical properties of the channel layer. Simultaneously deep-levels are introduced into the implanted layers as a result of lattice defect formation or stoichiometry change during the ion implantation and annealing. These levels produce time dependent effects such as drain current drift, looping of the characteristics and backgating. Deep-level transient spectroscopy (DLTS) (LANG, 1974) has been widely used as a probe for deep-levels detection in ion implanted and annealed layers (KUZUHARA et al., 1986). This technique provides information on

the electronic properties of the damage defects, their concentrations and distribution with depth.

In short-gate GaAs MESFETs, the DLTS technique is commonly used in the conductive mode (SRIRAM et al., 1983) based on monitoring of the transient response of the drain current, since the gate capacitance is too small for an accurate detection of the capacitive transients. On the other hand, in the conductance DLTS spectra measured on short-gate FETs, where the ungated surface of the device becomes commensurate with the surface area of the gate electrode, we can observe a signal whose sign corresponds to the emission of minority carries. This surprising phenomenon may be explained in terms of a depletion region relaxation due to the surface states (BLIGHT et al., 1986, HARRANG et al., 1987).

The present paper deals with the investigation of electron traps in n^- ion implanted channel layers prepared by selective direct ion implantation of Si^+ ions into semi-insulating Cr doped GaAs substrate. Both capacitance and conductance DLTS were used for traps identification in GaAs MESFETs with different geometry. DLTS study is supplemented by electrical and optical characterization of the investigated layers prepared under different annealing conditions.

Experiments

The GaAs wafers used for both experimental studies — the investigation of the electrical parameters of the channel layers and the measurement of the electron traps in GaAs MESFETs — were prepared form (100) — oriented liquid encapsulated Czochralski (LEC) grown Cr-doped semi-insulating single crystals. In the first case, the $^{28}Si^+$-ion implantation was carried out with a dose of 4×10^{12} cm^{-2} at an energy of 160 keV at room temperature in a nonchannelling direction. Following the implantation the samples were covered with an 80 nm thick layer of pyrolytic SiO_2, deposited at 650°C during 15 minutes. Isochronal furnace annealing of the implanted samples was performed in a dry argon atmosphere for 15 minutes at 800°C, 830°C, 860°C and 900°C temperatures. The electrical properties were determined by Hall-effect measurements. The concentration profiles of free carriers were measured using a Polaron 4200 C–V profiler. To make clear the optical properties of the implanted layers, photoluminescence measurements were made at 80 K and 10 K using the 514.5 nm line of the cw Ar–ion laser as an excitation source.

MESFET transistors used for DLTS measurements were prepared by planar GaAs integrated circuit technology based on multiple local ion implantation in the TESLA Popov Research Institute of Radiotelecommuni-

cation. The fabrication details of these devices can be found in (CHMEL, 1986). Two types of $^{28}Si^{+}$-ion implantation were used: The shallow one (160 keV 3×10^{12} cm^{-2}) for forming the MESFET channel and a deeper one (200 keV 8×10^{12} cm^{-2}) located in the switching diodes region. Both implants were used for the level-shifting diodes and for the layers under the ohmic contact regions. Subsequent furnace annealing was done at 850°C for 15 minutes with the incorporation of 80 nm thick pyrolytic SiO_2 cap. Schottky Au–Cr or Ti–Pd–Au contacts were fabricated by plasma sputtering.

Two types of MESFETs were used for DLTS measurement: FATFET testing structure with 255 μm gate-length and a normal short-gate (3.2 μm) device. The drain-to-gate and source-to-gate spacing were 25 μm for FATFET and 3.2 μm in the case of the short-gate FET. Capacitance DLTS measurements were made using a computer-controlled multichannel system based on the utilization of the HP 4280A 1MHz capacitance meter. The source and drain of the MESFET were short-circuited and the FET structure was used as an ordinary Schottky diode. Capacitance transients as a result of electron emission from the traps were observed after majority carrier filling pulse excitation. Conductance DLTS measurements were realized as follows: A small DC bias voltage $V_{DS} = 40$ mV was applied between the source and the drain of the MESFET so that it operated in the ohmic region. Electron traps in the Schottky barrier gate depletion region were filled by reducing the gate reverse bias for a short time (20 μs) to avoid emission from the surface states into the ungated channel and from the traps into the backgate-substrate region. Upon returning to the quiescent bias, the electron traps emit electrons with their characteristic emission rate, causing the depletion width and hence the channel current to vary. In the case of small change of the depletion layer width the transient is purely exponential with a time constant being proportional to the electron emission rate just like in the case of the capacitance transient. Current transients corresponding to the change of the MESFET conductance were monitored using fast current to voltage converter and processed by computer-controlled DLTS system based on the utilization of a lock-in amplifier.

Results and discussion

The temperature dependence of sheet carrier concentration and electron mobilities measured by Hall-effect of 160 keV 3×10^{12} cm^{-2} Si implant is summarized in *Fig. 1*. Data shown here are not corrected for surface depletion. It is shown that the mobility is nearby constant over the 800°C

to 860°C temperature region and drastically decreases above the 860°C annealing temperature. Activation increases with the annealing temperature and reaches its maximum value of 70% between 860°C and 900°C. *Fig. 2.* shows typical carrier concentration depth profiles of the investigated layers obtained from electrochemical C–V profiler measurements for different annealing conditions. The curve of LSS theory is also shown. The obtained results correspond to the conclusions of the Hall-effect measurements. The peak carrier concentration achieved at the highest degree of activation is about 1.6×10^{17} cm^{-3}.

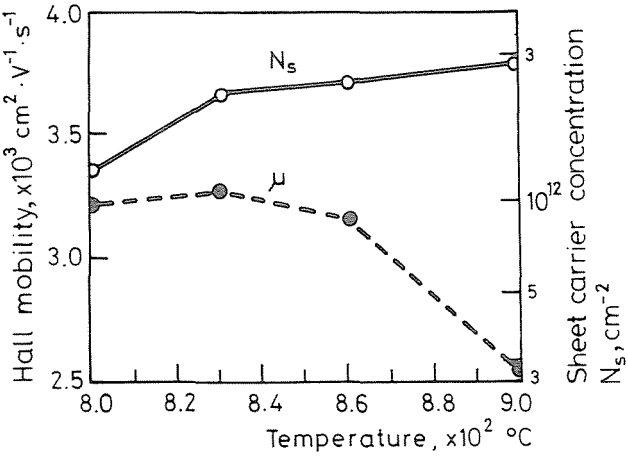

Fig. 1. Temperature dependence of sheet carrier concentration and Hall mobility

Photoluminescence measurements were carried out for all annealing temperatures at 10 K and 80 K in the emission wavelength range between 800 nm and 1600 nm. The following significant emission peaks were resolved in all measured photoluminescence spectra: the 1.51 eV emission peak due to the near intrinsic band-to-band transition, the 1.49 eV peak associated with carbon-related transition and his LO-phonon replica (1.46 eV) and a broad 1.32 eV emission band, whose origin is not clear at present but it may be related to the occurrence residual damages. The emission band at 1.476 eV related to an acceptor level of Si on As site was observed in neither of the measured photoluminescence spectra. This indicates that all activated Si atoms replace Ga sites and show donor behaviour in the applied annealing temperature range. The 1.51 eV peak height increased (*Fig. 3.*) and the 1.32 eV broad band emission intensity decreased with increasing annealing temperature. This shows an increase of the donor concentration and the removal of the ion implantation defects with increasing

post-implantation annealing temperature. These results correspond to the conclusions of the electrical measurements and all together show that the post-implantation annealing conditions used for MESFET channel layer activation (850°C 15 min) provide maximal carrier mobility, optimum activity and good reproducibility.

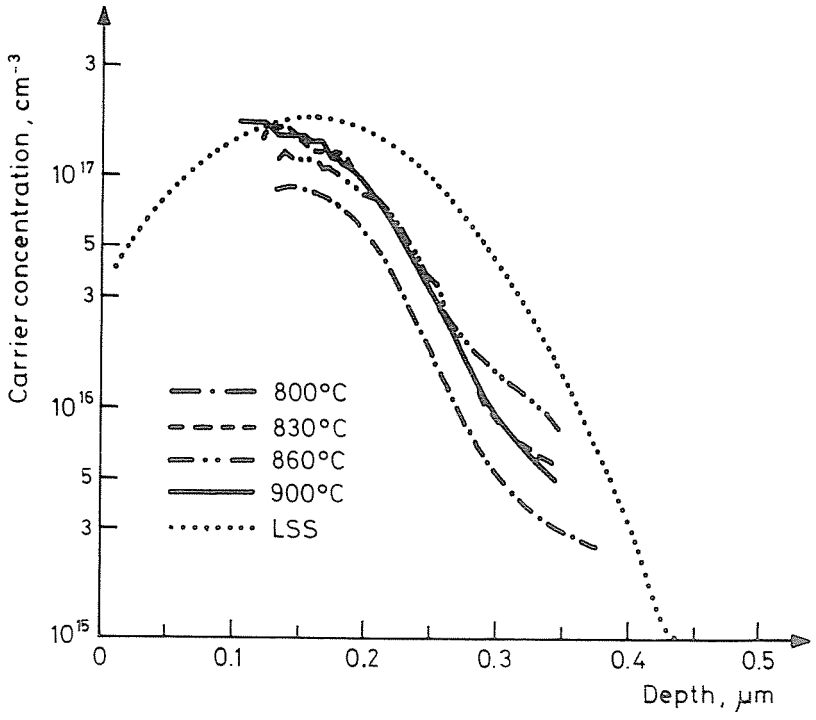

Fig. 2. Typical carrier concentration depth profiles

Conductance DLTS measurements were carried out on short- and long-gate MESFETs from different production series. *Fig. 4.* and *Fig. 5.* shows representative electron-trap DLTS spectra of the long-gate (FAT-FET) and short-gate MESFETs. In all samples six major electron traps (E1–E6) were observed. The absence of the minority-like traps shows that there is no influence of the surface states emission in the ungated channel region. Analogous spectra were obtained by capacitance DLTS measurements (*Fig. 6.*). The identification of the electron traps was based on comparison with the literature:

The electron trap E1 ($\Delta E_T = 0.15 - 0.18$ eV, $\sigma_n = 1 \times 10^{-18}$ m^2): The activation energy of this level was spatially dependent. The same level was also detected in GaAs MESFETs fabricated by Si ion implantation

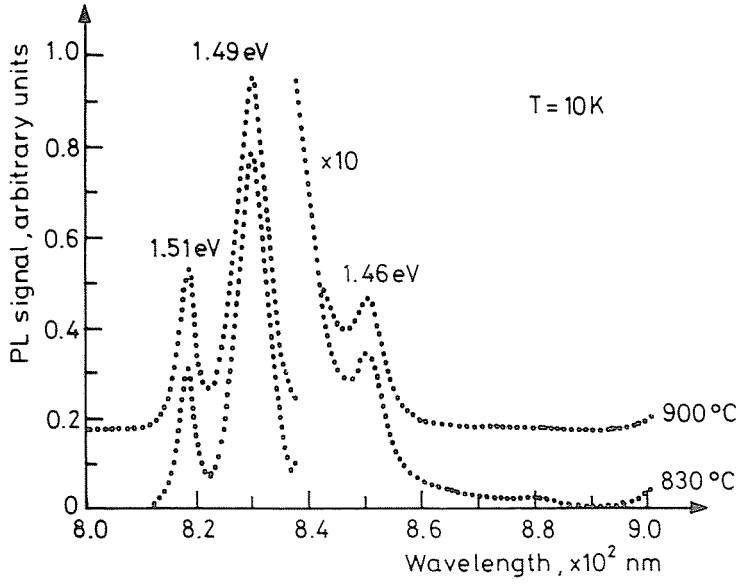

Fig. 3. Photoluminescence spectra

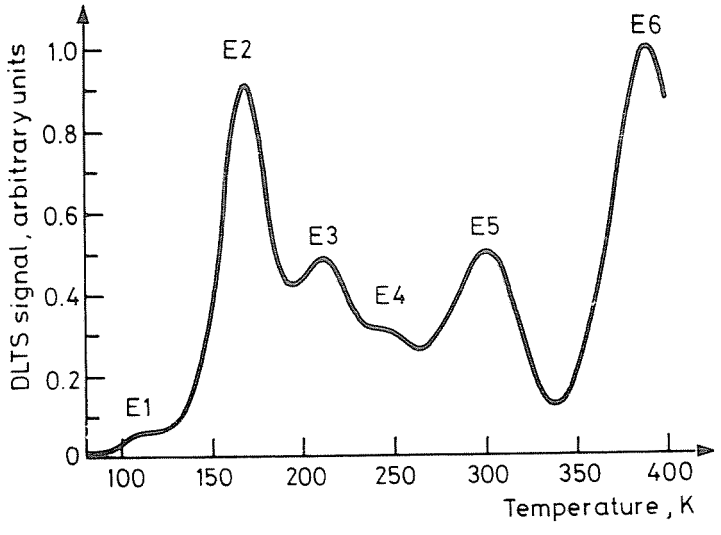

Fig. 4. Electron-trap DLTS spectrum of long-gate MESFET

into undoped as well as Cr-doped GaAs substrate (SRIRAM et al., 1983)

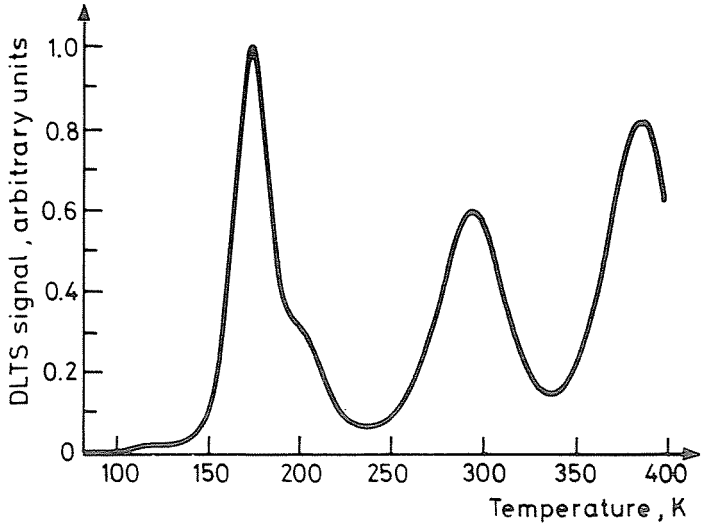

Fig. 5. Electron-trap DLTS spectrum of short-gate MESFET

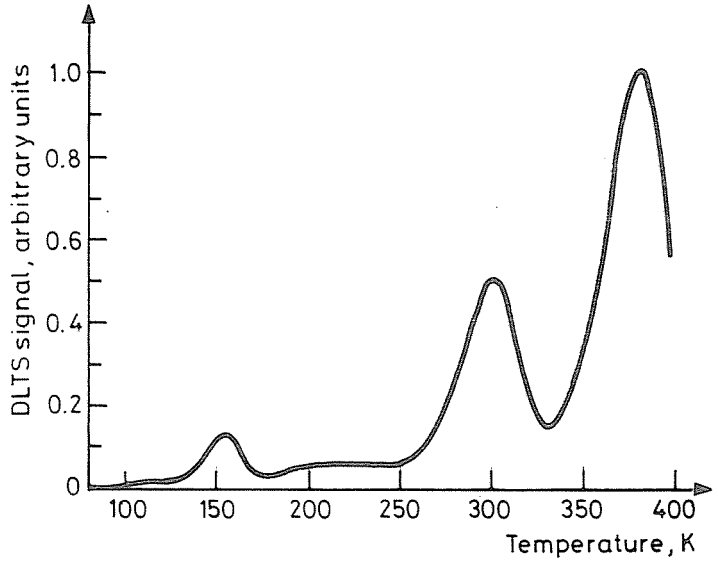

Fig. 6. Result of capacitance DLTS measurement

and in furnace annealed Si implanted GaAs (HENINI et al., 1986). It might be attributed to the EL11 level.

The electron trap E2 ($\Delta E_T = 0.28$ eV, $\sigma_n = 1 \times 10^{-18}$ m^2):
This investigated electron trap did not correspond to any level previously reported in the literature. It was therefore considered to be new.

The electron trap E3 ($\Delta E_T = 0.33$ eV, $\sigma_n = 8 \times 10^{-20}$ m^2):
This electron trap has been observed by many authors in Si implanted GaAs layers obtained by rapid thermal annealing (CHAN et al., 1986), furnace annealed Si implanted GaAs (WANG et al., 1981) and Si implanted GaAs MESFET layers with Cr–Au metallization (CHRISTOU et al., 1985). It might be attributed either to an unknown impurity or to recoil-induced defect or to Cr–GaAs interdiffusion effect.

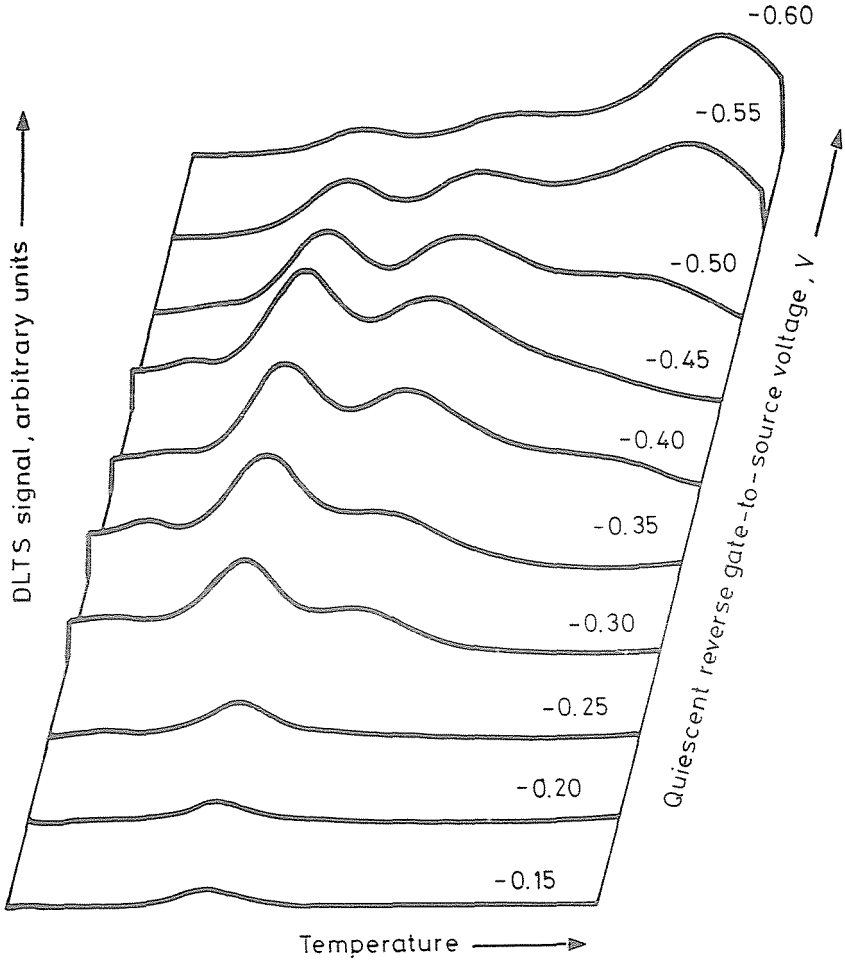

Fig. 7. Deep-level defect distributions

The electron trap E4 ($\Delta E_T = 0.42$ eV, $\sigma_n = 7 \times 10^{-19}$ m^2):
This level could be the same as the trap found by (HENINI et al., 1986) in annealed LEC GaAs layers and by (MARTIN et al., 1977) in VPE GaAs layers and labelled by them as trap EI1. Its origin is not known.

The electron trap E5 ($\Delta E_T = 0.58$ eV, $\sigma_n = 1 \times 10^{-18}$ m^2):
This defect state was reported in the case of ion implanted MESFETs based on Cr-doped substrates (SRIRAM et al., 1983) and in the case of VPE MESFETs fabricated on Cr-doped semi-insulating GaAs (GHEZZI et al., 1987). It was assigned to electron trap EL3 or to a Cr associated level.

The electron trap E6 ($\Delta E_T = 0.84$ eV, $\sigma_n = 2 \times 10^{-17}$ m^2):
This trap is called EL2 and has received a great deal of attention for many years. Recently, this trap has been attributed to an GaAs antisite defect (HENINI et al., 1986).

The deep-level defect distributions were obtained using results of many conductance DLTS measurements. Each spectrum was obtained with small pulse (0.15 V) excitation superimposed on different dc bias so that the investigation of various channel layer regions was possible (*Fig. 7.*). Deep-level distributions (E1, E2, E3, E5) in the channel layer of long-gate MESFET obtained in this manner is shown in *Fig. 8.*

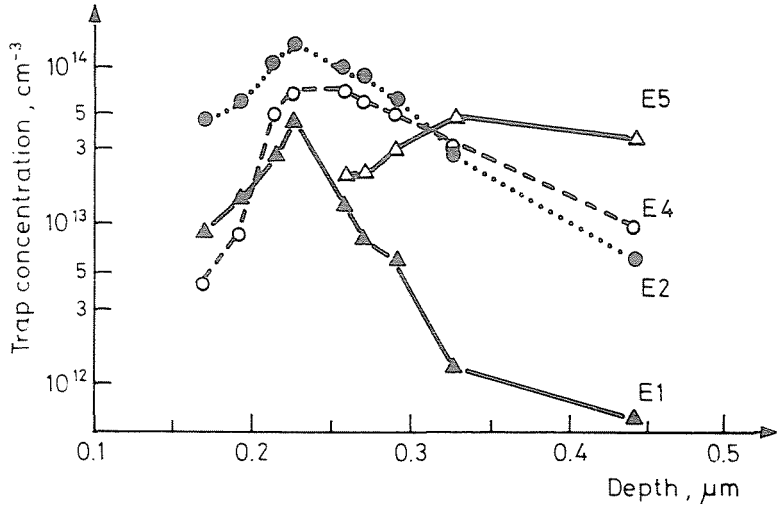

Fig. 8. Deep-level distributions in the channel layer of long-gate MESFET

The distinct shape of the E5 profile implies a different nature of this defect in comparison with electron traps E1, E2, E3 whose generation might be associated with ion implantation, annealing or surface treatment. It

confirms the assumption that the E5 level is connected to bulk effects like chromium occurrence.

Conclusions

The influence of the annealing temperature on the electrical and optical parameters of Si-ion implanted channel MESFET layers was studied. The results show that temperatures near 850°C provide optimum activity and maximal carrier mobility. Conductance and capacitance DLTS measurements were used in order to identify the electron traps in implanted n^- MESFET channel layers annealed under different conditions described above. The results achieved by both methods were comparable and confirmed the presence of six electron traps. Deep-level identification showed an analogy between the detected electron traps and the deep-level reported for analogous MESFET structures.

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