NEW STRUCTURE OF A FAST HIGH RESOLUTION ADC WITH GOOD LINEARITIES

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Abstract

This paper proposes a new structure of a high speed analog-to-digital converter (ADC) with high resolution and good linearities. First a coarse survey of common architectures for high speed ADC-s with high resolutions including their drawbacks and limits is given. The principle of the proposed ADC is discussed and electronic circuits, used in this structure, are noted.

Keywords: analog to digital converter, linearity error, fast ADC.

Introduction

The most common architecture for a high-speed ADC is the parallel or flash converter structure (ZOJER et al, 1985). In this structure (*Fig. 1.*) a set of increasing reference voltages is generated by connecting a series string of equal value resistors R to a reference voltage source V_{ref}. Each reference voltage corresponds to a quantization level. For each quantization level there is one comparator, comparing the input voltage V_x with the reference voltage. The output of those comparators whose reference voltages are smaller than V_x is high, i.e. '1'. The other outputs assume the state '0'. At a certain rate dictated by the sampling frequency, these states are transferred to a corresponding number of latches, where they are stored. In a decoding logic the digital output is then obtained in the required code.

The major merit of this conversion technique is its high speed, but its major drawback is the high component count. For an n-bit ADC the required number of comparators is $(2^n - 1)$ and the required number of precision resistors is 2^n. One more bit resolution of the converter requires a doubled amount of components (comparators, resistors, latches). In addition there is need for a high quality buffer amplifier, that is able to feed, both statically and dynamically, this large number of comparators in parallel.
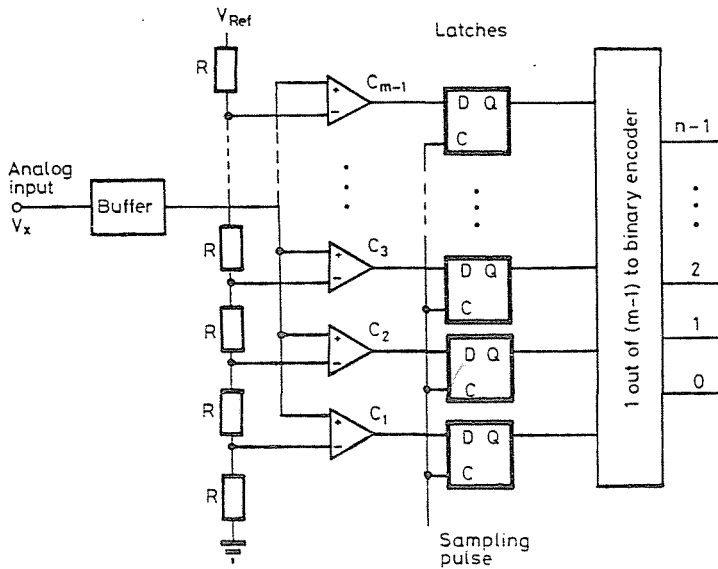
Fig. 1. Flash ADC

   A technique that trades conversion speed for circuit simplification is
the parallel-series or cascade approach (MUTO et al, 1982). In a two stage
cascade (*Fig. 2.*) a coarse flash encoding of the input voltage is performed
to get the most-significant bits. Then the analog voltage equivalent to the
coarse encoder's digital output is generated and this is subtracted from
the input voltage. The difference voltage is then digitized by a fine flash
encoder to get the least-significant bits.

   With this subranging technique a remarkable reduction of compo-
nents is achieved. A 8-bit parallel-series converter can be built with 30
comparators — an order of magnitude reduction, compared to the par-
allel flash converter. However, there are significant tradeoffs. Not only
is the parallel-serial converter slower, but it also requires several difficult-
to-build components: a high-speed digital-to-analog converter (DAC) that
transforms the first-pass word into an analog level, a high-speed operational
amplifier that performs the subtraction, and a high-performance sample-
and-hold circuit that guarantees no change of the input voltage between
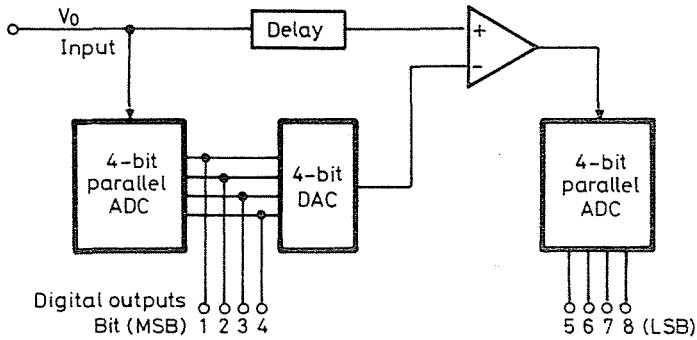the first-pass and the second-pass conversions.

Fig. 2. Cascade (two step) ADC

A structure of a fast ADC, which needs neither a DAC nor a subtract-
ing amplifier is an ADC based on the folding principle (VAN DE PLASSCHE
and BALTUS, 1987; ARBEL and KURZ, 1975). In these converters the analog
signal is encoded before it is converted into the digital domain. The folding
technique is like taking the quotient and the remainder of the input signal
and some part of the input signal range. This folding process is shown in
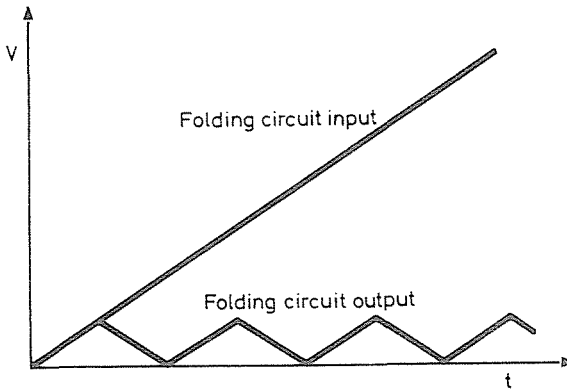Fig. 3.

Fig. 3. Folding process: input and output voltages V vs. time t

Note that the folded signal is not quite the remainder of the input sig-
nal divided by some subrange: this would have been a sawtooth signal. But
the discontinuities of the sawtooth signal contain very high frequency com-
ponents which are difficult to process. A triangular signal is used instead,
containing the same information differently coded.

A structure of a folding ADC is shown in the block diagram *Fig. 4.*
The input signal is put in parallel to a folding circuit and a 4-bit flash
ADC. This flash ADC makes a coarse quantization and indicates one of
16 subranges where the input signal actually is. The output of the folding
stage is also fed to a 4-bit flash ADC. These 4 bits indicate the offset of the
input signal within one of the sixteen subranges. In this way the number
of comparators for the flash converter is reduced to 30 instead of 255. In
addition, as conversion from signal value into quotient and remainder (or
coarse and fine quantization) is done in the analog domain, there is no need
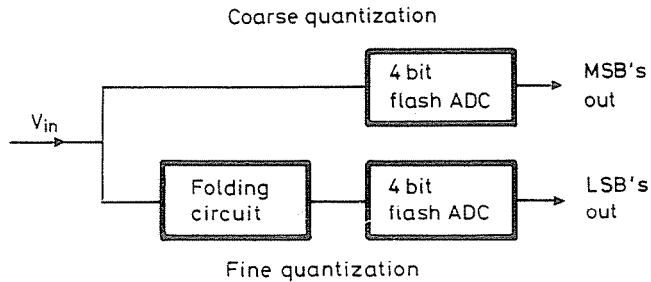for a sample and hold circuit.

Coarse quantization

V_{in}

4 bit
flash ADC
MSB's
out

Folding
circuit
4 bit
flash ADC
LSB's
out

Fine quantization

Fig. 4. Block diagram of a folding ADC

Architecture and principle of the proposed ADC

The new proposed ADC structure (see below) also eliminates many of
the disadvantages of the two step ADC. Instead of the usual division into
subranges with coarse ADC, DAC and subtracting amplifier, a so called
window-amplifier (WA) is used for each subrange. In *Fig. 5.* the basic
idea of the new ADC is demonstrated.

The input voltage range is divided into several subranges and each of
them is projected to the full scale range of an ultra fast ADC. This split up
is done by the WA-s, which amplify the input signal only in a certain range.
Fig. 6. gives an example of the basic structure of this ADC. Using an 8-bit
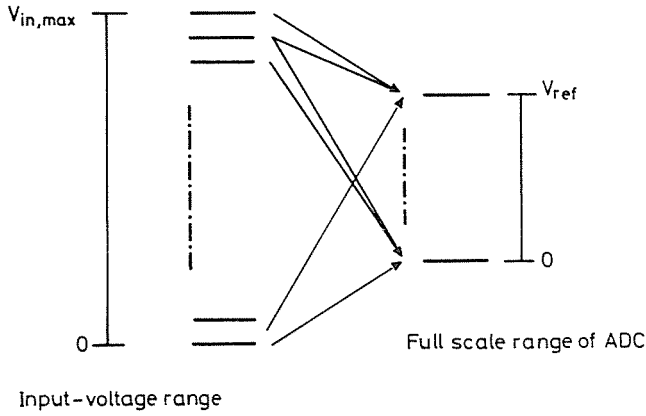ultra fast ADC and 4 WA-s, a total resolution of 10 bits is achieved.

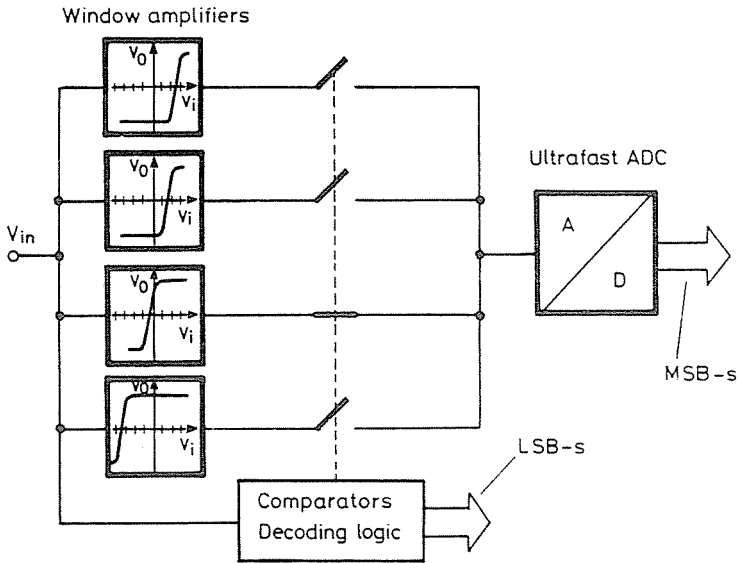*Fig. 5.* Principle of the new ADC

Fig. 6. Basic structure of the proposed ADC

According to the input signal only one of these WA-s is in its active range, so only this amplifier-output is switched in a suitable way to the ultra fast ADC.

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The WA-s only have to have the bandwidth of the input signal, so the dynamic behaviour is better compared with the cascade ADC, where the subtracting amplifier has to handle the high slew rate of the output signal of the DAC.

The transfer characteristic (*Fig.* 7.) shows some problems occurring with the basic structure:

  —close to the boundaries of the subranges the linearity deteriorates;
  —the transitions between the subranges are hard to realize;
  —high-frequency input signals with low amplitudes, situated between the subranges will cause problems to the switches;
  —the WA outputs have to be selected very accurately by high precision comparators (decoding of the Msb-s).
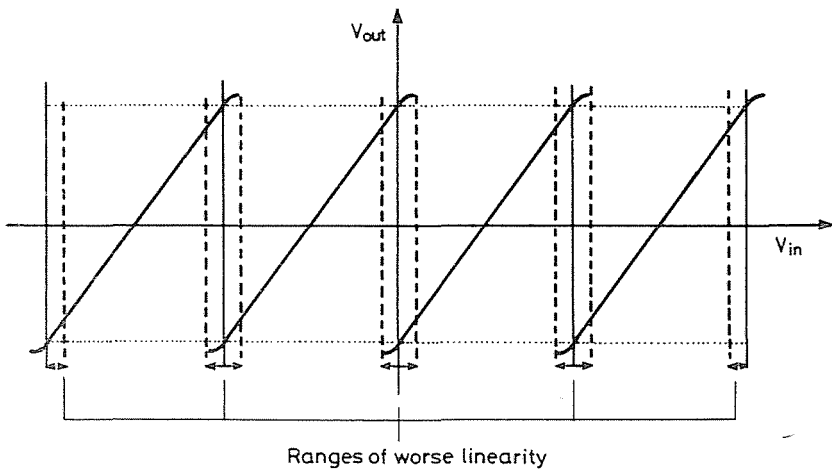
Ranges of worse linearity

Fig. 7.   Transfer characteristics of the basic structure

All trouble associated with the switches can be eliminated by using a separate ultra fast ADC for each WA output. So only the output of the ADC-s are selected which can be done digitally in a convenient way. At the moment, due to prices of ultra fast ADC-s, this would not be a very economical approach. But in order to reduce the problems arising by switching the WA outputs two ultra fast ADC-s are used.

A further step to improve the basic structure is made by overlapping the ranges of the WA-s. In this way wrong codes, caused by wrong switching of the comparators, are eliminated and in addition a better linearity is achieved. Because of this overlapping the account of WA-s has to be
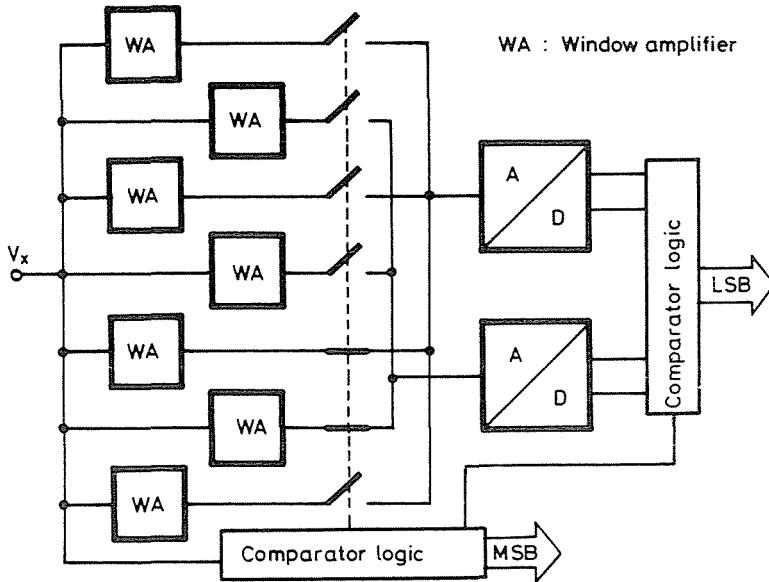
Fig. 8. Block diagram of the improved ADC structure

increased to get the same total resolution of the converter. In the final structure (*Fig. 8.*) two sets of WA-s (total count is 7) are used with a 50% overlapping.

In the new transfer characteristic (*Fig. 9.*) the continuous line indicates the first set of WA-s, feeding ADC1, and the dotted line indicates the second set, feeding ADC2, respectively. In this characteristic also the threshold voltages of the comparators with associated uncertainties are drawn.

Obviously, using the two sets of WA-s, there is at least one amplifier in a range of good linearity. The ultra fast ADC, supporting the LSB-s, converts the output signal of this WA, while non-linearities of adjacent WA-s have no effect. A logic, which selects the ideal WA output by decoding the states of the comparators, delivers the MSB-s of the converter.

For the best performance of the whole system two sets of comparators are used:

—one is driving the switches and selects the WA output to be connected to the two ADC-s;

—the second one chooses the digital output of the one ADC, which converts in the best subrange.
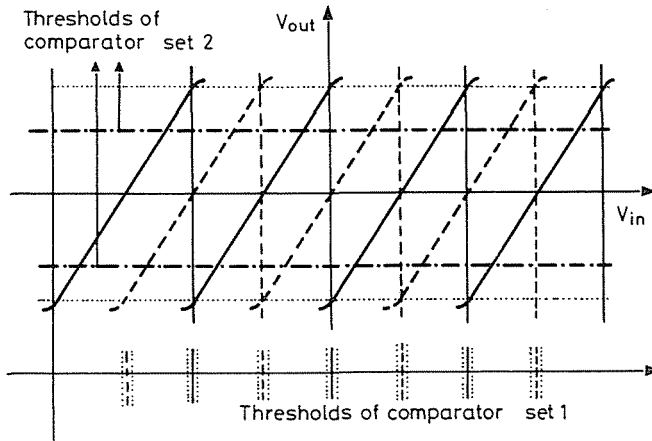
Fig. 9.   Transfer characteristics of the improved ADC structure

The thresholds of the first comparator-chain are located at the transitions of the subranges, the ones of the second comparator-chain at about 1/4 and 3/4 of each range. The exact level of the threshold voltages is already unimportant due to overlapping of the subranges. In *Fig. 9.* the ranges of the ADC-s, actually used, are marked with dotted lines at 1/4 and 3/4 of the WA output range. So a rising input voltage V_x causes a change from ADC1 to ADC2 already at about 3/4 of the WA output range. At this time all comparators, used to decode the MSB-s, are in a stable state, if the time, in which the input voltage passes one subrange, is not smaller than the switching times.

In the improved structure (*Fig. 8.* and *Fig. 9.*) there are still some critical points to consider. Different gains of the WA-s are displayed in different slopes of the transfer characteristics of each subrange. Furthermore, inaccuracies of the reference voltages of the WA-s produce an offset error in the corresponding subranges (*Fig. 10.*). But the errors, mentioned before, can be eliminated easily during the production by performing a calibration cycle and storing the codes for correction.

The method of overlapping offers a further possible way of error correction. *Fig. 11.* shows the transition between two subranges in greater details. Obviously there are two output codes available for one input voltage V_x. These two code words can be used for error correction by taking their mean. To accomplish this correction all transients from switching may not add any dynamic errors.
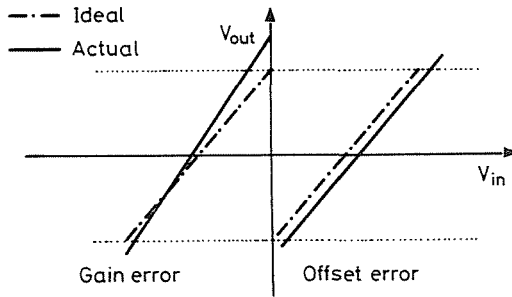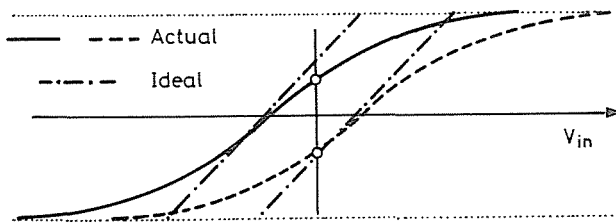
Fig. 10. Offset and gain error

Fig. 11. Transition between two overlapping subranges

Electronic realization

The basic principle of a WA is a differential amplifier (*Fig. 12.*). To pro-
vide sufficient linearity, emitter resistors are used, although their presence
reduces the gain but also increases the input impedance. To reduce the
influence of the Miller capacity at high frequencies the cascode differential
amplifier is used.

The dynamic performance of the proposed ADC is mostly influenced
by the switches, connecting the WA outputs to the ADC-s, and their driving
logic. Generally with a switch based on a diode gate (*Fig. 13a.*) switching
times in the sub-nanosecond-region could be realized. But the design of the
electronic circuit is done with respect to an integration. As the diode gate
switch contains pnp transistors, which cause difficulties in the integration
process, a current switch (basic principle see *Fig. 13b.*) is used. The ultra
fast ADC-s will be standard flash ADC-s, e.g. 8-bit 100 MHz (SDA 8010).
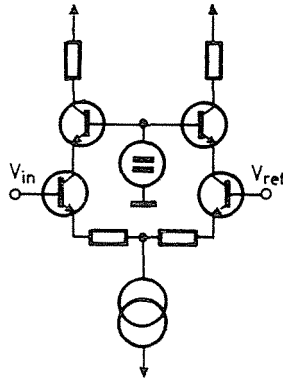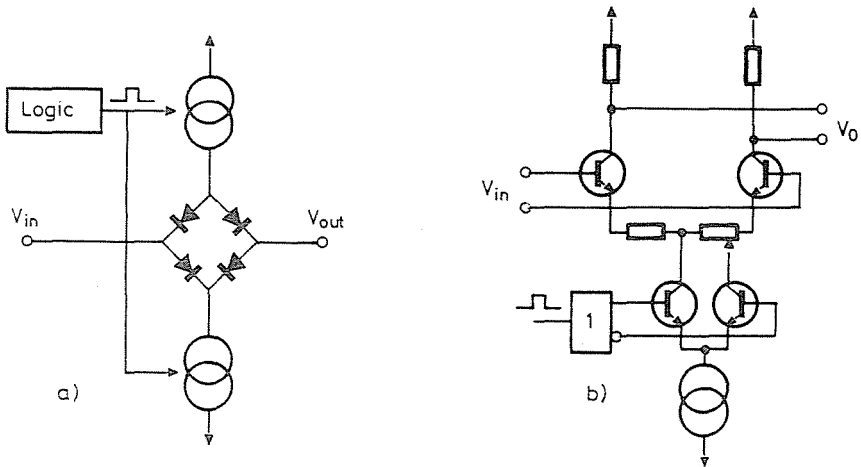
Fig. 12. Cascode differential amplifier

Fig. 13. a) Diode-gate switch, b) current switch

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