CHARACTERISTIC PROPERTIES OF JUSTIFICATION IN PLESIOCHRONOUS DIGITAL NETWORKS*

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Abstract

In this paper, the justification in plesiochronous digital networks is outlined. The branching processes model for evaluating the performances of random justified time slot streams is proposed. This allows to compute a probability distribution of series of justified time slots in the digital information streams. Justification jitter analysis is presented.

The problem of justification of digital information streams and switching processes appears in the design and planning of digital networks based on digital transmission systems and digital switching centers (DSC). The same problem is emerging in packet switching circuits with continuous digital streams to save on the carrying capacity of communication lines.

In numerous scientific works the problem of justification was related only to asynchronous multiplexing [1, 2]. In a justification scheme of multiplexer, time slots in the outgoing multiplexed signal will become available at a rate exceeding that of the incoming data, so that the tributary signal will tend to lag. At some stage the multiplexer will decide that this lag has become large enough to require justification; at this point a message will be sent to the receiving terminal to inform it of this decision, and the next assigned time slot will be justified. The receiving terminal will then delete justified time slot from the signal. It is purposive to carry out the analysis of justification in plesiochronous digital networks [4]. It should be noted that in plesiochronous digital networks the special features of justification are related with multiinserting and multiremoving justified time slots. If the information transmitting route is accidental and the switching rates of different DSC are independent even if they are approximately equal, the justified time slots stream is random. This paper deals with the analysis of justification in plesiochronous digital networks. The

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branching processes model for the evaluation of the performances of random justified time slots streams is used. This allows to compute a justified time slots distribution in the digital information streams. In addition, justification jitter analysis is presented. But for the sake of simplicity waiting-time jitter and communication lines jitter are not taken into account in this paper.

Regulation of justification

Consider the following network model:

1. The network topology is free
2. Network contains N DSC numbered from 1 to N and M sources of digital information numbered from 1 to M
3. The clock period of each link of a DSC is driven by the DSC clock generator.

Let us denote by $\delta_1, \ldots, \delta_N$ the clock periods of DSC and by $\Delta_1, \ldots, \Delta_M$ the clock periods of digital information sources. To avoid losses of information the data transmission rate from every source must be lower than the carrying capacity of interswitching centre links. This restriction can be written by

$$\delta_i \leq \Delta_j; \qquad i=\overline{1,N}; \quad j=\overline{1,M}. \tag{1}$$

Suppose that the traffic of the jth information source comes to the ith DSC. Let us denote by m_i the mth clock period of ith DSC, by $m_j(k_i)$ the mth information bit of jth information source before k_ith justified time slot, by β the number of clock periods of one justified time slot. The k_ith justified time slot occurs after $m_j(k_i)$th information bit, if

$$\begin{cases} \sum\limits_{m=m_j(k_i-1)+1}^{m_j(k_i)-1} \Delta m_j - \sum\limits_{m=m_j(k_i-1)+(k_i-1)\beta+1}^{m_j(k_i)+(k_i-1)\beta-1} \delta m_i < \sum\limits_{m=m_j(k_i)+(k_i-2)\beta}^{m_j(k_i)+(k_i-1)\beta-1} \delta m_i \\ \sum\limits_{m=m_j(k_i-1)+1}^{m_j(k_i)} \Delta m_j - \sum\limits_{m=m_j(k_i-1)+(k_i-1)\beta+1}^{m_j(k_i)+(k_i-1)\beta} \delta m_i \geq \sum\limits_{m=m_j(k_i)+(k_i-2)\beta+1}^{m_j(k_i)+(k_i-1)\beta} \delta m_i \end{cases} \tag{2}$$

If condition (2) is satisfied, then the k_ith justified time slot will be inserted into the outgoing digital stream after $m_j(k_i)+(k_i-1)\beta$th clock period of ith DSC. Geometric representation of justification is shown in Fig. 1. In the following, $i+1$th, DSC additional justified time slots will be inserted, if

$$\delta_{i+1} < \delta_i \tag{3}$$

or some justified time slots inserted at the first DSC will be eliminated, if

$$\delta_{i+1} > \delta_i. \tag{4}$$

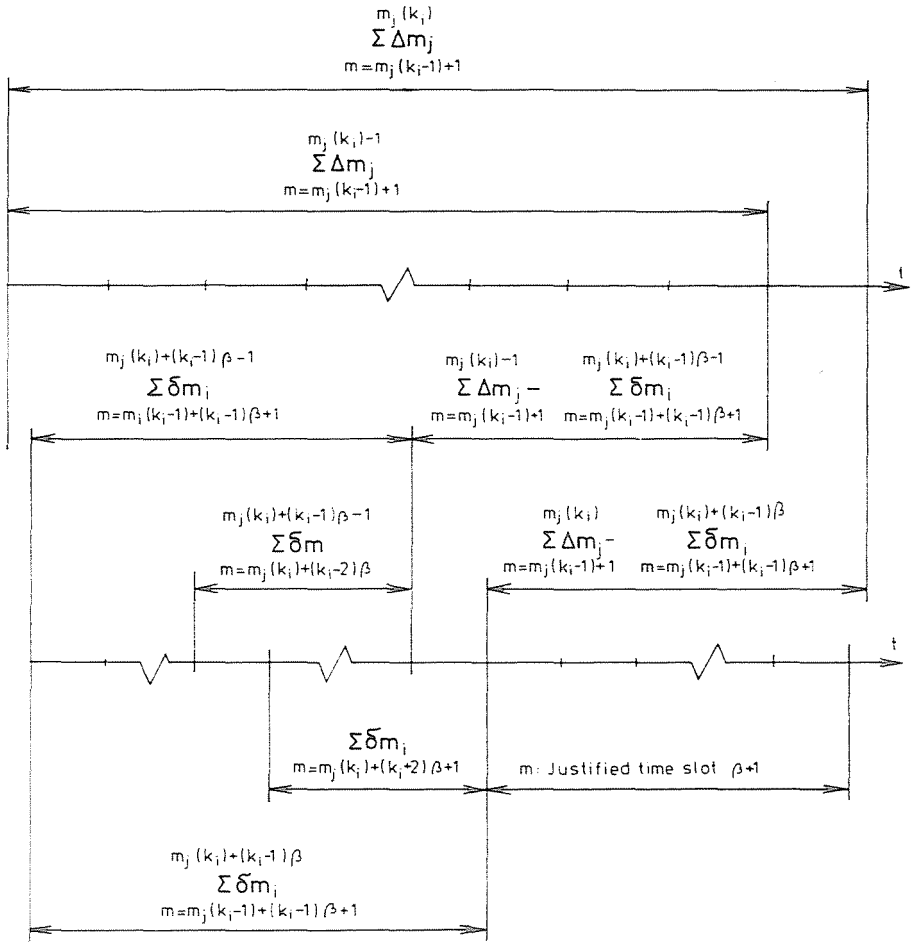

Fig. 1. Geometric representation of justification at ith DSC

It follows that the rth additional justified time slot will be inserted into the information pulse stream of the jth source at the $i+1$th DSC after the $m_j^+(r)$th information bit, if

$$\begin{cases} \sum_{m=m_j^+(r-1)+1}^{m_j^+(r)-1} \delta m_i - \sum_{m=m_j^+(r-1)+(r-1)\beta+1}^{m_j^+(r)+(r-1)\beta-1} \delta m_{i+1} < \sum_{m=m_j^+(r)+(r-2)\beta}^{m_j^+(r)+(r-1)\beta-1} \delta m_{i+1} \\ \sum_{m=m_j^+(r-1)+1}^{m_j^+(r)} \delta m_i - \sum_{m=m_j^+(r-1)+(r-1)\beta+1}^{m_j^+(r)+(r-1)\beta} \delta m_{i+1} \geq \sum_{m=m_j^+(r)+(r-2)\beta+1}^{m_j^+(r)+(r-1)\beta} \delta m_{i+1} \end{cases} \tag{5}$$

or a justified time slot inserted at the ith DSC will be eliminated for the sth time, if

$$\begin{cases} \sum\limits_{m=m_j^-(s-1)+1}^{m_j^-(s)-1} \delta m_{i+1} - \sum\limits_{m=m_j^-(s-1)-\beta+1}^{m_j^-(s)+(s-1)\beta-1} \delta m_i < \sum\limits_{m=m_j^-(s)-\beta}^{m_j^-(s)-1} \delta m_{i+1} \\ \sum\limits_{m=m_j^-(s-1)}^{m_j^-(s)} \delta m_{i+1} - \sum\limits_{m=m_j^-(s-1)-\beta+1}^{m_j^-(s)+(s-1)\beta} \delta m_i \geq \sum\limits_{m=m_j^-(s)-\beta+1}^{m_j^-(s)} \delta m_{i+1} \end{cases} \tag{6}$$

Under these conditions the l_sth justified time slot will be eliminated, if

$$m_i(l_s) > m_{i+1}(s) > m_i(l_s - 1). \tag{7}$$

If condition (3) holds for the following pairs of DSC, additional justified time slots would be inserted at every DSC and justification rate will grow. If we assume that condition (4) holds for the following pairs of DSC some justified time slots will be eliminated and justification rate will be lower. If the information transmitting route is accidental, the satisfaction of one of the two conditions (3) or (4) will be accidental and the justified time slots stream will be accidental.

Model of the random justified time slots stream

Consider digital information stream, which is transmitted via a chain of DSC's. We have to determine the justified time slots distribution at each DSC.

At the first DSC justified time slots will be inserted at the moments $m_1(k_i)$, $k_i = 1, 2, \ldots$, described by (2). In terms of the random branching processes [5] these time slots can be called first generation ones. At the second DSC in the digital information stream the second generation of justified time slots will appear. Thus in the digital information stream at the nth DSC the nth generation of justified time slots will be present. During transmission of digital information streams from the first to the second DSC being accidental transmitting route and accidental clock intervals, for every justified time slot of the first generation with probabilities $P_2(k)$, $k = 0, 1, 2, \ldots$ will be k justified time slots of the second generation. If we assume that these probabilities are identical for all generations of justified time slots we have a random branching process.

The above mentioned assumption cannot be exactly satisfied for justified time slots streams in plesiochronous digital networks. Taking into account, however, that:

(i) the maximal possible number of justified time slots increases together with the number of transit DSC,

(ii) clock intervals are independent,

(iii) the probability of inserting additional justified time slots depends only on the difference of the clock periods of the nth and $n+1$th DSC's allows

us to use a model of branching processes with an accuracy sufficient for practical purposes. By this model the location of justified time slots will be denoted by the set of time slots $t_1, t_2, \ldots$, and so the justified time slots stream at the nth DSC can be described by the moment-generating functional

$$\Phi_t^n(s)=\pi_0^n+\sum_{k=1}^{\infty}\int\ldots\int\pi_k^n(t_1^n,\ldots,t_k^n)e^{-s(t_1^n)-\ldots-s(t_k^n)}dt_1^n\ldots dt_k^n \tag{8}$$

where

$$\pi_k^n(t_1^n,\ldots,t_k^n)dt_1^n\ldots dt_k^n \tag{9}$$

is the probability of the appearance of k justified time slots in the intervals $(t_l^n, t_l^n + dt_l^n)$, $l=\overline{1,k}$ at the nth DSC; π_0^n — the probability of no justified time slots, $s(t)$ — a non-negative function. If the time slots $t_1, t_2, \ldots$ are independent of location of justified time slots at the first DSC the probability density $\pi_k^n(t_1^n,\ldots,t_k^n)$ can be represented by

$$\pi_k^n(t_1^n,\ldots,t_k^n)=P_n(k)\prod_{m=1}^{k}v_m^n(t) \tag{10}$$

where $P_n(k)$ denotes the probability of the appearance of k justified time slots at the nth DSC and $v_m^n(t)dt$ denotes the probability of the appearance of justified time slot in $(t, t+dt)$. The numerical values of $P_n(k)$ can be calculated by

$$P_n(k)=qA_n(k) \tag{11}$$

where $A_n(k)$ is a coefficient at s^k of the probability generating function, given by the following relation

$$f_{n+1}(s)=f_n[f(s)], \tag{12}$$

$f(s)$ is a probability generating function of the second generation

$$f(s)=f_2(s)=P_2(0)+P_2(1)s+P_2(2)s^2+\ldots, \tag{13}$$

s is a complex variable. Note that function $f(s)$ can be obtained by integration of (8) with $e^{-s(t)}$, $k=0,1,2\ldots$. Probabilities $P_2(k)$ for $k=0,1,2$ can be expressed as

$$\begin{aligned}
P_2(0)&=\frac{1}{\Delta-\delta}\int_{-\infty}^{\infty}\int_{-\infty}^{\delta_1}(\delta_1-\delta_2)w_\delta(\delta_1)w_\delta(\delta_2)d\delta_2 d\delta_1\\
P_2(2)&=\frac{1}{\Delta-\delta}\int_{-\infty}^{\infty}\int_{-\infty}^{\delta_2}(\delta_2-\delta_1)w_\delta(\delta_2)w_\delta(\delta_1)d\delta_1 d\delta_2\\
P_2(1)&=1-P_2(0)-P_2(2)
\end{aligned} \tag{14}$$

where Δ and δ represent the average of clock periods of sources and DSC's, respectively, and w_δ is the probability density of DSC clock period.

The averages Δ and δ in (14) permit us to obtain the average characteristics of justified time slots traffic in the average time interval between justified time slots. In many cases, the accuracy and stability of DSC clock intervals are higher than the accuracy and stability of source clock intervals. To take into account this fact we can state that at each DSC at most one additional justified time slot can be inserted into the digital information stream, i.e. $P_n(k) \neq 0$ if $0 \leq k \leq n$ and $P_n(k)=0$ otherwise. Thus, in (11) $k=\overline{0, n}$ and factors q_n can be obtained by the normalizing condition

$$q_n = \frac{1}{\sum_{k=0}^{n} A_n(k)}. \tag{15}$$

Table 1

Probability distribution of a number of justified time slots in average time interval between two justified time slots

$\Delta-\delta$	k \ n	2	3	4	5	6	7
$6\sigma_\delta$	0	0.092552	0.168899	0.232831	0.287298	0.334303	0.375312
	1	0.814896	0.678554	0.573979	0.492377	0.427368	0.374679
	2	0.092552	0.138575	0.159786	0.167540	0.167853	0.164056
	3		0.013972	0.029205	0.042018	0.051733	0.058630
	4			0.004199	0.009065	0.014292	0.019229
	5				0.001702	0.003605	0.005898
	6					0.000846	0.001718
	7						0.000478
$14\sigma_\delta$	0	0.040291	0.077406	0.111699	0.143490	0.173051	0.200607
	1	0.919418	0.848370	0.785264	0.729044	0.678721	0.633484
	2	0.040291	0.071239	0.094935	0.112982	0.126600	0.136725
	3		0.002985	0.007633	0.013094	0.018826	0.024497
	4			0.000469	0.001282	0.002476	0.003986
	5				0.000108	0.000294	0.000603
	6					0.000032	0.000086
	7						0.000012
$22\sigma_\delta$	0	0.025632	0.049968	0.073102	0.095123	0.116110	0.136136
	1	0.948736	0.901361	0.857452	0.816706	0.778821	0.743531
	2	0.025632	0.047424	0.065938	0.081650	0.094959	0.106204
	3		0.001247	0.003377	0.006115	0.009250	0.012621
	4			0.000131	0.000385	0.000794	0.001358
	5				0.000021	0.000062	0.000136
	6					0.000004	0.000013
	7						0.000001

As an example, in Table 1 calculated values of probabilities are represented when average values of differences between information sources and DSC clock intervals are $\Delta-\delta=6\sigma_\delta$, $\Delta-\delta=14\sigma_\delta$ and $\Delta-\delta=22\sigma_\delta$, where σ_δ is the standard deviation of a Gaussian random variable representing DSC clock intervals.

Probability distribution $v_m^n(t)$ in (10) represents relative detuning of sources and DSC clock intervals $v_m^n(t)=R=\dfrac{\Delta-\delta}{\delta}$. It follows that the average number of clock periods between series of k justified time slots at the jth DSC is given by

$$N_n(k)=\frac{\beta}{P_n(k)R^k}. \tag{16}$$

As an example in Fig. 2 numerical values of $N_4(k)$ are shown as a function of R when $\Delta-\delta=22\sigma_\delta$ and $\Delta-\delta=6\sigma_\delta$, $\beta=1$, probability density of clock intervals is Gaussian. These results may be used for determining parameters of jitter filtering equipments.

For designing of justification jitter filtering equipments of digital networks it is also very important to know the distribution of justification jitter caused by multiinserting and multiremoving justified time slots. To obtain this distribution is difficult because the insertion of justified time slots is a non-linear algorithm. The second difficulty lies in the representation of justification process which consists of an infinite set of separate justification realization, i.e. the process under consideration is not ergodic. However, a sufficiently good representation can be obtained under the assumption that the distribution of phase difference between input and output clock periods of every DSC is independent of the number of DSC's in the information transmitting route and

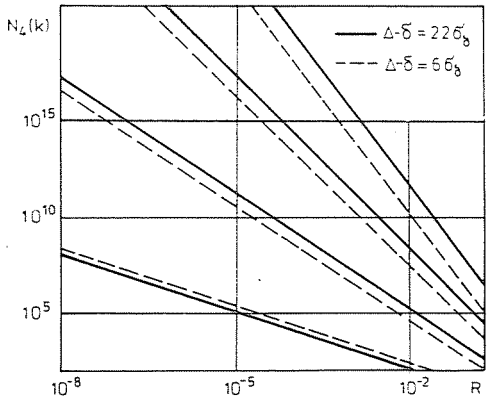

Fig. 2. Average number of clock periods between series of justified time slots

has a uniform distribution [6]. In this case the probability density of justification jitter in a DSC may be represented as a convolution of phase difference probability density

$$W_{\theta_l}(z) = \int_0^{l_\beta} W_{\Delta\varphi}(\psi) W_{\theta_{l-1}}(z-\psi) d\psi \tag{17}$$

where l is a number of DSC's in the information transmitting way. When l approaches ∞ jitter distribution law approaches the Gaussian one.

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