

# ON THE SIMULATION OF IC CHIP TEMPERATURE DISTRIBUTION

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## Summary

A new algorithm is found and a computer program developed for the more exact calculation of IC chip surface temperature distribution. The algorithm takes into account the effect of non-ideal (non-isotherm) heat-sink and the heat conductivity of bonding wires as well. The simulation is based on the fast Fourier-cosinus calculation method. The heat conducting effect of IC's environment is considered by linear calculation methods. The computer simulation is supported by measurements taken by liquid crystal.

The over-step of the usual isotherm heat-sink assumption is very important because the length to thickness ratio of chips is usually so great that the propagation of heat in the nonideal heat-sink can cause a significant influence in the temperature distribution on the top surface.

Bonding wires should be taken into consideration: the thermal resistance of bonding wires is high enough, but they are connected directly to the surface of the chip, so their influence becomes much more important.

Heat dissipation is considered as a two-dimensional function on the top surface, the generated heat-power leaves through the mounting and the bonding wires.

The top surface and the bottom rectangle of the chip are divided into  $N \times N$  and  $M \times M$  subrectangles, respectively, so the heat-power density and the temperature distributions can be written into hypervectors of  $N^2$  or  $M^2$  elements.

In our calculations the semiconductor chip (and the eventually present other layers) are treated as homogeneous, isotropic and linear materials.

The numerical procedures are based on the discrete, two-dimensional FFT method.

The perpendicular heat flow distribution on the top surface of the chip is given by the data of the power dissipations of circuit elements.

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On the bottom (mounted) rectangle the temperature distribution should be known because from these two distributions a conventionally-formed program segment (based on the well-known Fourier method<sup>1, 2, 3, 4, 5</sup>) can serve to calculate the top temperature distribution of multilayer chips.

### Computing the temperature distribution at the bottom

Let the hypervector of the heat flux density on the top surface be  $p$ . Let the hypervector of the heat flux density at the bottom of the chip be  $p^0$ , and the temperature vector be  $t^0$ .

In the first step  $t^0 \equiv 0$  is supposed. In this case  $p^0$  is the perpendicular heat flux density through the bottom rectangle, when the heat dissipation on the top surface is the actual  $p$ .

In the next step  $p \equiv 0$  is supposed. In this case  $p^0 = \mathbf{A}t^0$  can be written for any  $t^0$  distributions (because of the linearity).  $\mathbf{A}$  is the  $M^2 \times M^2$  thermal conductance hypermatrix of the chip from the bottom side. This characterizes the heat-conduction inside the chip.

Elements of  $p^0$  and  $\mathbf{A}$  are computed by FFT from the actual heat dissipation distribution on the top rectangle and from more supposed temperature distributions on the bottom rectangle of the chip.

Generally, when  $p \neq 0$  and  $t^0 \neq 0$ , then

$$p^0 = \mathbf{A}t^0 + p^0 \quad (1)$$

for the bottom side of the chip.

To get the  $t^0$  distribution, the chip side of the mount should be taken into account, too.

The mount is considered as a thermal multi-port with  $M^2$  ports. The locations of these ports are determined by the  $M \times M$  subrectangles at the bottom side of the chip. For further computation the  $M^2 \times M^2$  thermal conductance matrix of this multi-port should be determined. In our model this matrix is treated as the sum of a diagonal part  $\mathbf{D}$  and a symmetrical, singular part  $\mathbf{B}$ . The elements of the diagonal part are originated simply from the mount-to-ambient thermal conductance (divided by  $M^2$ ) while the elements of the symmetrical part (the transconductances) describe the thermal couplings between the different ports (different points) of the mount. The latter elements are calculated by the solution of the Laplace equation for the actual near-chip mount geometry (e.g. for a plate with finite thickness). With these matrixes

$$p^0 = [\mathbf{B} + \mathbf{D}]t^0 \quad (2)$$

(1) and (2) give the third set of equations:

$$[\mathbf{B} + \mathbf{D} - \mathbf{A}]t^0 = p_0^0 \quad (3)$$

From (3) the  $t^0$  distribution is given.

In the formulas above the raster-density on the bottom rectangle (M) can be much smaller than the raster-density on the top rectangle (N). So computing has become much faster. The corresponding resolution loss at the bottom surface is tolerable because the fineness of heat dissipation distribution on the top rectangle is already not perceptible at the bottom heat flux distribution.

### The influence of the bonding wires

The contact pads are considered now as ports of a linear thermal network. The  $k$ -element vector of the input heat-flow is  $p_w$  ( $k$  is the number of contact pads).  $t_w^0$  contains the temperatures of the pads when the bonding wires are disconnected.  $C_w$  is a thermal transfer impedance matrix which characterizes the thermal interactions among the contact pads inside the chip. This matrix can be calculated in the following way: when a unit heat flux flows through the contact pad  $j$ , the temperature of contact pad  $i$  is increasing with  $C_{ij}$ .  $C$  is computed by the program described in the previous paragraph. In the case of any symmetries of the contact pad locations only a reduced number of solutions is needed due to the corresponding symmetries in  $C$ .

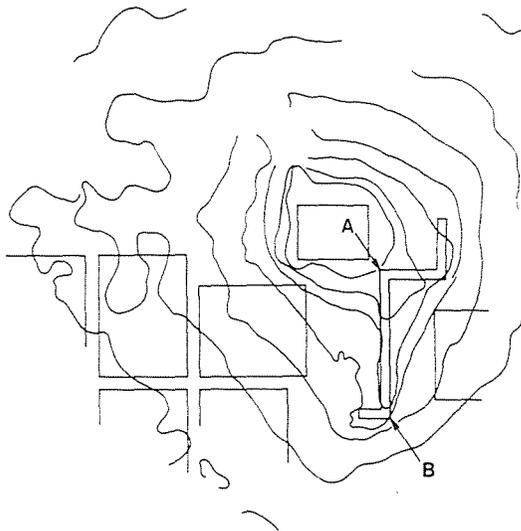


Fig. 1. Measured isotherms and schematic layout of the chip

Let  $Y_w$  be the heat conductance diagonal matrix of the bonding wires. We can get an equation like in the case of (3):

$$[E + Y_w C_w] p_w = -Y_w t_w^0 \quad (4)$$

where  $E$  is the unit matrix. Solving this set of equations for  $p_w$ , an element of the  $p_w$  vector with its minus sign gives a virtual heat-source, so it can be taken into account in the model according to the previous paragraph<sup>4,5</sup>.

A computer program has been developed on the basis of the considerations above. The resolution is  $N = 128$  on the top rectangle, and  $M = 8$  at the bottom.

Both the model and the program have been verified by different measurements.

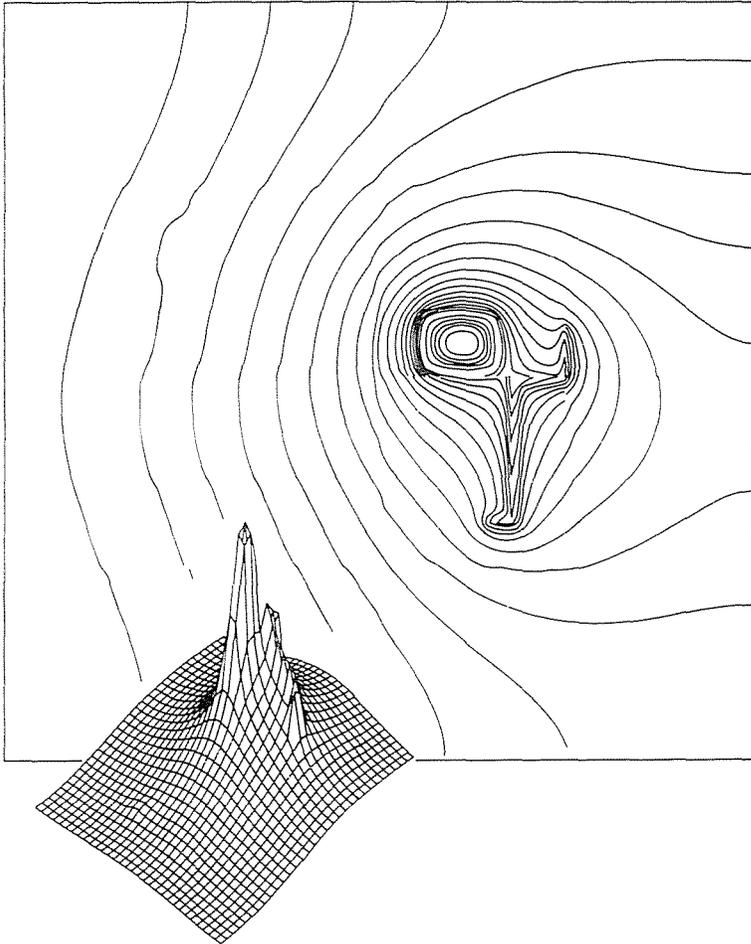


Fig. 2. The computed isotherms

## Verification with nematic liquid crystal measurements

The isothermas of a working opamp chip could be traced under changing environment temperature by determining the boundary of the phase-change of the nematic liquid crystals<sup>6</sup>.

The measured thermal map is seen in Fig. 1, and the computed one in Fig. 2. The temperature-difference between points **A** and **B** (Figure 1) is  $17.88 - 16.41 = 1.47$  °C by measurement, and  $17.97 - 16.33 = 1.64$  °C by computing (at 0 °C supposed ambient temperature).

The difference between measurement and computing is within the margin of the measurement error.

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