A STRAY-INSENSITIVE SWITCHED-CAPACITOR DELAY CIRCUIT

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Summary

A circuit configuration is introduced for two-phase clocked delay and summing units with reduced sensitivity to stray capacitance spread. An example of a three-point running DFT processor circuit is given.

Introduction

Most of the known SC delay circuits seem to be very complicated for practical purposes requiring either two operational amplifiers for one stage [1] or a multi-phase clocking scheme [2]. Another two-phase clocked solution with one operational amplifier [3] suffers from being sensitive to top-plate parasitic capacitance tolerances. Starting from the latter configuration a modified structure is introduced. The main goal of the present contribution is to get a circuitry less sensitive to parasitic capacitance spread for applications in delay and weighted summing stages.

Improving the sensitivity properties

The first version of a two-phase *SC* subcircuit is illustrated in Fig. 1. C_1 is the integrating capacitor. C_2 is charged to a voltage equal to v_{out} in phase 2. For $C_2 = C_1$ (i.e. the relative error value Δ is zero) the charge sample on C_1 preceding the last one is compensated in the next phase 1 resulting in a zero output component by recharging C_2. On the other hand the new charges $q_{in}(z)$ entering the system in phase 1 and 2 are summed and disappear in the next cycle from the stage involved. The last sample should be saved or processed before the charge representing that sample is compensated. From a theoretical point of view the circuit in Fig. 1 seems to be a suitable unit delay element.

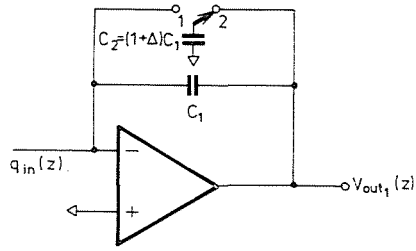

Fig. 1. Basic two-phase delay circuit

However the relative top-plate parasitic capacitance spread of C_2 causes an error represented by the relative error parameter Δ. With proper dimensioning of the nominal capacitance values the sign of Δ in a realized stage may be positive as well as negative.

$$v_{\text{out}}(z) = \frac{1}{C_1} q_{\text{in}}(z) \cdot z^{-1}. \tag{1}$$

As $q_{\text{in}}(z)$ enters the stage by coupling capacitors, the properties of the stage depend on ratios of capacitances. However, for a finite value of Δ

$$v_{\text{out1}}(z) \cdot (1 - \Delta \cdot z^{-1}) = \frac{1}{C_1} q_{\text{in}}(z) z^{-1} \tag{2}$$

i.e. the intended finite memory delay element changes into an infinite impulse response unit. As the top-plate parasitic capacitance has a wide spreading range the structure of Fig. 1 is not good for practical applications. If the value of Δ for the different stages on a given chip has a wide spread the method of determining the pole and zero shifts in the z-plane for a given constant value of Δ [4] is not feasible. On the other hand, even if the value of Δ on a given chip can be considered essentially constant (i.e. correlated tolerances) the method of [4] can be applied for analysis purposes only, because the value of Δ for a chosen chip sample is stochastic in nature. As the top-plate capacitance spread (relative to the "main" capacitance level) is determined by the technology applied we try to find a solution to reduce the effect caused by it. Reducing the coefficient of the error term (corresponding to Δ in Eq. (2)) results in a response closer to the parasitic-free ideal case.

Let the structure be extended according to Fig. 2. In this case the new information sample (charge) should enter the stage at the beginning of phase 1.

The error is represented by the relative error parameter of C_3, Δ. The top-plate capacitance spread of C_3 is supposed to be the dominant source of error. Equation (2) should be modified yielding

$$v_{\text{out2}}(z) \cdot \left(1 - \frac{\Delta}{\alpha} z^{-1}\right) = \frac{1}{C_1} q_{\text{in}}(z) z^{-1}. \tag{3}$$

Increasing the value of α results in decreasing error coefficients in the left-hand side of Equation (3). Supposing that the (nominally equal) capacitors C_1/α and C_3 are chosen to be unit capacitors the total capacitance involved is $(1+\alpha)$; e.g. for $\alpha = 10$ the summed value is 11. If C_1 and C_2 in Fig. 1 are of unit values the total capacitance is 2. The circuitry presented in Fig. 2 compared to that of Fig.

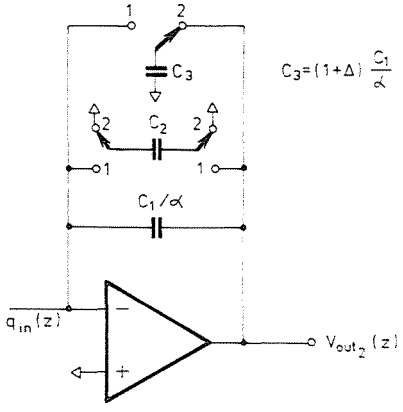

Fig. 2. Improved delay circuit schematic

1 is more complex (four switching transistors and one capacitor should be added) and the summed capacitor value is higher as well. The price paid is, however, converted into the reduced influence of the top-plate capacitance value spread. The relative stray capacitance uncertainty error Δ and the application dependent allowable error coefficient Δ/α are to be considered for choosing the value of α.

An example

The charge input of each delay unit of a circuit may be used as a weighted inverting and/or non-inverting summing point. Recursive and non-recursive circuits may also be implemented. Figure 3 shows a unit delay or summing element with $\alpha = 10$. As a system illustration a three-point running DFT processor is given in Fig. 4. The unit elements are as in Fig. 3 and are represented here by boxes for simplicity. The position of the switches in Fig. 4 corresponds to phase 2.

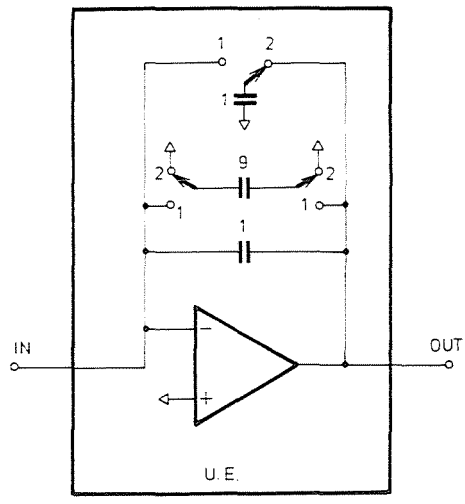

Fig. 3. Unit element ($\alpha = 10$)

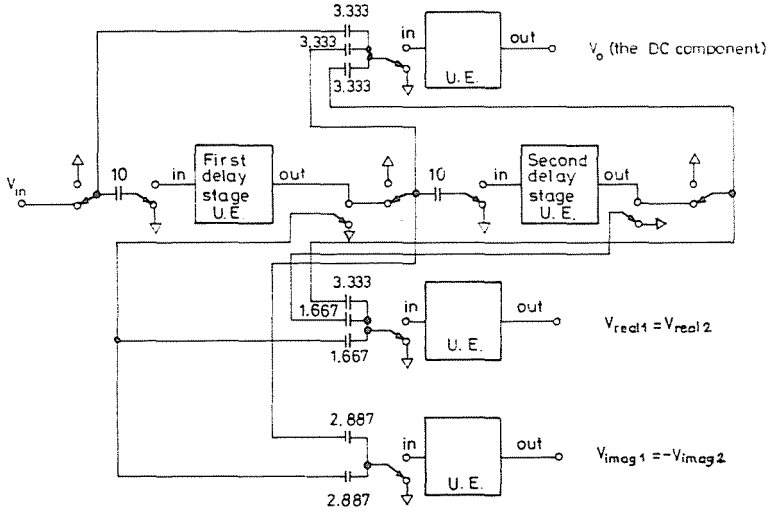

Fig. 4. Three-point DFT processor circuit

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