AMPLIFIER SLEW RATE AND FREQUENCY DEPENDENT GAIN EFFECTS IN SWITCHED-CAPACITOR CIRCUITS

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Summary

The transient behaviour of the MOS SC integrators containing a two-stage pole-splitting compensated op amp is analyzed. A nonlinear two-pole op amp model is used in the analysis. Analytical expressions for the SC integrator response and settling time are derived. A design example is given where these results are used to minimize the integrator settling time.

Introduction

Active switched-capacitor (SC) circuits process signals by delaying and transforming charge sequences. Op amps are used in these circuits to force charges from one capacitor into another one. Op amps are operated in impulse mode and the accuracy of their output voltages at the end of clock phases is the key factor. In MOS monolithic integrated circuits the accuracy of these samples is limited by the finite and frequency dependent gain of op amps and by their finite slew-rate.

The effect of the finite op amp gain and band-width in SC filters was investigated by several authors [1], [2], [3]. In these works a linear op amp model having a single dominant-pole transfer function was assumed and the effect of the slew rate limitation was not taken into account.

In audio-range MOS SC filters two-stage pole-splitting compensated op amps are commonly used (Fig. 1). If we want to know the exact operation of a SC circuit where such an amplifier is used a more elaborated op amp model must be applied. A second-order (two-pole) transfer function has to be considered and above a certain signal level the finite slew rate—resulting from the limited available current of the input stage to charge the compensation capacitor—has to be taken into account, too.

This paper deals with the transient and settling behaviour of the basic integrators used in most SC filters. According to the requirements mentioned

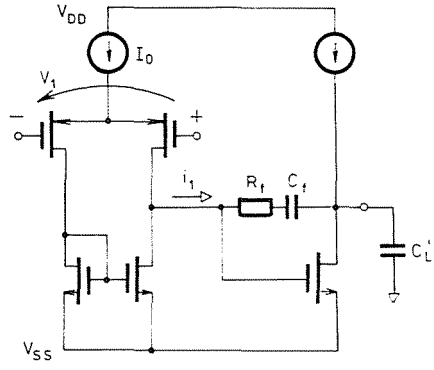

Fig. 1. CMOS two-stage op amp

above a nonlinear two-pole op amp model is applied. The detailed time-domain analysis results in analytical expressions for the SC integrator response and settling time. To illustrate the practical usefulness of the results a design example is given where the integrator settling time is minimized by the proper choice of the compensation capacitor.

Op amp model for transient analysis

If small signal operation is assumed the linear equivalent circuit of the two-stage op amp can be applied as illustrated in Fig. 2 [4]. The transfer function is the following

$$\frac{V_0(s)}{V_1(s)} = \frac{A_0(1-s/\omega_z)}{(1+s/\omega_1)(1+s/\omega_2)} \tag{1}$$

where

$$A_0 = g_{m1}g_{m2}R_1 \cdot R_2, \qquad \omega_z = [C_f(1/g_{m2} - R_f)]^{-1} \tag{2}$$

$$\omega_1 \cong g_{m1}/A_0 C_f, \qquad \omega_2 \cong g_{m2}/C_L \quad \text{if} \quad C_f, C_L \gg C_1 \tag{3}$$

and the gain-bandwidth product is $\omega_u = g_{m1}/C_f$. If R_f is chosen to be equal to $1/g_{m2}$, then the zero in the right half plane is eliminated. The Y_0 admittance of the model is

$$Y_0^*(s) = \frac{g_{m2}R_1}{R_1+R_f}\,\frac{s/\omega_0}{1+s/\omega_0} + sC_f\,\frac{1}{1+s/\omega_0} = G_0^*(s) + sC_0^*(s) \tag{4}$$

where

$$\omega_o = [C_f(R_1+R_f)]^{-1} \cong \omega_u/(g_{m1}R_1) \qquad \text{if} \quad R_1 \gg R_f \tag{5}$$

As it will be shown later, the accuracy of the op amp model is most critical

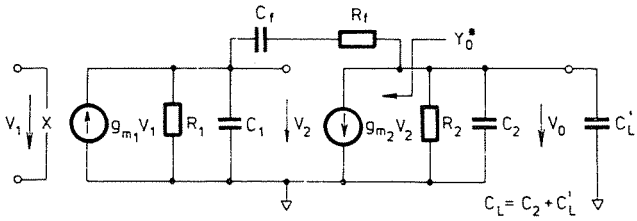

Fig. 2. Small-signal equivalent circuit

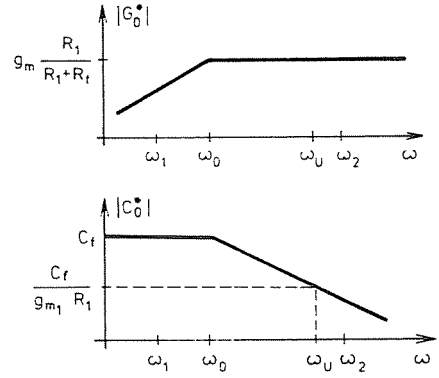

Fig. 3. Y_0^* admittance versus frequency

around $\omega_2/2$. In amplifiers compensated for a phase margin of about 60° $\omega_2/2 \cong \omega_u$, thus (5) yields $\omega_2/2 \cong g_{m1} R_1 \omega_0$. Figure 3 shows G_0^* and C_0^* versus frequency. Around $\omega_2/2$.

$$C_0^* \ll C_L \qquad \text{and} \qquad G_0^* \cong g_{m2} \gg 1/R_2 \tag{6}$$

therefore the output admittance of the amplifier will be approximated by g_{m2}.

If a large voltage step is applied to the input of the amplifier, then the current of the input stage becomes limited to I_0 and the linear model is not adequate any more. Therefore, the input stage will be modelled by a piecewise linearized approximation of its nonlinear transfer function.

Transient analysis

The *SC* integrator model used in transient calculations is shown in Fig. 4. The position of the switches in the noninverting configuration are shown in brackets. The basic physical operation of the inverting and noninverting integrators are the same and it can be described by two phases periodically following each other

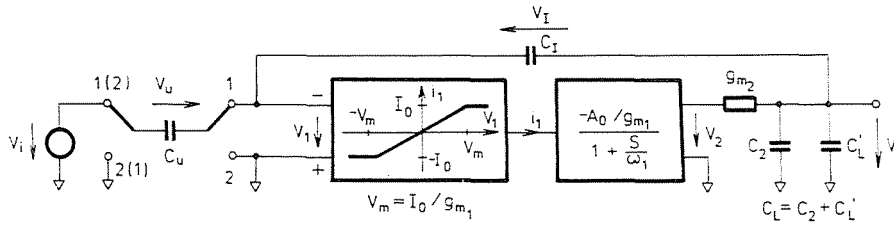

Fig. 4. SC integrator model for transient analysis

1. Charge transfer, when the charge of C_u is transported to C_I
2. Hold, when C_u is disconnected from the op amp input.

In the following, only the inverting integrator will be analyzed but the result can be applied to the noninverting circuit, too.

In the interval $t<0$ the input signal is zero and all the capacitors in the circuit contain zero charge. Let $t=0$ be the instant when the switches turn into their 1 position and at this moment an input step of magnitude V_i is applied

$$v_i(t)=V_i \qquad t\geq 0 \tag{7}$$

Charge transfer interval $0<t\leq T/2$

The elements v_i, C_u, C_I, C_L form a loop. It is assumed that after switching, the capacitors are charged instantaneously, while v_2 cannot change abruptly. In reality, the current in the loop is limited by the finite switch resistances (R_{0n}). It is easy to show, however, that v_1 approaches UV_i exponentially with a time constant $2R_{0n}C_u \ll 1/\omega_2$. This process requires only a very small fraction of the time interval of interest thus the voltages can be assumed to be step functions

$$v_1(t=+0)=\frac{C_u}{C_u+C_I\times C_L}V_i=UV_i \tag{8}$$

$$v_I(t=+0)=\frac{C_u\times C_L}{C_I+C_u\times C_L}V_i=IV_i \tag{9}$$

$$v_0(t=+0)=\frac{C_u\times C_I}{C_L+C_u\times C_I}V_i=LV_i \tag{10}$$

$$v_2(t=+0)=0 \tag{11}$$

The network can be described by the following equations

$$v_u(t)=v_i(t)-v_1(t) \tag{12}$$

$$C_I[v_I(t)-v_I(t=t_i)]+C_u[v_u(t)-v_u(t=t_i)]=0 \tag{13}$$

Using eq. (7) and (12) eq. (13) can be rewritten

$$C_I[v_I(t)-v_I(t=t_i)]=C_u[v_1(t)-v_1(t=t_i)] \tag{14}$$

$$v_0(t)=v_1(t)+v_I(t) \tag{15}$$

$$g_{m2}[v_2(t)-v_0(t)]-C_L\frac{dv_0(t)}{dt}-\frac{dv_I(t)}{dt}C_I=0 \tag{16}$$

$$i_1(t)=-\frac{g_{m1}}{A_0}v_2(t)-\frac{g_{m1}}{A_0\omega_1}\frac{dv_2(t)}{dt} \tag{17}$$

Here and throughout the paper, t_i denotes the initial instant of the process.

The transient must be analyzed in two cases depending upon whether $v_1(t=+0)=UV_i$ is larger or smaller than the threshold I_0/g_{m1}.

(i) $UV_i>I_0/g_{m1}$

A) slewing period

After switching on the current of the input stage jumps to a value I_0 and stays there for a while

$$i_1(t)=I_0 \qquad t>0. \tag{18}$$

The set of differential equations (14)...(17) and (18) can be solved for every node voltage with the initial conditions at $t_i=+0$. The output voltage will be the following

$$v_0(t)=-\frac{I_0A_0}{g_{m1}}\left[1-\frac{\omega_2^*}{\omega_2^*-\omega_1}e^{-\omega_1 t}+\frac{\omega_1}{\omega_2^*-\omega_1}e^{-\omega_2^* t}\right]+LV_ie^{-\omega_2^* t} \tag{19}$$

where

$$\omega_2^*=g_{m2}/(C_L+C_U\times C_I). \tag{20}$$

Taking into account that $\omega_2^*\gg\omega_1$ we obtain

$$v_0(t)\cong\frac{-I_0A_0}{g_{m1}}(1-e^{-\omega_1 t})+LV_ie^{-\omega_2^* t}. \tag{21}$$

The first term represents the slew limited rise of the output signal, the second fast-decaying one comes from the direct feed-through. The slew limited period lasts until the input signal reaches the threshold I_0/g_{m1}. The time when this occurs will be denoted by T_s.

$$v_1(t=T_s)=I_0/g_{m1}. \tag{22}$$

Substitution of the expression for $v_1(t=T_s)$ yields an implicit exponential equation

$$\frac{I_0}{g_{m1}} = UV_i - \frac{kI_0A_0}{g_{m1}}\left[1 - \frac{\omega_2^*}{\omega_2^* - \omega_1}e^{-\omega_1 T_s} + \right.$$
$$\left. + \frac{\omega_1}{\omega_2^* - \omega_1}e^{-\omega_2^* T_s}\right] - kLV_i(1 - e^{-\omega_2^* T_s}) \tag{23}$$

where $k = C_u/(C_u + C_I)$

T_s can be computed from this equation.

B) Linear region

For $t > T_s$ the circuit operates in its linear region, where the current of the first stage is proportional to its input voltage

$$i_1(t) = g_{m1}v_1(t) \qquad t > T_s. \tag{24}$$

The set of differential equations (14)...(17) and (24) must be solved for $v_0(t)$, $v_I(t)$ and $v_2(t)$ with the initial values corresponding to $t_i = T_s$. The nature of the voltage waveforms are determined by the damping factor ξ of the second order linear feedback system.

$$\xi_1 = \frac{\omega_1 + \omega_2^*}{2[(1 + A_0k)\omega_1\omega_2^*]^{1/2}}. \tag{25}$$

Assuming that $A_0k \gg 1$ and $\omega_2^* \gg \omega_1$, after substitution we obtain

$$\xi_1 \cong \frac{1}{2}\left[\frac{g_{m2}}{g_{m1}}\left(1 + \frac{C_u}{C_I}\right)\frac{C_f}{C_L + C_u \times C_I}\right]. \tag{26}$$

It can be readily shown that for practical MOS op amp and SC filters $\xi_1 < 1$, that is, an underdamped transient having overshoot and ringing will occur. The output voltage can be written as

$$v_0(t) = -\alpha V_i\frac{A_0k}{1 + A_0k}\left\{1 - \frac{K_{01}}{\sqrt{1 - \xi_1^2}}\sin\left[\omega_{n1}\sqrt{1 - \xi_1^2}\cdot\right.\right.$$
$$\left.\left.\cdot(t - t_i) + \beta_{01}\right]e^{-\frac{\omega_1 + \omega_2^*}{2}(t - t_i)}\right\} \qquad t > t_i \tag{27}$$

where

$$\alpha = C_u/C_I, \qquad \omega_{n1} = \sqrt{(1 + A_0k)\omega_1\omega_2^*} \tag{28}$$

$$K_{01} = \frac{1 + A_0k}{A_0k}\frac{v_0(t = t_i)}{\alpha V_i}(X_{01}^2 + Y_{01}^2)^{1/2} \tag{29}$$

$$\beta_{01} = \operatorname{arctg} \frac{Y_{01}}{X_{01}} + \operatorname{arctg} \frac{\sqrt{1-\xi_1^2}}{\xi_1} \tag{30}$$

$$X_{01} = 1 - 2\xi_1^2 + \xi_1 \left[\frac{\omega_1}{\omega_{n1}} + \frac{v_2(t=t_i)}{v_0(t=t_i)} \frac{\omega_2^*}{\omega_{n1}} \right] + \frac{A_0 k}{1 + A_0 k} \frac{\alpha V_i}{v_0(t=t_i)} \tag{31}$$

$$Y_{01} = \sqrt{1-\xi_1^2} \frac{\omega_2^*}{\omega_{n1}} \left[1 - \frac{v_2(t=t_i)}{v_0(t=t_i)} \right]. \tag{32}$$

Now $t_i = T_s$ has to be substituted in eq. (27). A typical transient of a SC integrator in the charge transfer period is shown in Fig. 5. Settling time can be approximated by the time after which overshoot will be less than the settling error E_{set}. The length of the linear transient T_{SL} can be computed from eq. (27)

$$T_{SL} = \frac{2}{\omega_1 + \omega_2^*} \left\{ \ln \left[\frac{100}{E_{set}[\%]} \frac{K_{01}}{\sqrt{1-\xi_1^2}} \cdot \sin \left(\operatorname{arctg} \frac{\sqrt{1-\xi_1^2}}{\xi_1} \right) \right] + \operatorname{arctg} \frac{\sqrt{1-\xi_1^2}}{\xi_1} \right\}. \tag{33}$$

Total settling time will be

$$T_{set} = T_s + T_{SL}. \tag{34}$$

(ii) $UV_i < I_0/g_{m1}$.

In this case the whole charge transfer transient takes place in the linear network. Eq. (27) describes correctly the whole process with the substitution $t_i = +0$. Now the total settling time is given by eq. (33) as

$$T_{set} = T_{SL}. \tag{35}$$

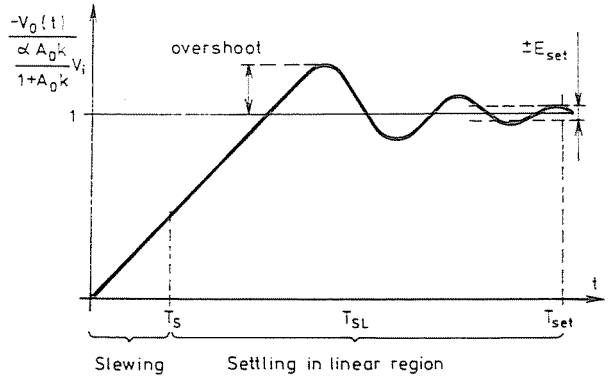

Fig. 5. Typical underdamped transient of a SC integrator during charge transfer

Hold interval $T/2 < t \leq T$

It is assumed that at the instant of switching the circuit is operating in its linear region. The following equations will describe the operation

$$v_I(t) = v_I(T/2) \tag{36}$$

$$v_0(t) = v_I(T/2) + v_1(t) \tag{37}$$

$$g_{m2}[v_2(t) - v_0(t)] - C_L \frac{\mathrm{d}v_0(t)}{\mathrm{d}t} = 0 \tag{38}$$

$$i_1(t) = -\frac{g_{m1}}{A_0} v_2(t) - \frac{g_{m1}}{A_0 \omega_1} \frac{\mathrm{d}v_2(t)}{\mathrm{d}t} \tag{39}$$

$$i_1(t) = g_{m1} v_1(t). \tag{40}$$

This set of differential equations has to be solved for $v_0(t)$. The node voltages at the end of the charge transfer period $t = T/2$ give the required initial conditions. Damping factor in this period will be the following

$$\xi_2 = \frac{\omega_1 + \omega_2}{2\sqrt{(1 + A_0)\omega_1 \omega_2}} \cong \frac{1}{2}\left[\frac{g_{m2}}{g_{m1}} \frac{C_f}{C_L}\right]^{1/2}. \tag{41}$$

if $A_0 \gg 1$, $\omega_2 \gg \omega_1$.

For practical MOS op amps $\xi_2 < 1$. The output voltage can be written

$$v_0(t) = v_I(T/2) \frac{A_0}{1 + A_0} \left\{1 + \frac{K_{02}}{\sqrt{1 - \xi_2^2}} \cdot \sin\left[\omega_{n2} \cdot \right.\right.$$

$$\left.\left. \cdot \sqrt{1 - \xi_2^2}(t - T/2) + \beta_{02}\right] \exp\left[-\left(\frac{\omega_1 + \omega_2}{2}\right)(t - T/2)\right]\right\} \tag{42}$$

where

$$t > T/2; \qquad \omega_{n2} = \sqrt{(1 + A_0)\omega_1 \omega_2} \tag{43}$$

$$K_{02} = \frac{1 + A_0}{A_0} \frac{v_0(T/2)}{v_I(T/2)} (X_{02}^2 + Y_{02}^2)^{1/2}. \tag{44}$$

$$\beta_{02} = \operatorname{arctg} \frac{Y_{02}}{X_{02}} + \operatorname{arctg} \frac{\sqrt{1 - \xi_2^2}}{\xi_2} \tag{45}$$

$$Y_{02} = \sqrt{1 - \xi_2^2} \frac{\omega_2}{\omega_{n2}} \left[1 - \frac{v_2(T/2)}{v_0(T/2)}\right] \tag{46}$$

$$X_{02} = 1 - 2\xi_2^2 + \xi_2 \left(\frac{\omega_1}{\omega_{n2}} + \frac{v_2(T/2)}{v_0(T/2)} \frac{\omega_2}{\omega_{n2}}\right) - \frac{A_0}{1 + A_0} \frac{v_I(T/2)}{v_n(T/2)}. \tag{47}$$

As could be expected, the output voltage will approach that of C_I in an underdamped fashion. The settling accuracy of the output voltage will improve but it cannot be better than that of $v_I(T/2)$.

Application example

The settling time of the SC integrator is a nonlinear function of the compensation capacitor C_f. It means that there must be an optimum value of C_f where the settling time is minimum. This will be illustrated in the following example.

The parameters of the circuit are

$$I_0 = 9\ \mu A, \quad g_{m1} = 20\ \mu S, \quad g_{m2} = 60\ \mu S, \quad A_0 = 10^4,$$

$$C_L = 5\ pF, \quad C_U = 1\ pF, \quad C_I = 5\ pF, \quad I_0/g_{m1}\,U = 1{,}575\ V.$$

The transient response of the SC integrator was computed with four different values of the input step V_i, while C_f is varied from 1 to 5 pF. The slewing period and the 0,1% settling time are given in Table I.

Table I

V_i [v]	C_f [pF]	T_s [μsec]	T_{set} [μsec]
3.5	1	0.1	1.598
	2	0.136	1.633
	3	0.163	1.666
	4	0.187	1.533
	5	0.207	2.034
2.5	1	0.063	1.558
	2	0.081	1.583
	3	0.092	1.596
	4	0.101	1.454
	5	0.108	1.934
2	1	0.037	1.528
	2	0.045	1.611
	3	0.049	1.629
	4	0.052	1.403
	5	0.055	1.991
1	1	—	1.535
	2	—	1.560
	3	—	1.579
	4	—	1.344
	5	—	1.931

An optimum value of $C_f = 4$ pF can be found in every cases.

Conclusion

The transient analysis of the SC integrators applying nonlinear two-pole op amp model has been presented. It has been shown that slew-rate limitation occurs if the integrator input voltage is larger than $I_0/g_{m1}\,U$. In the linear region the integrator output approaches its final value in an underdamped fashion that is with overshoot and ringing. The exact time functions for the slew-limited and the linear-period during charge transfer are given by Eq. (19) and (27). Hold mode transient given by Eq. (42) shows that the settling accuracy of the integrator is formed in the charge transfer interval. Analytic expressions for the *SC* integrator settling time are presented. These results can be used in circuit design, e.g. for choosing the proper value of the compensation capacitors to minimize the settling time (error) of every integrator in the SC filter.

If the whole transient takes place in the linear region, theoretically it does not meet any difficulties to extend the time domain analysis for periodic operation. From the sequence of the output voltage the *z*- and frequency-domain transfer functions of the SC integrator can be derived. These calculations are straightforward but are expected to be extremely lengthy.

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