THE COMPENSATION OF AMPLIFIER OFFSET AND FINITE-GAIN EFFECTS IN SWITCHED-CAPACITOR CIRCUITS*

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Summary

Among several nonideal effects which affect the performance of switched-capacitor (SC) filters, amplifier imperfections play an important role. With the tendency towards the use of SC techniques in video applications, these effects become increasingly serious, since the required fast amplifier circuits often have a low gain and a large systematic offset. This is the case, e.g., when a single inverter stage is used, instead of a multi-stage operational amplifier, in the SC integrators. The purpose of this paper is to overview some recently developed methods for eliminating (or at least drastically reducing) offset and finite-gain effects in SC circuits.

The input-referred dc offset voltage V_{os} of an amplifier is defined as the input voltage required to set the output voltage to zero. The offset condition $V_{os} \neq 0$ may be caused by *systematic* causes, such as improper biasing conditions or the deliberate use in high-frequency applications of inherently level-shifting amplifier circuits, such as inverters. Nonzero offset is also caused by *random* effects, such as matching errors, threshold voltage variations, etc. Systematic offset errors can have any magnitude, up to several volts large; random errors typically cause $V_{os} = 5 \sim 20$ mV input referred offset.

The presence of dc offset is especially detrimental to the operation of *voltage comparators*. These are basically high-gain amplifiers operated in an open-loop configuration, and used to compare two input voltages (one of which is often zero). These circuits are important components of the commonly used digital-to-analog (D/A) and analog-to-digital (A/D) converters. In such applications, the comparison accuracy required is typically of the order of 1 mV, and hence the effective value of V_{os} must be reduced to achieve adequate accuracy. An effective and commonly used method for this is *autozeroing* (Fig. 1). In this arrangement [1], during the time interval illustrated, the output voltage is $v_{out} = V_{os}(1 + 1/A) \cong V_{os}$, and hence C is also charged to $v_C = V_{os}$. In the next time interval, S_1 connects v_C in series with v_{in}, and S_2 opens. Then, the

* Dedicated to Professor Károly Simonyi on the occasion of his Seventieth Birthday

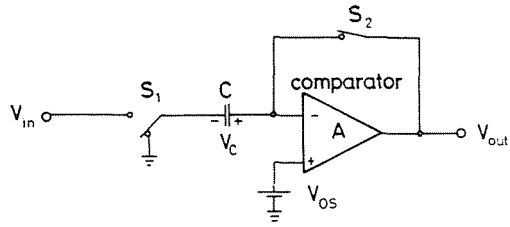

Fig. 1. An autozeroed SC comparator

comparator output will be $v_{out}=A(V_{os}-v_{in}-v_C)=-Av_{in}$. Thus, V_{os} is cancelled by this arrangement, and v_{out} will depend only on v_{in}, as required.

In a multistage comparator, the feedback represented by S_2 may lead to instability. To avoid this, each stage may be autozeroed separately (Fig. 2). In this circuit, all stages are first autozeroed simultaneously, with the input capacitance C_1 grounded. Then S_1 opens, causing some clock feedthrough charges to enter C_1 and hence changing V_1 somewhat. This shift in V_1 causes C_2 to recharge and hence to absorb this change. Next, S_2 opens, and its clock feedthrough effect is absorbed by C_3, etc. Finally, S_0 changes position and the comparator evaluates the polarity of v_{in} with the offset and clock feedthrough effects largely cancelled by the described autozeroing process. If, as is usual, the stages shown in Fig. 2 are simple inverters, then the switches $S_1, S_2, \ldots$ can

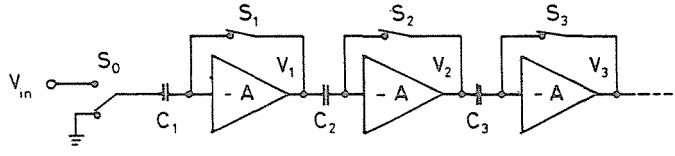

Fig. 2. A multistage SC comparator

also be used to provide nearly optimal biasing conditions for each stage [1]. The described arrangement can also be implemented using differential circuits, in which case power supply noise, clock feedthrough effects, etc. will also be approximately cancelled. This autozeroing technique can also be extended to continuous-time signal processing, by using *two* identical SC circuits which take turns in performing the autozeroing and signal processing tasks.

The autozeroing principles described can also be extended to SC amplifiers and filter stages. As an illustration, Fig. 3a shows an offset-compensated SC amplifier [2]. During the interval when $\Phi_1=1$, the capacitor C_1 is charged to $V_{os}-v_{in}$, while C_2 to V_{os}. During the $\Phi_2=1$ interval, C_1 charges to V_{os} and C_2 to $V_{os}-v_{out}$. Charge conservation then results in

$v_{out}=(C_1/C_2)v_{in}$, independently of V_{os}. During $\Phi_1=1$, however, $v_{out}=V_{os}$, and hence the output has the waveform shown in Fig. 3b. The same principle holds for inverting amplifiers (Fig. 4) and for delay circuits (Fig. 5). The dc offset compensation also reduces the noise near dc and all even harmonic of the clock frequency f_c. The scheme is also applicable to D/A stages based on the circuits of Fig. 3& 4, and to SC integrators [2]. In the latter case, C_2 is open-circuited during the $\Phi_1=1$ interval.

A major disadvantage of the offset compensation method illustrated in Fig. 3–5 is that the output voltage v_{out} is forced to slew back and forth between

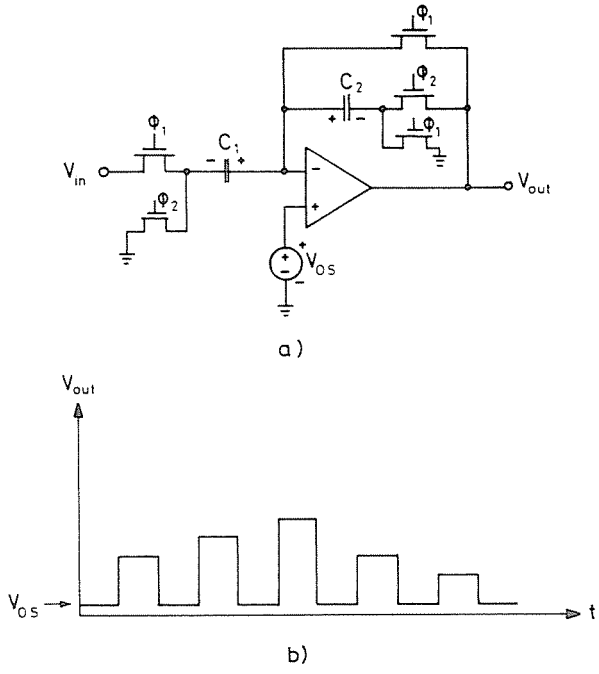

Fig. 3. Offset-compensated noninverting SC amplifier

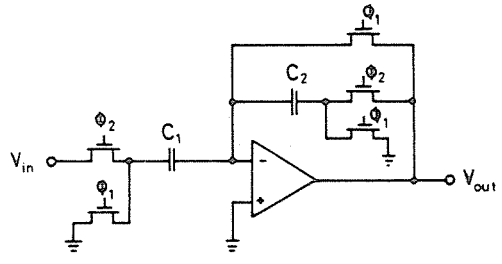

Fig. 4. Offset-compensated inverting SC amplifier

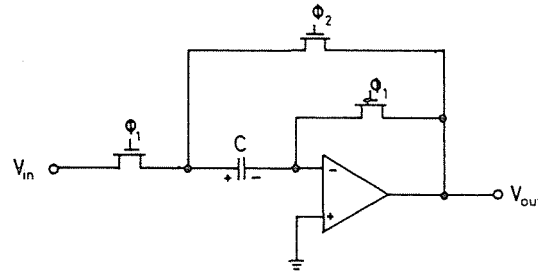

Fig. 5. Offset-compensated SC delay stage

the value of the signal and V_{os} (Fig. 3b). This is due to the feedback switch connected between the output and inverting input terminals. The switch performs two functions: it keeps the amplifier stable during the reset period, and it also allows C_1 to recharge without changing the charge in the integrating capacitor C_2. Thus, it makes possible the charging and discharging of C_1 without disconnecting it (or C_2) from the inverting input terminal. Thus, the source V_{os} is only capacitively connected to the rest of the circuit, and hence it has no effect on v_{out}. Fortunately, the above advantages can be retained, and also the slewing problem eliminated, if the feedback switch is replaced by a switched capacitor C_3 (Fig. 6). In this circuit [3], illustrated for an *inverting integrator* in Fig. 6, C_3 is charged to v_{out} during the integration phase when

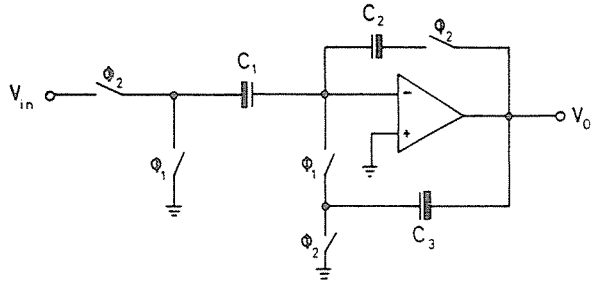

Fig. 6. Offset-compensated low-slew SC integrator

$\Phi_2 = 1$, and then recharged to $v_{out} + (C_1/C_3)v_{in}$ during the reset phase. Thus, the output voltage changes only by $V_{os} + (C_1/C_3)v_{in}$ between the two intervals. This change is typically less than 100 mV, and hence is much smaller than the maximum value of the change $v_{out} - V_{os}$ occurring when only a switch was used as the feedback branch. The offset compensation process functions otherwise exactly as before. By interchanging the phasing of the two input switches, the circuit can also be used as a *noninverting integrator*. The scheme can also be used in SC amplifiers (Fig. 7). Here, the output voltage changes by V_{os} for an

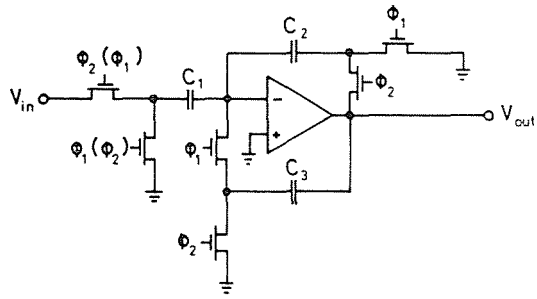

Fig. 7. Offset-compensated low-slew SC amplifier

inverting circuit, and by $V_{os}-(C_1/C_2)\Delta v_{in}$ for a noninverting one, where Δv_{in} is the change in v_{in} during the clock period. The method (as before) is directly applicable to D/A converters.

The change in v_{out} between the signal processing and resetting phases can be further reduced by a simple modification of the circuit of Fig. 6, as shown in Fig. 8. In this circuit [4], C_3 is precharged to $v_{out}-v_{in}$ during the $\Phi_1=1$ interval; hence, for $C_3=C_1$, the output voltage changes only by V_{os} between integration and reset periods. For *noninverting integration, two* extra capacitors are needed for the precharging (Fig. 9). For $C_1'=C_1$, the change in v_{out} is now $(1+$ $+C_1/C_3)V_{os}$.

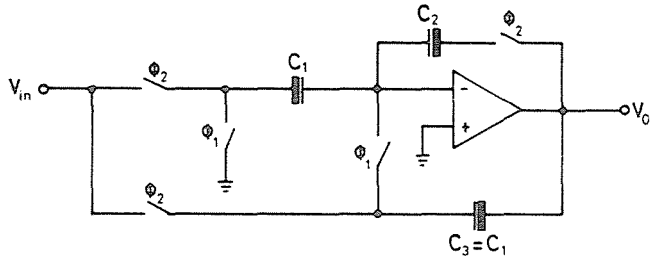

Fig. 8. Offset-compensated low-slew inverting SC integrator

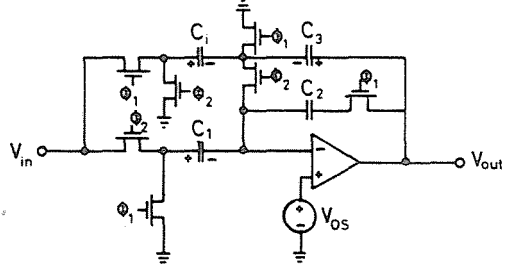

Fig. 9. Offset-compensated low-slew noninverting SC integrator

In an SC circuit containing n amplifiers, it may not be necessary to compensate all stages to obtain an offset-compensated output voltage for the overall circuit. If the network has (or can be transformed into) the structure shown in Fig. 10, then a single offset-free integrator OFI is sufficient to achieve

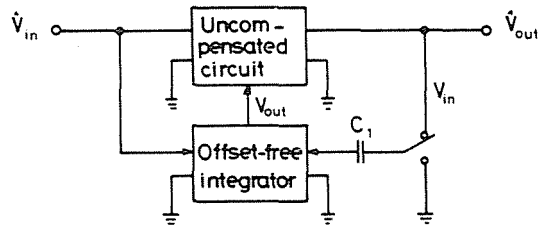

Fig. 10. Offset-compensation using a single offset-compensated SC integrator

an offset-compensated output voltage v_{out} for the complete network [4]. This can be seen by realizing that, for a stable circuit, in steady state the OFI output voltage v_{out} cannot change. This is only possible if $\hat{v}_{out}=0$ (for a bandpass or highpass circuit) or, for a lowpass circuit, if $\hat{v}_{out}/v_{in}$ has the ideal (nominal) value. Any clock feedthrough charge q_{cf} entering the feedback capacitor of the OFI will however change the value of v_{out} by an offset $-q_{cf}/C_1$. Hence, the OFI also may need some compensation for clock-feedthrough effects.

Fig. 11 shows how the principle of Fig. 10 can be applied to a bandpass *biquad stage*; Fig. 12 illustrates how a bandpass *ladder filter* can be transformed to the configuration of Fig. 10 [5]. In both of these circuits, only the single integrator OFI needs to have offset compensation.

The other imperfection discussed in this work is the finite dc gain of the amplifiers. Although unrelated to the offset effect in terms of its origin, its

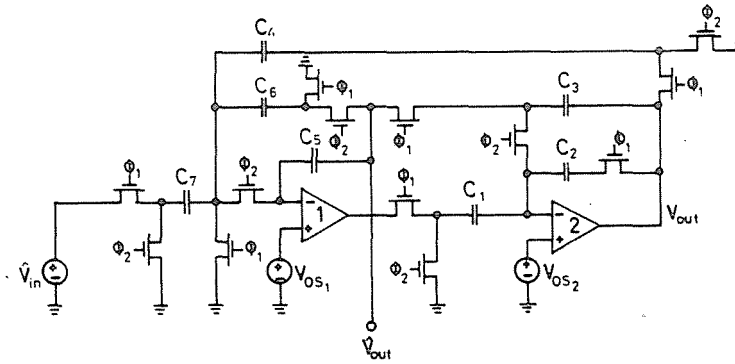

Fig. 11. Offset-compensated SC biquad

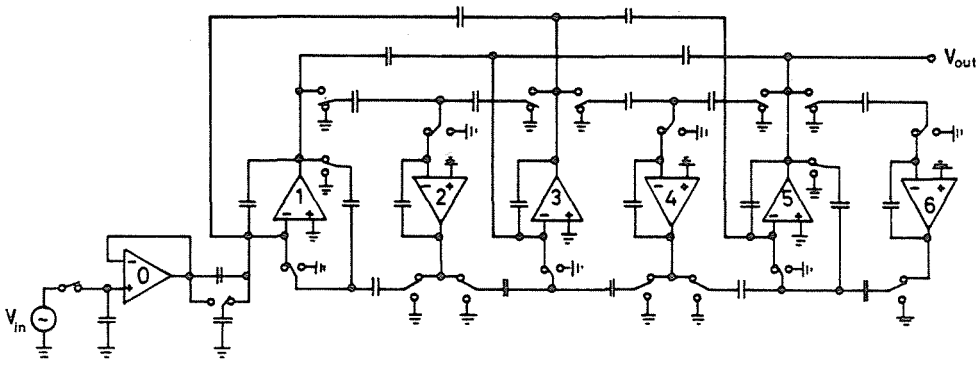

Fig. 12. Offset-compensated SC bandpass ladder filter

manifestation is somewhat similar. It gives rise to a spurious voltage μv_{out} ($\mu = 1/A$) between the input terminals of the amplifier, when the latter is operated in a negative feedback loop. This spurious voltage is in series with V_{os} as far as the inverting input terminal is concerned, and if v_{out} changes very little from one clock interval to the next (i.e., if $\omega T \ll 1$, where ω is the radian frequency of the signal, while $T = 1/f_c$ is the clock period) it can be regarded as a dc voltage. Hence one would expect that its effects will also be reduced by offset compensation. It was recently verified [6] that this is indeed the case. Figure 13

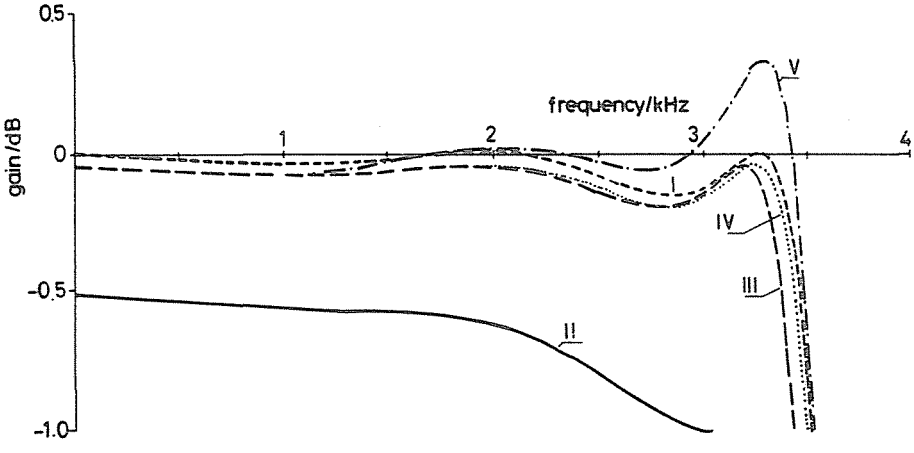

Fig. 13. Gain responses an SC ladder filter:

I. Ideal response ($A \to \infty$)
II. Uncompensated response, $A = 100$
III. Compensation using the circuits of Figs 6 & 8, $A = 100$
IV. As in III, with prewarping
V. Compensation using the circuit of Fig. 15, $A = 100$

shows how the sensitivity of a fifth-order SC filter to finite-gain effects is reduced by the application of the offset-compensated integrators shown in Figs. 6, 8, 9 and 15 (below). To explain this phenomenon [7], we recall that the finite dc amplifier gain in an integrator introduces both an amplitude and a phase error. Thus, the ideal integrator transfer function $H(\omega)$ becomes [8] for the finite-gain case

$$H_a(\omega) = H(\omega)\,[1 + m(\omega)]\,e^{j\Theta(\omega)} \tag{1}$$

where the real functions $m(\omega)$ & $\Theta(\omega)$ are the gain and phase errors, respectively. Writing the difference equation representing the charge conservation law at the inverting amplifier input node for both the integrating and reset periods, these error functions can be found. The results are given by the expressions [7] shown in Table 1. They were derived using the assumptions

Table 1

Error formulas for SC integrators with finite op-amp gain $A = 1/\mu$

Integrator	Gain error $m(\omega)$	Phase error $\Theta(\omega)$	Unity-gain phase error $\Theta(\omega_0)$
Uncompensated	$-\mu\left[1+\frac{C_1}{2C_2}+\frac{\mu}{2}\left(\frac{C_1/C_2}{\omega T}\right)^2\right]$	$\mu\frac{C_1/C_2}{\omega T}$	μ
Fig. 6	$-\mu(1+C_1/C_2+C_1/C_3)$	$\mu\frac{C_1}{C_2}\left(\frac{C_2}{C_3}\omega T+\frac{\mu}{\omega T}\right)$	$\mu\left(\frac{C_1^2}{C_2C_3}+\mu\right)$
Fig. 8	$-\mu(1+C_1/C_2)$	$\mu^2\frac{C_1/C_2}{\omega T}$	μ^2
Fig. 15 (for $C_3=C_4$)	$-\mu(C_1/C_2+\mu)$	$-\mu\left(\omega T-\mu\frac{C_1/C_2}{\omega T}\right)$	$-\mu\left(\frac{C_1}{C_2}-\mu\right)$

$\mu = 1/A \ll 1$ and $\omega T \ll 1$. The values of $m(\omega)$ and $\Theta(\omega)$ at $\omega_0 = 2f_c \sin^{-1}(C_1/2C_2)$ are also given in the Table. Here, ω_0 is the unit-gain frequency of the integrator; this is usually in the same range where the critical frequencies (cutoff, gain peak) of the overall circuit lie. Figure 14 [7] shows the frequency responses for the error functions in the case where $A = 1/\mu = 100$, $C_1/C_2 = 0.2$ and $f_c = 1/T = 100$ kHz. The integrators analyzed include the uncompensated circuit, the circuits of Figs 6 & 8 and a somewhat more involved offset-compensated integrator (Fig. 15) recommended by Nagaraj et al. [6] recently. All these compensated integrators have the important property, as explained above, that their output voltages v_{out} change only by a small amount during the transition between the reset and integration phases. By contrast, the output voltages of

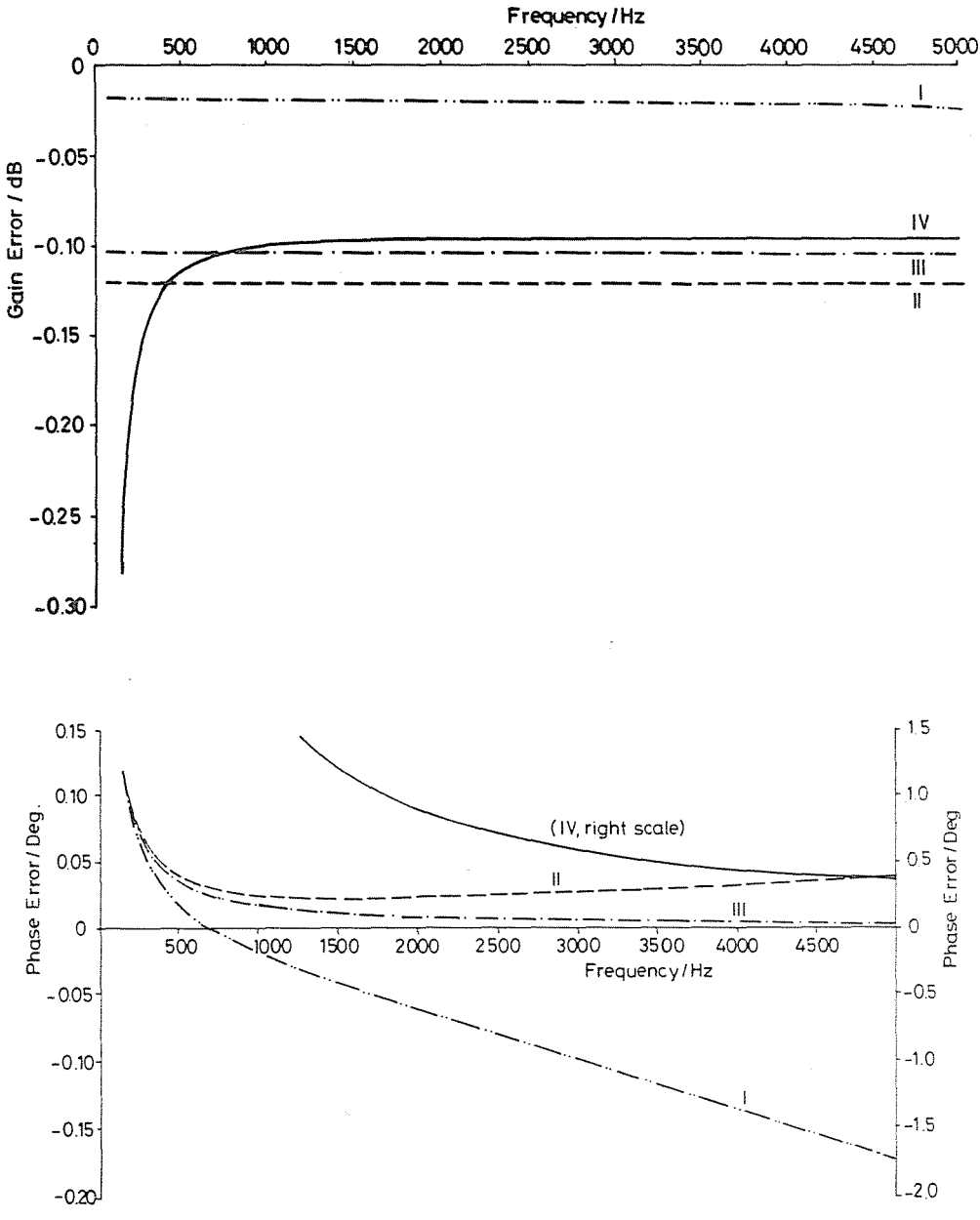

Fig. 14. Gain and phase error responses of SC integrators for $C_1/C_2 = 0.2$ and $f_c = 100$ kHz:
I. The circuit of Fig. 15 ($C_3 = C_4$)
II. The circuit of Fig. 6 ($C_3 = C_2$)
III. The circuit of Fig. 8 ($C_3 = C_1$)
IV. The uncompensated integrator

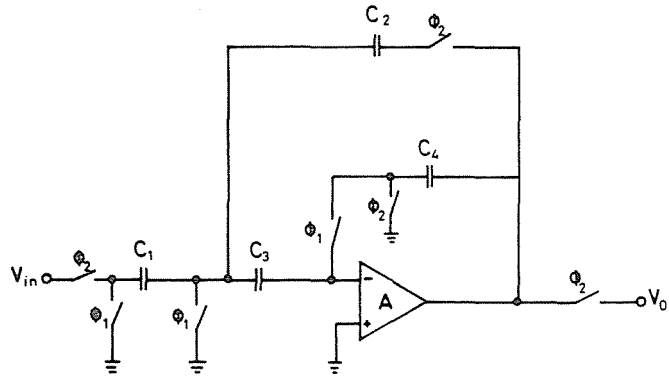

Fig. 15. Offset-compensated low-slew SC integrator

the compensated integrators based on the schemes of Figs 3–5 change back and forth between the signal value and V_{os}. As a result, there is no coherence between the values of v_{out} during the reset and integration periods, and hence the error functions are simply those of the uncompensated integrator.

A comparison of the error functions of Table I and Fig. 14 reveals that the gain error $m(\omega)$ is the smallest ($m \approx -\mu C_1/C_2$) for the integrator of Fig. 15 [6]. On the other hand, the phase error is the least ($\Theta \approx \mu^2 C_1/(C_2 \omega T)$) for the inverting integrator of Fig. 8. (Note that the noninverting integrator of Fig. 9 has the same gain error, but twice the phase error, as the circuit of Fig. 8). It is interesting to note that $\Theta(\omega_0)$, which equals $\mu = 1/A$ for uncompensated integrator, becomes μ^2 for the compensated circuit of Fig. 8. Thus, the compensated integrator using an amplifier with a dc gain of 40 dB gives a phase response performance comparable to that of an uncompensated integrator with an 80 dB amplifier. The performance of the circuit of Fig. 6 is slightly inferior to that of Fig. 8; however, used as a noninverting integrator, this circuit has an advantage in terms of simplicity over the integrator of Fig. 9.

It is well known [8] that the gain error of an integrator is equivalent to an element-value change, while a phase error results in a finite-Q effect. Hence, using the integrators of Figs 8 & 9 (or Figs 8 & 6), the finite amplifier gain results essentially in a small frequency shift of the overall response, while using the integrator of Fig. 15 (which has a negative phase error $\Theta \sim -\omega\mu T$) the finite-gain effect gives a somewhat peaked passband behavior. These conclusions are confirmed by the curves of Fig. 13. If the value of μ is fairly well controlled, then for the circuit using the integrators of Fig. 6, 8 & 9 it is also possible to "prewarp" the element values, i.e., to replace C_2 by $C_2(1-m)$ in each integrator. This reduces the gain error to a negligible value, and hence eliminates the frequency shift of the overall response.

It is important to note that the sensitivity of the response of SC filters to finite-gain effect is also influenced by its scaling. Both theory [9] and experience

suggest that nearly minimum sensitivity is obtained for that scaling which also optimizes the dynamic range of the filter. The improvement between scaled and unscaled responses is especially large for narrowband filters.

It is hoped that using the circuits and observations contained in this paper selective SC circuits can be designed using only simple and hence fast amplifiers. This may allow an extension of the present frequency range of these devices.

Acknowledgement

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