TESTING ELECTRONIC COMPONENTS BY HOLOGRAPHY

A. AMBRÓZY

Department of Electronics Technology,
Technical University, H-1521 Budapest

R. FEIERTAG

Department of Electromechanical Constructions
University of Wuppertal*

D-5600 Wuppertal 1, Fuhlrottstrasse 10.

Received September 22, 1984

Summary

A five-year cooperation is described in which the German partner provided the test method with real time holography and the Hungarian partner—using its technological experience—designed and made the printed circuit and hybrid microelectronic samples to be investigated. The results give better insight to the reliability of the above mentioned structures since the deformations caused mainly by thermal stresses are readily observable.

Introduction

The revolutionary changes occurring in the electronic industries were connected with the printed circuit. With the introduction of the transistor, the number of components and interconnections in circuits rose considerably. Printed circuits, where electrical and mechanical connections are identical, have proved to be ideal for mass production. Moreover, they are excellent supports for integrated components with high packing densities.

Table 1 shows the increase in the number of elements beginning with early radios in 1930. Up to 1000 components could be connected by soldering of wires at resonable prices and with only a small number of faults. This is impossible in the case of modern electronic equipment such as a microcomputer or a fiber-optical communications system. Here the printed circuit in connection with integrated circuits is the basic technology for production at reasonable costs.

* Formerly Universität Karlsruhe.

Table 1

Increase of component number in electronic equipment

Instrument	Year	number of elements	Technology of connections
Radio	1930	100	wire
Television	1950	1000	wire
Color Television	1970	10^4	printed circuit
Computer	1970	10^5	printed circuit + IC
Microcomputer	1980	10^6	printed circuit + IC
Fiber optical communications system	1982	10^7	printed circuit + IC

Printed circuits are typical multi-function elements, as they are at the same time:

a) conductors of electric current

b) supports for electrical and electromechanical components and, consequently,

c) themselves components of the superstructure and

d) part of the electrical components, because resistors can also be printed.

Moreover, circuit plates serve as

e) loose or fixed contacts,

f) screenings,

and, finally,

g) descriptions of wiring diagrams

h) gauging and measuring standards and

i) type and name

can be printed upon them.

For faultless operation of electronic equipment, printed circuits have to be highly reliable since ruptures in the circuit lines will in most cases result in a break-down of the entire system. Such ruptures of circuits printed on plates are brought about by a number of different causes:

Mechanical loads result in damage to the supporting material and to the conductors. Chemical damage is due to faulty etching. Thermal overloads during soldering damage the layer of glue between conductors and board and, as a result, circuit lines around soldering joints will peel off and break, especially under dynamic loads. Excessive electric loads deform circuits and plates [1, 2].

Beginning with the mid-seventies the fine-pattern double- and multilayer boards became dominating. Characteristic is the linewidth and space of 0.35 mm and the width of an eyelet ring is about 0.2...0.3 mm.

Recently, the superfine pattern printed circuit boards begin to appear. Usually two conductor lines are squeezed between two IC pins and the line and space is around 0.2 mm.

According to forecasts at the turnover of eighties and nineties the line and space will decrease to 0.08. . .0.15 mm, the hole diameter to 0.5 mm.

Presently the thickness of the copper cladding is generally 35 μm. Now one can observe the spreading of the use of 17.5 μm copper foils. Presumably the smaller features—line and space of 0.1 mm—will need thinner foils, say 5. . . 10 μm. Also the galvanoplated layers become thinner. So the total structure turns into more and more vulnerable.

In general, the producing technology develops more quickly than the active control between manufacturing steps or the final qualification. Frequent weakness of fine-pattern boards is the narrowing of conductors, or more seriously, their cracking and breaking. Another characteristic fault is the breaking of copper deposited into the holes. The reason of the above mentioned faults is partly the imperfect technology, partly the mechanical stress caused by thermal load. The linear thermal expansion coefficient of the glass-epoxy substrate material is anisotropic: in the direction perpendicular to the plane it is about ten times as of in the plane or as of the copper. Printed circuit boards are damaged mostly by soldering but the electrical load of conductors may also cause problems.

The refinements and failure modes described above are demanding for advanced testing methods. Non-destructive testing of printed circuits and components are in most cases too complicated for application in the production line. Testing by ultrasonics, X-rays or infrared, as well as most electric methods, are restricted to the laboratory.

In the following, an optical testing method will be described which is more suitable for industrial production, as it is easy to apply and because its results are open for direct observation.

Such a method is necessary, as it is impossible to determine temperature increases and deformations of printed circuits by calculation. Calculation of the temperature of one single circuit line under load, alone, yields a wide range of results [3]. Similarly, there is no way of predicting by calculation any damages from the soldering process nor areas of vibration at special frequencies.

Nondestructive testing method

With the invention of the laser, a tool for nondestructive testing was created. The coherent radiation of laser made possible the generation of certain phenomena by means of light, which had been known for a long time in other fields of electromagnetic waves.

Reflection of laser light is used for the localization of vibrations and superposition of laser light is the basis for the wide range of holographic techniques for structural testing.

The laser speckle phenomena

For structural testing lasers are used which emit light of a single wave length. Helium-Neon-Laser with the wavelength of $\lambda = 0.6328$ μm and Argon-laser with $\lambda = 0.5145$ μm are preferred for these purposes. Dye-lasers and tunable lasers are the sources for a number of other wavelengths, between ultraviolet and infrared [4, 5].

An object illuminated by laser light, has a grainy or speckled appearance. These laser speckle phenomena are caused by random interference of coherent laser light, scattered from a diffuse surface. Actually, these speckle spots do not occur on the surface of an object, they are created by interference on the retina of the observer's eye, or on the photographic plate of the camera. The size of the speckles is determined by the aperture of the lens; the smaller the lens aperture, the larger the speckles [6].

These laser speckles can be observed on stationary objects illuminated by laser light. As soon as the object starts moving, the speckles disappear on those parts of the object which are in motion or vibrating, while they remain visible on the stationary parts of the object. Therefore, the laser speckles are very useful for direct observation of vibrating objects. The speckle spots remain to be seen in all stationary areas and node lines, while they are blurred where the object is in motion [7].

Holographic testing methods

Holography [8] is the first non-contact measuring method for making accurately visible the exact size of deformations. As shown in Fig. 1, a hologram is obtained by lensless photography: The image is not recorded directly on the photographic plate, only the wave fronts of a coherent beam of light scattered from the object are recorded and caused to interfere with a reference beam [9—11].

When the hologram is illuminated by a coherent beam of laser light, incident from the same angle, we get a three-dimensional image of the object, which can be observed and photographed from different angles (Fig. 2).

If two holograms of the same object, which has meanwhile slightly changed its shape, are superimposed, the image reveals interference fringes, which serve as a criterion for the displacement of the object. Thus, deformations of three-dimensional objects can be investigated with accuracies hitherto unknown. Deformations in the range of 10^{-3} mm become directly visible, in certain circumstances methods of interpolation result in accuracies up to 10^{-6} mm.

Figure 3 shows such a double exposure holograms, as an example for the deformation of a circuit plate, due to heating up of the conductors. The visible interference fringes may be regarded as topographical contour lines of equal

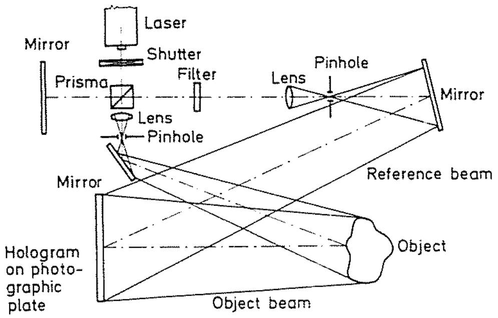

Fig. 1. Arrangement for forming a hologram

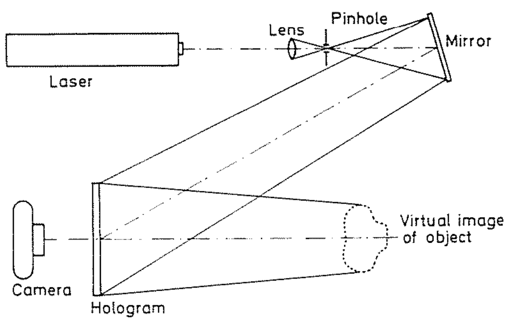

Fig. 2. Reconstruction of a hologram

displacement. The fringe spacing is one-half the wavelength of the laser light used for illumination. Here a red He-Ne-gas-laser with $\lambda = 632.8$ nm was used, one half the wavelength is 0.316 μm.

A conductor crossing the entire plate of 109 × 106 mm was heated up for two minutes with 2A and 0.43 V. The plate is screwed to supports in its four corners. In the centre we have a displacement of the surface by 16 fringes away from the observer. In addition, the hologram reveals the path of the heated circuit. It forms a shallow trough, indicated by sharp bending of the interference fringes, showing clearly the path of the circuit line across the surface of the plate.

Deformation holograms of that kind permit conclusions as to the operation of conductors and components [12]. They are particularly useful for locating overheated or insufficiently heated areas, caused by defective circuits, e.g. where circuit lines are too narrow or have hairline cracks.

In testing laboratories holograms are usually recorded on large-size photographic plates of 13×18 cm. These plates have high resolutions of

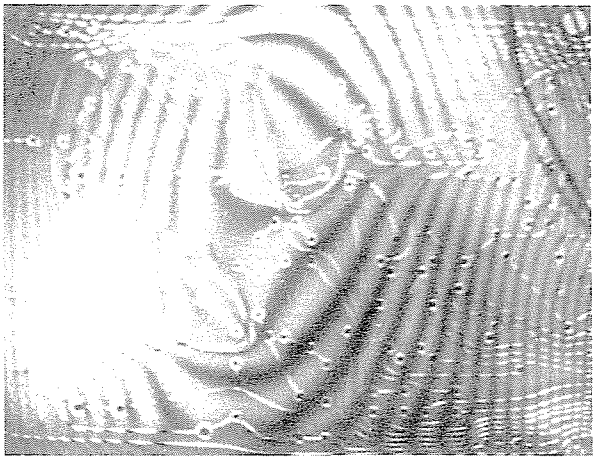

Fig. 3. Double exposure hologram of a printed circuit board

approx. 3000 to 5000 lines/mm, so that the entire image information can be stored in each individual area of the hologram. When reconstructed, the object, appearing as a virtual three-dimensional image, can be observed by looking at it through the large plate, just as if looking through a window.

After exposure, the hologram plates have to be developed, fixed and dried, according to the normal procedure for photographs. In order to simplify the process and to obtain real time holograms, automatic development systems were designed, with the liquids being pumped against the plates. But this process is also difficult to accelerate and, therefore, not very suitable for production testing.

Real-time holography

Compared with other non-destructive testing methods for electronic components, real-time holography has the advantage of revealing hidden defects.

For the reproduction of holograms a high resolution photomaterial is used. This is a photothermoplastic holographic film, produced by Kalle-Hoechst AG. The film is developed in situ. It is equally well suited for the visible laser spectrum from 441.6 nm to 632.8 nm and has a high resolution of up to 2000 lines/mm. It is sensitized by electrostatical charging. Because of the photoconductive properties of the film these charges are discharged where the film is exposed, forming thus a charge image. To develop the film, heat of up to glass temperature is applied to the thermoplastic layer. The result is a ghost image, the phase hologram.

Rapid cooling fixes the image, which can be erased by applying heat of higher than glass temperature [13] (Fig. 4).

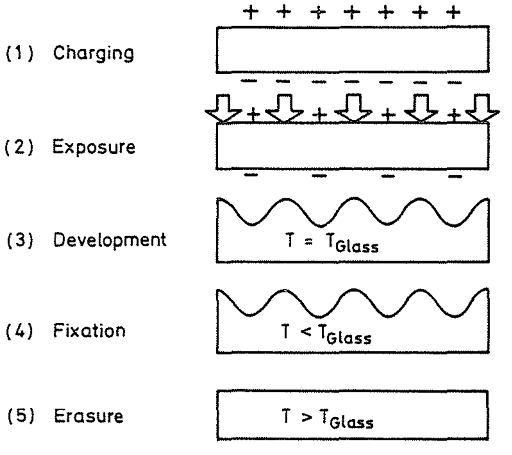

Fig. 4. Recording-erasure cycle of a hologram on photo-thermoplastic film

Four steps are required to produce a hologram:

1. The film is sensitized by applying an electrostatic charge to the film.

2. On exposure the static charge gathers at the exposed points, due to photo-conductivity.

3. The film is developed by warming it for a short period. The relief picture is identical to the load distribution picture.

4. The film is cooled to fix the relief picture.

The PT Holographic Instant Picture Unit (Fig. 5) performs these steps automatically. Transportation of the film and sensitization take 4 seconds. The exposure value of 5 J/cm^2 is comparable to that of a silver-coated film. For development a warm burst of approx. 50 joules is applied to the film for 0.15 seconds immediately after exposure. Then, the heat is absorbed by air blown in through jets pointing at the film carrier. The entire process takes 40 seconds. The hologram can be observed while the film is being fixed [14, 15].

The reconstructed hologram is superimposed with the object. As the position of the object has remained unchanged since the hologram has been taken, any subsequent deformation is revealed by interference fringes, which are contour lines in a distance of $\lambda/2$.

A video camera together with a monitor and a video casette recorder are very useful for observing and recording the image.

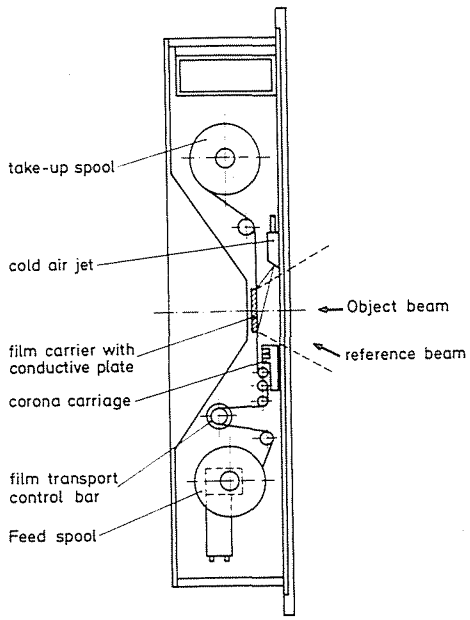

Fig. 5. Holographic instant-picture unit for photo-thermoplastic film

Testing of printed circuit boards and other structures [16–37]

The real-time holographic equipment was given at the Karlsruhe University. (Later on it was transferred to Bergische Universität-Gesamthochschule Wuppertal.) At the same time a strong technology center of printed circuit boards and hybrid microcircuits has evolved at the Technical University, Budapest. It was obvious to combine the efforts of both parties to gather informations about the deformations of several different structures.

The Department of Electronics Technology, Technical University Budapest developed the real circuit boards or special models which imitated one or more characteristical properties of such structures. Combined efforts of both parties were necessary to develop proper fixtures for holographic measurements: rigid clampings are necessary at corners or edges but the deformation of central parts should be permitted.

In the followings, typical experiments will be described.

Broken-line wiring

The design practice of printed wiring considers the change in direction of 90° and the through-plated hole as weakest points with regards to reliability. Our investigations verified them only partially.

Experimental patterns were made of 1–3 conductor paths with 90° change in direction and with different shapes of the corner: angled, arched and diagonal with 45° (Fig. 6). The conductors were loaded by current. The center

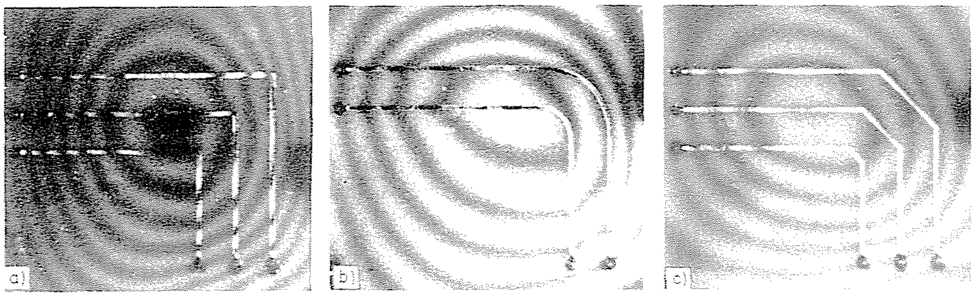

Fig. 6. Lines with 90° change in direction a) angled, b) arched, c) diagonal

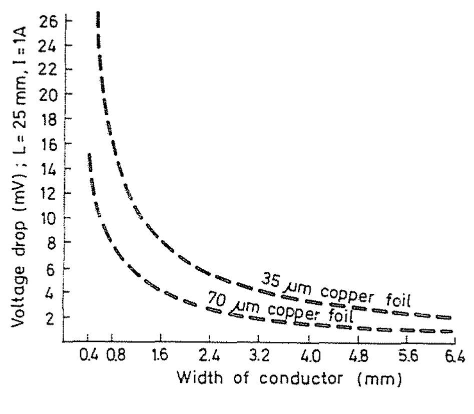

Fig. 7. Voltage drop along a conductor

of the deformations were always at around the midpoint of the conductors. The temperature at the midpoint was higher by 5...6 °C than at the ends.

The situation becomes worse with the fine and very fine patterns. The resistance of the conductor increases with the decrease of width and thickness (Fig. 7). At the same time, the heat conduction and radiation also diminishes. It follows from the above reasoning that the breakpoints and holes should keep away the midpoint of lines with heavy current load and the particular shape of the break is almost irrelevant.

Through plated hole

Typical failure of through plated hole—especially with long, slim holes—the rupture in the neck (Fig. 8). It is caused mostly by mismatch in the temperature coefficients of the linear expansion of copper and of the epoxy-glass substrate in the z-direction.

The tensile stress in the copper and the compression stress in the epoxy glass should be equal. The ratio of the linear thermal expansion coefficient is

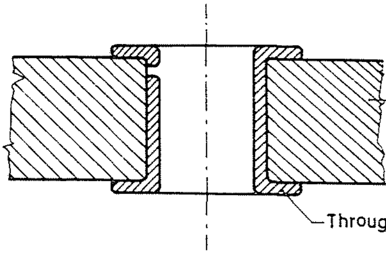

Fig. 8. Break in the neck of the hole

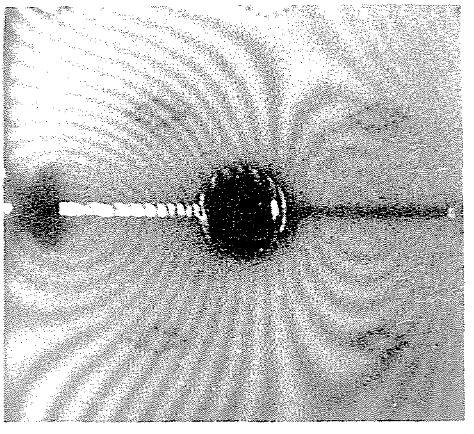

Fig. 9. Enlarged through-plated hole

between 4. . .30. That of the copper $\alpha_{C_1} = 17.10^{-6}$ K^{-1} (between -65 °C and $+260$ °C); that of the epoxy $\alpha_e = 75.10^{-6}$ K^{-1} below a temperature depending on the composition, and above it suddenly changes to approx $400 \cdot 10^{-6}$ K^{-1}. This is dangerous to the copper plating in the hole.

According to our observations the most highly stressed area of a hole is where the line is connected. The real size of a hole is too small for observation in an interference picture. Therefore an artificial "big hole" was developed with the diameter of 10 mm (Fig. 9). From the pattern of interference lines one can observe that the mechanical stress is highly uneven which can cause partial rupture in the neck (as it is drawn in Fig. 8). Of course, by the magnification of the diameter the inhomogeneity of the stress is exaggerated. The current flowing through the mantle of the hole was 10A.

In the next series of experiments the mantle of the hole was outspread: the linear hole is shown in Fig. 10. The conducting copper sheet was divided into 5

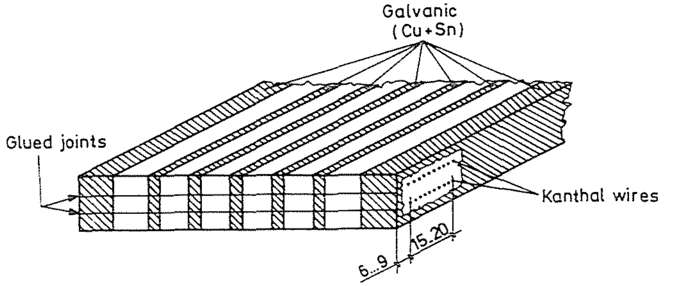

Fig. 10. The "linear hole"

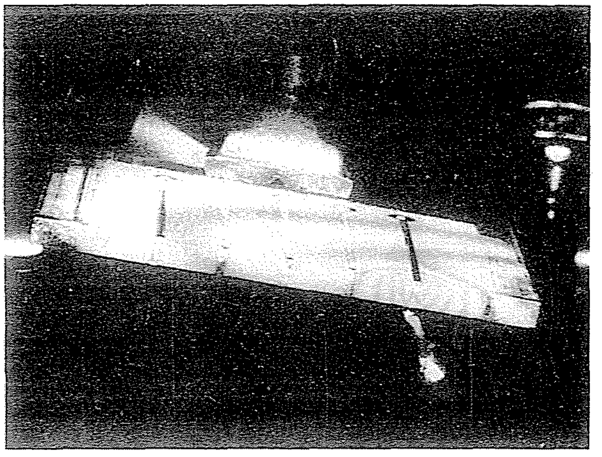

Fig. 11. Heating by soldering iron, $T = 130$ °C

lines. The thermal stress was applied by three different ways: by current flowing through the copper lines, by heating with soldering iron, and by heating with additional kanthal wires built in one or two layers. The total thickness of the board was about 7.5 mm to emphasize the dimension in the z-axis.

Fig. 11 shows the deformation during heating by a soldering iron of 130 °C and Fig. 12 the same, during cooling down, at about 50 °C.

The next three Figures (13—15) show the effect of current flowing through the copper conductor. The nonlinearity of thermal expansion

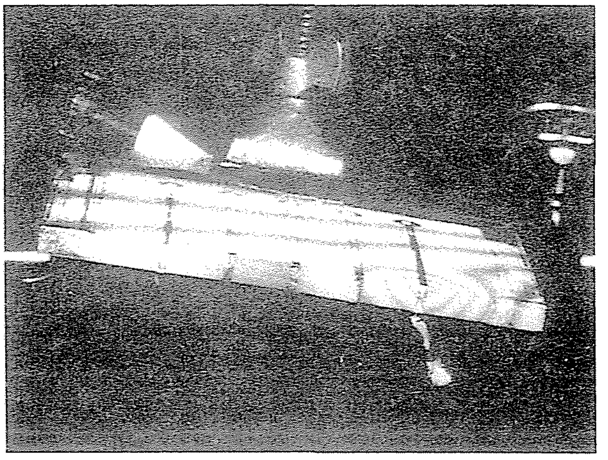

Fig. 12. As Fig. 11, cooled to $T=50\,^{\circ}C$

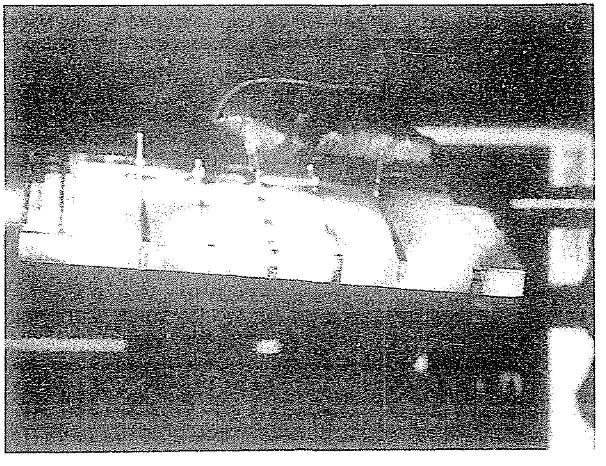

Fig. 13. Current of 2,5A in one conductor

coefficient of epoxy-glass mentioned above is clearly seen comparing Fig. 13 and Fig. 14: while in the first case the current is 2.5 A, in the second it is only by 20% higher, i.e. 3 A. If all the conductors are in series then the deformation is more homogeneous (Fig. 15).

Unfortunately, we got no useful photographs with the built-in heating elements.

No rupture was found during the experiments, probably the structure was very robust.

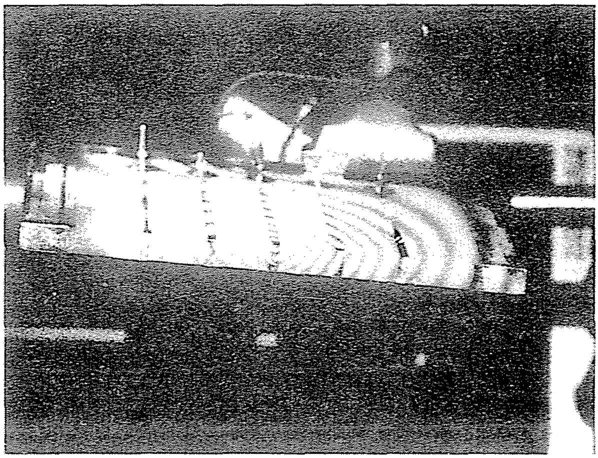

Fig. 14. Current of 3A in one conductor

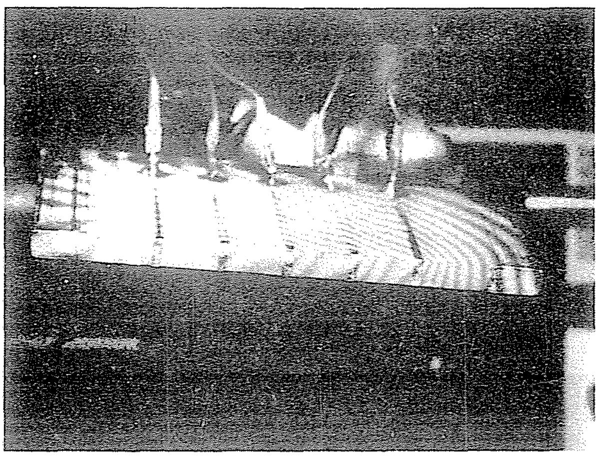

Fig. 15. All conductors in series, $I = 3A$

Multilayer boards

In the course of the investigation of multilayer boards the following questions arise:

— how large are the deformations caused by the dissipation of heat of the inner conductors

— what are the effects of large-size inner conductors (supply-planes)

— whether the gluing failures can be detected.

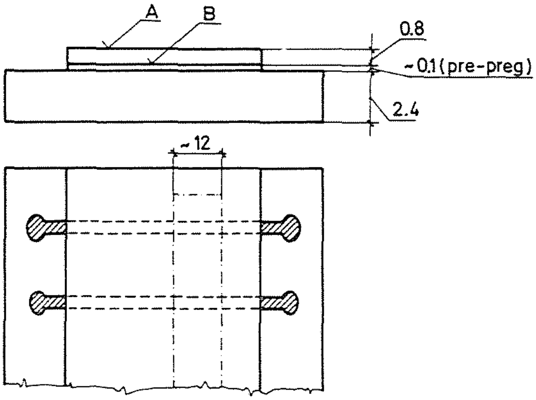

Fig. 16. Structure of the multilayer specimen. Planes *A* and *B* may or may not be copper cladded

The structure to be investigated is shown in Fig. 16. To obtain the proper rigidity the base plane was much thicker (2.4 mm) than usually. Some samples contained an artificially damaged area (the adhesive layer, i.e. the so-called pre-preg was removed in a stripe).

In stationary state (I = 4 A) the deformation pattern of Fig. 17 comes into being. If the adherence is asymmetrically damaged, the deformation pattern is also asymmetrical (Fig. 18).

If there is a supply plane the articulation of the pattern disappears (Fig. 19); however, the changing deformation along the length axis can be easily

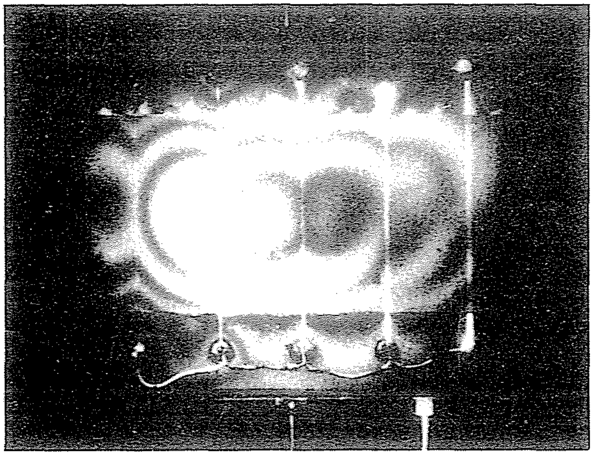

Fig. 17. Multilayer specimen heated by currents flowing through the five lines of different widths

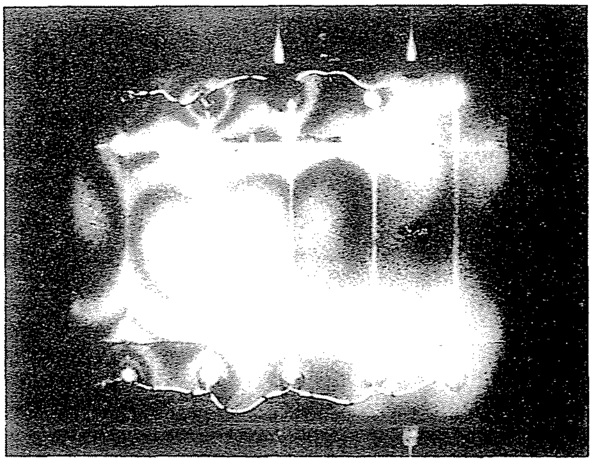

Fig. 18. As Fig. 17, with damaged adherence. Interference pattern shifted upwards

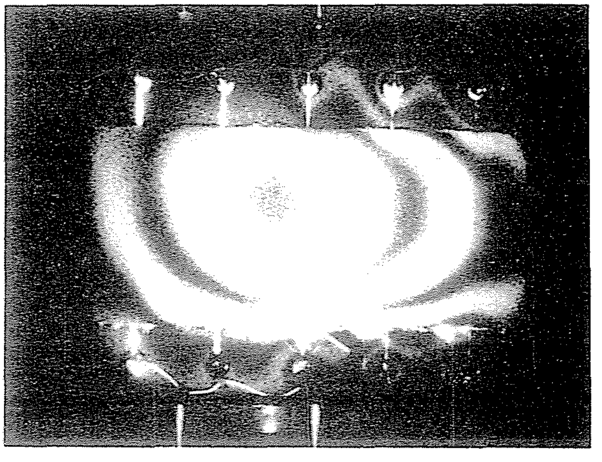

Fig. 19. As Fig. 18, the B plane of Fig. 16 is now of copper

observed. It is caused by the varying dissipation which depends on the widths of conductors. This sample also contains a damaged area: this is the reason of the asymmetry observable along the perpendicular direction.

Surface mounting

A new mounting style begins to spread in the last few years: the surface mounting. Components, such as resistors, capacitors, integrated circuits are manufactured in chip form, without leads. This influences the thermal conditions of their carrying plate, the printed circuit board since the components are in close proximity to it.

Figure 20a shows our experimental model. Two pairs of resistors were formed on glass substrates by evaporating nickel-chromium. One resistor pair has a square form ("point thermal source"), the other ones are elongated ("line thermal source"). In the first experiment one point source dissipated 100 mW and the neighbouring line source 200 mW (Fig. 20b); in the second experiment the powers were doubled (Fig. 20c). The other resistors were idle. Studying the interference curves a dome at about the mid, and a bending of one edge can be discovered as expected.

In our experiments the specific power stress was not especially high—about 5 mW/mm^2. To model the real conditions smaller dimension heat sources and higher powers will be necessary.

Fig. 20. a) Surface mounted panel, b) interference lines with 100 + 200 mW, c) interference lines with 200 + 400 mW

Thin film microcircuit

The substrate of a microcircuit is either glass (for thin films) or ceramic (for thick films). Today the most widespread size is 50×50 mm^2 but the expansion of dimensions is foreseen. During manufacturing and normal use these substrates are exposed to mechanical and thermal stresses; the larger the dimensions are the higher the danger of crack since both materials are brittle.

Until now this is the one structure which can be handled theoretically [21, 22]. Let us assume that we have a thin glass plate with thickness d and the two other dimensions are infinite. If one side is kept at ambient temperature T_1 and a higher temperature T_2 is applied suddenly to the other side the partial differential equation

$$\frac{1}{a}\frac{\partial T}{\partial t}=\Delta T=\frac{\partial^2 T}{\partial z^2}$$

is valid, since $\partial^2 T/\partial x^2=\partial^2 T/\partial y^2=0$. From the solution it follows that the deformed shape of the plate is a spherical calotte with a radius of

$$R=\frac{\text{const}}{T_2-T_1}$$

The constant depends on the thickness of the plate, and other factors. Fig. 21 shows $1/R$ in function of temperature and Fig. 22 demonstrates the transient behaviour of R.

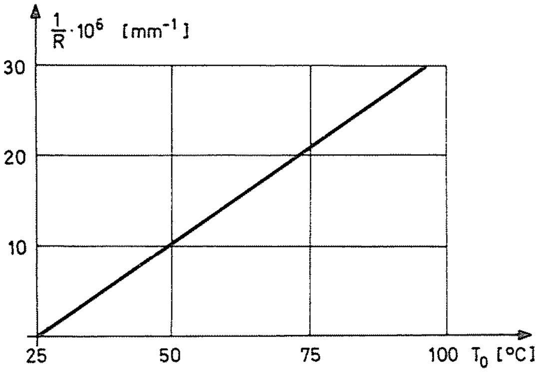

Fig. 21. Reciprocal of curvature radius *vs* temperature

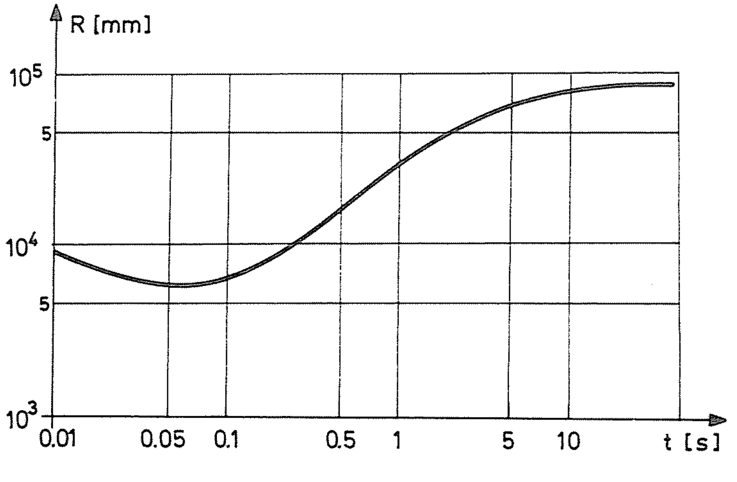

Fig. 22. Transient behaviour of curvature radius

The above partial differential equation is valid also for the case when the heat is applied on one side by a stripe-like heat source. Of course, the boundary conditions change. Fig. 23 shows the interference lines corresponding approximately to a spherical calotte. Investigations of the transient solution demonstrated that a peak in tensile state develops if the heat source is placed to the edge of the substrate. The edges are more vulnerable than the centre since at cutting microcracks come into being and therefore it is advisable to place the high-power resistors as centrally as possible.

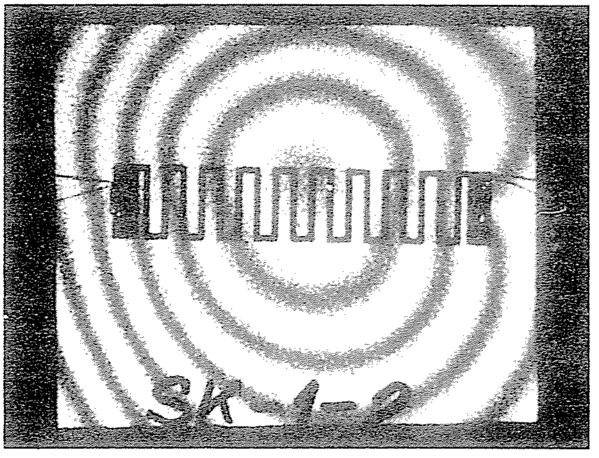

Fig. 23. Interference lines of a stripe-heated glass substrate

Encapsulated integrated circuit

In the course of the encapsulation—whether it is done by low pressure molding or resin pouring—the encapsulated circuit becomes deformed. In an experiment [38] a silicon chip, provided with strain gauges, was encapsulated and the resistances of the strain gauges were monitored. The deformation caused by the tensions in the encapsulating material modified the resistances (Fig. 24).

In the resistors of a hybrid integrated circuit considerable power may dissipate. It results in a mechanical stress in the case-substrate-pins-hybrid component parts system. A lot of consequences may occur:

— changes in resistance values

— damages in adherence between the substrate and encapsulation

— in a more serious situation, the hybrid component parts or the leads may break off.

Figure 25 shows an audio power amplifier encapsulated into an aluminium case with pouring of resin. The amplifier was loaded to the normal

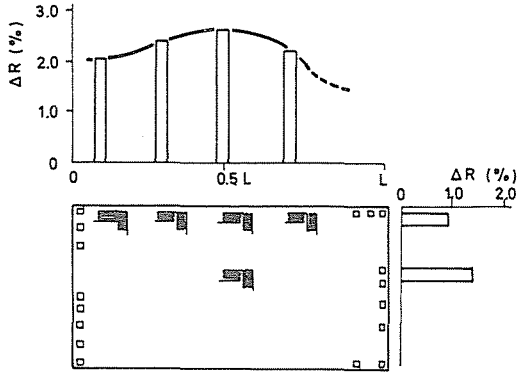

Fig. 24. Resistance changes of strain gauges caused by mechanical tensions in encapsulation

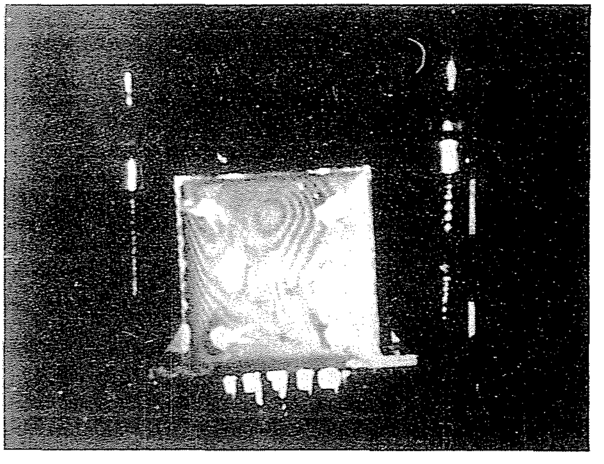

Fig. 25. Mechanical stresses in encapsulated power amplifier

working conditions. One can see from the interference-picture that the topology of the hybrid circuit is far from ideal. The two hottest elements (one power transistor and one resistor) should have been placed to the center of the substrate.

Mounted circuit

Figure 26 shows a rectifier under operating conditions in a stable state. The plate is fastened on its longitudinal sides near the corners. Under load it buckles in the centre, forming a dome (Fig. 27). Maximum deformation is 41 lines $\times$ 0,257 μm, a little below the centre of the plate. At the back of the lower

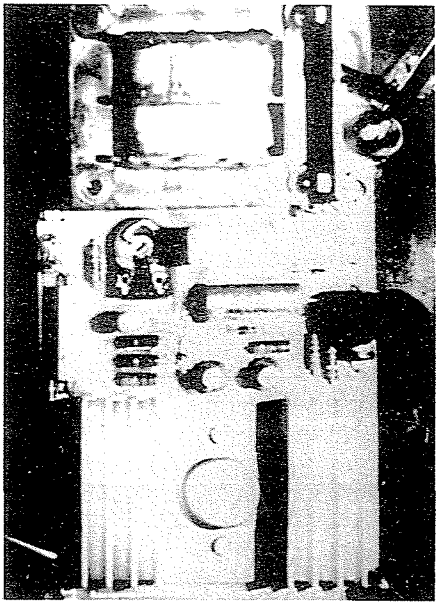

Fig. 26. Rectifier mounted to a printed circuit board

Fig. 27. Interference lines of circuit in Fig. 26

third of the plate there is a cooling unit for a power transistor. The pattern of deformations provides indications as to the most durable type of fastening, i.e. by riveting, soldering or gluing and for the positioning of the fixing points. Depending on the directions of the electric current in the circuits, maximum deformation occurs in a kind of centre of the load. Individual circuits under particularly high loads appear as ridges, with the interference fringes bending abruptly.

Conclusion

The fundamentals of the cooperation were given at both parties: Karlsruhe (later Wuppertal) University is provided with the real time holographic equipment and the Technical University, Budapest has the necessary technological background for electronic components and subassemblies. A broad spectrum of printed circuit and hybrid microelectronic was investigated.

With the development of the electronics more and more fine patterns come into prominence. Their reliability can be assured only if the nondestructive testing methods keep pace with the development. The continuation of the work reported here is highly recommendable.

Acknowledgements

The authors are indebted to the Deutsche Forschungsgemeinschaft, as well as to the Hungarian Ministry of Education who gave the financial aid for the research work. Many coworkers of both sides contributed to this final report, their names are collected in the reference list.

References

1. FAULSTICH, K.: Zerstörungsfreie Prüfung von Lötstellen, Feingerätetechnik *22*, 13–14 (1973)
2. HELM, H.: Zerstörungsfreie Prüfung von Mehrebenen-Leiterplatten, Feingerätetechnik *22*, 10–12 (1973)
3. FEIERTAG, R.: Die Temperaturen belasteter Leiterzüge und des Trägermaterials von gedruckten Leiterplatten, Feinwerktechnik + Meßtechnik *82*, 316–320 (1974)
4. KUHL, J.–SCHMIDT, W.: Tunable Coherent Light Sources. Appl. Phys. *3*, 251–270 (1974)
5. New Infrared CW Dye Laser, Spectra Physics Laser Review *4*, 1 (1977)
6. ADAMS, F. D.: Speckles are Needed, LASER + Electro-Optik *9*, 20 (1977)
7. ELIASSON, B.–MOTTLER, F. M.: Determination of the Granular Radiance Distribution of a Diffuser and its Use for Vibration Analysis, J. Opt. Soc. America *61*, 559–561 (1971)
8. GABOR, D.: A new Microscopic Principle. Nature *61*, 777–78 (1948)
9. COLLIER, R. I.–BURCKHARDT, C. B.–LIN, L. H.: Optical Holography, Academic Press, New York and London 1971

10. FRANCON, M.: Holographie, Springer-Verlag, Berlin, Heidelberg, New York 1972
11. KIEMLE, H.–RÖSS, D.: Einführung in die Technik der Holographie, Akademische Verlagsgesellschaft, Frankfurt/M, 1969
12. FEIERTAG, R.: Verformungsbewegungen von gedruckten Leiterplatten bei elektrischer Belastung. Feinwerktechnik + Meßtechnik *84*, 59–64 (1976)
13. MORAW, R.: Photothermoplastische Aufzeichnungsmaterialien für die Holographie. Kongreßband Fachreferate 4. Internat. Kongreß für Reprographie und Information 1975, 13–17. *4*, 1975, Hannover.
14. FEIERTAG, R.: Echtzeit-Hologrammbeobachtung bei Verformungsmessungen mit fotothermoplastischem Film, Feinwerktechnik + Messtechnik *85*, 150–154 (1977)
15. CRAWFORD, J. R.–BENSON, R.: Holographic Interferometry: Identification of Circuit Board Component Failure. Applied Optics *15*, 24–25 (1976)
16. FEIERTAG, R. M.: Echtzeitholographie bei der Auslegung elektrisch leitender Bauelemente, Constronic '80, 3rd Conference on Mechanical Aspects of Electronic Design, OMKDK-Technoinform Budapest 1980, 187–195
17. HAJDÚ, I.–PINKOLA, J.–TÓTH, E.: Holographic and thermographic tests of printed circuit boards, Constronic '80, 3rd Conference on Mechanical Aspects of Electronic Design, OMKDK-Technoinform Budapest 1980, 205–211
18. FATH, W.: Verformungsmessungen an hoch belasteten Leiterplatten mit Hilfe der Holographie In: Feinwerktechnik bei elektronischen System S. 180–189 (NTG-Fachberichte Bd. 69) Berlin 1979
19. HAJDÚ, I.: Examination of printed circuit boards In: Test Methods in Electronics Technology Balatonfüred 15.–18. 5. 1979 p. 138–144.
20. TÓTH, E.: Technological Aspects of multilayer board design, In: Vorträge zum 4. Int. Frühjahrs-Seminar Elektroniktechnologie der TH Ilmenau "Hybridtechnologie". Manebach 6.–9. 5. 1980 S. 91–96
21. DEÁK, I.: Investigations of deformations of hybrid structures. M. Sc. Thesis, Budapest, 1980
22. DEÁK, I.–LACZHÁZI, G.: Einige Bemerkungen über die Temperaturänderung verursachte Spannung und Deformationen der Träger von hybriden Schaltkreisen. In: Vorträge zum 4. Int. Frühjahrs-Seminar Elektroniktechnologie der TH Ilmenau "Hybridtechnologie". Manebach, 6.–9. 5. 1980 S. 106–113.
23. KLEIN, W.: Didaktische Darstellung der Ätzverfahren, Auftrag- und Abdampfverfahren zur Herstellung elektronischer Bauelemente. Wissenschaftliche Arbeit 1979, Lehrgebiet Feinwerktechnik, Universität Karlsruhe
24. DIETRICH, R.: Die Prüfung der gedruckten Leiterplatten im Fertigungsablauf von der Platte bis zur bestückten Baugruppe. Studienarbeit 1979. Lehrgebiet Feinwerktechnik, Universität Karlsruhe
25. ROSCH, A.: Spannungs- und Dehnungsverhalten von durchkontaktierten Bohrungen in gedruckten Leiterplatten bei großen Temperaturschwankungen. Studienarbeit 1979. Lehrgebiet Feinwerktechnik, Universität Karlsruhe
26. SEEMANN, B.: Experimentelle Ermittlung von Verformungsbeiwerten von Multilayer-Leiterplatten bei statischen zentrischen Lasten und Randlasten. Studienarbeit 1980. Lehrgebiet Feinwerktechnik, Universität Karlsruhe
27. FEIERTAG, R.: Untersuchungen von Multilayer und Dickschichtschaltungen mit Echtzeitholographie in: Optoelektronik in der Technik, Herausgeber W. Waidelich, Springer-Verlag, Berlin, Heidelberg, New York 1982, S. 59–62
28. FEIERTAG, R.: Holographische Untersuchungen von Dickschichtschaltungen und Mehrlagenschaltungen. Tagungsband des 26. Int. wiss. Kolloquiums der Technischen Hochschule Ilmenau/Thüringen 1981, S. 177–178

29. HAJDÚ, I.–PINKOLA, J.–TÓTH, E.: Erfahrungen bei Prüfungen an gedruckten Schaltungen. Tagungsband des 26. Int. wiss. Kolloquiums der Technischen Hochschule Ilmenau/Thüringen 1981, S. 163–167
30. LOWINSKI, W.: Untersuchung der Temperaturverformung von Mehrschichtleiterplatten unter elektrischer Last. Studienarbeit am Lehrgebiet Feinwerktechnik der Universität Karlsruhe 1981
31. HAJDÚ, I.–BÁNLAKI, P.–PINKOLA, J.–TÓTH, E.: Methods for testing printed circuits. Fifth International Spring Seminar on Electronics Technology, Prenet (CS) June 1982. Printed in the proceedings of the seminar, p. 101–104.
32. TÓTH, E.–BÁNLAKI, P.–HAJDÚ, I.–PINKOLA, J.: Usage of SIMS and Auger methods in the production of multilayer boards. Ibid. p. 65–70
33. GERSTENMAYER, G.: Technology for multilayer printed circuit boards. Dr.-Ing. Thesis, Budapest, 1982.
34. FEIERTAG, R.–TRUNDT, M.: Echtzeitholographie mit dem Dauerstrichlaser bei Schwingungsuntersuchungen. Tagungsband Laser 83-Opto-Elektronik, Springer-Verlag, Berlin, Heidelberg, New York 1984 p. 212–16
35. FEIERTAG, R.: Holographic Methods for testing electronic components. Proceedings of the Symposium on Electronics Technology, Budapest, September 1983. OMKDK-Technoinform, Budapest, 1984.
36. FEIERTAG, R.: Messungen in der Elektronik mit Echtzeitholographie. Vortrag auf dem DAAD-Kolloquium an der Technischen Universität, Budapest, on 29. Oct. 1982
37. AMBRÓZY, A.: Investigations of electronics technology in a BRD-Hungarian cooperation, at the above meeting
38. SPENCER, J. L. et al.: New quantitative measurements of IC stress introduced by plastic packages. Proceedings of the IRPS, IEEE, New York 1981, p. 74–80

Prof. DR. András AMBRÓZY H-1521 Budapest
Prof. Dr. Rainer-Maria FEIERTAG D-5600 Wuppertal 1, Fuhlrottstraße 10