HIGH-SPEED A/D CONVERSION

J. CSERNÁK

Department of Microwave Telecommunication,
Technical University, H-1521 Budapest

Received Jan. 2, 1984

Presented by Prof. Dr. I. Bozsóki

Summary

Recently high-speed A/D converters are applied in increasingly more fields of data processing. On the one hand, it has been caused by the technological development and on the other hand, the digital method gives many new very convenient possibilities in signal processing. The high-speed (10 Mbit/sec) converters can be considered as the usual medium speed converters, in which improved devices are used, but there are many new solutions that use components becoming general in microwave techniques. The paper intends to survey the new trends in system elements and to examine some important circuit problems.

Introduction

The development of the communication and measurement has been exerting pressure on the circuit designers to increase the speed and accuracy of a—d converters in the last two decades. Designers have tried to fulfil the extreme expectation by different principles. In this way, accurate but slow, and fast but inaccurate converters have been developed.

Eagerness of the system designers have disturbed that idyllic state, and 9 bit resolution and 25 MHz word rate do not seem to be unusual nowadays. These expectations have been brought by the improvement of the digital techniques that is the 200 Mbit/s information can be processed effectively.

Circuit designers can choose of several principles and devices. The component makers can be classified in two groups whether they have leading monolythic technology or not, i.e. this classification determines the principle of the operation of converters.

Converter with leading monolithic technology

In this case the flash (parallel) converters are prevailing. The converter shown in Fig. 1, consists in n bit case $2^n - 1$ of comparators biasing with resistor chain, intermediate latch and decoder logic for the output code (binary or Gray). Using latches between the comparator array and the decoder logic is not

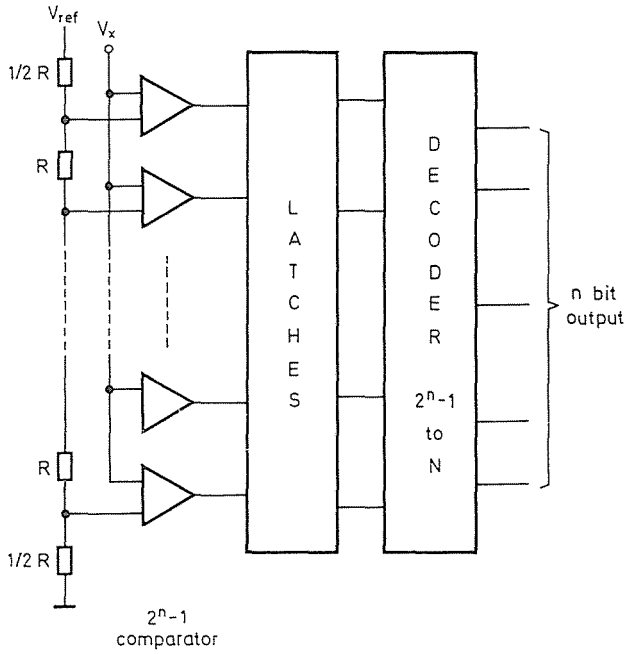


Fig. 1

only an elegant resolution but inevitable as well, because the different propagation time of the decoding elements can cause serious troubles. To sense the order in 8 bit case need 255 comparators and a rather complicated decoder logic. This converter built up of SSI circuits could show noticeable volume and power consumption. Only the very large-scale integration can give solution. The best known bipolar monolithic converter is made by TRW (3). The other developing direction could be the CMOS (SOS) technology which results 8 bit, 15 Mword/s specifications.

Converters without leading technology

No one can risk its reputation with the proclaim that he uses 255 discrete comparators. Fifteen year old principles became revived and newly evaluated.

Multi-stage parallel (subranging) A/D converters

A two-stage converter of j + k bit is illustrated in Fig. 2. The signal starting at the input reaches the sample holder and then a j bit parallel converter. Generally j means 3 or 4 bits. The result of the conversion is written into output

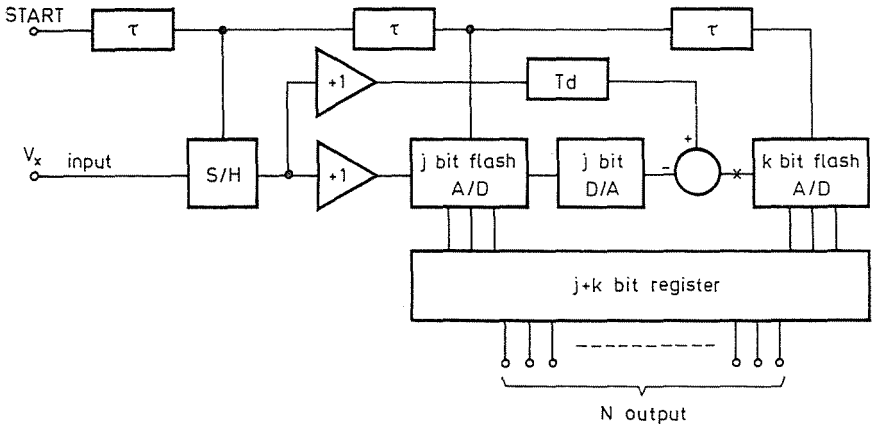


Fig. 2

register and afterward is reconverted into analog form by a j bit D/A converter. This voltage is subtracted from the input voltage and the result is converted by the second stage. The result of this parallel (k bit) converter is also stored into the output register. In Fig. 3 the operation is illustrated in the voltage scale.

The conversion speed can be increased by using sample holder at the input of the second stage. In this case the first stage can convert the new value, while the second is converting the old difference.

As a matter of fact, that converter can be considered as a two stage converter which uses only the first stage, and feed-backing the analog difference the second part of the input value is produced (9).

The typical performance in this category is of 9 bits resolution, 20 Mword/s.

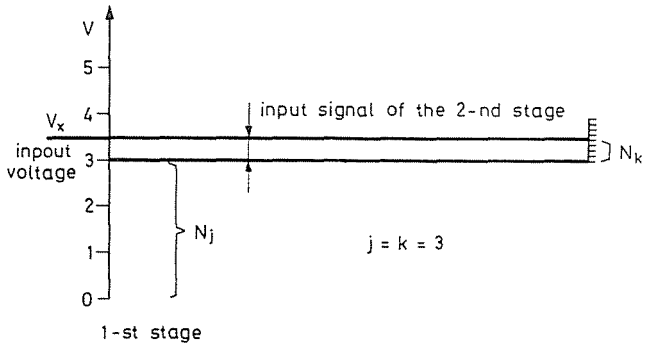


Fig. 3

Cascade or serial converter

The block diagram of a cascade converter is shown in Fig. 4 and its operation is illustrated in Fig. 5. This converter is built of uniform elements of each bit, connected serially. The transfer function of an element is:

$$V_{i+1} = -2|V_i| + V_R$$

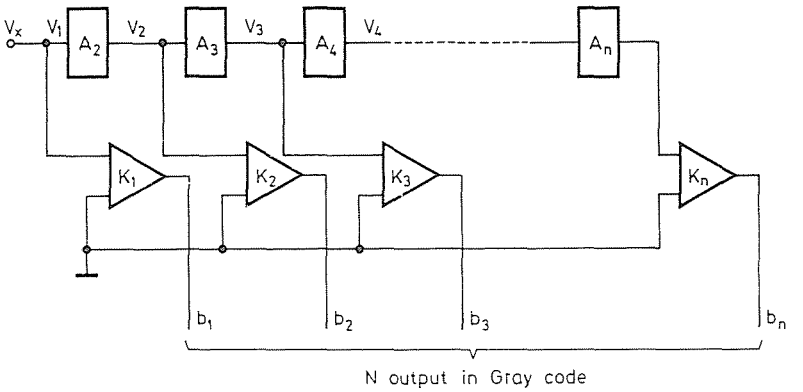


Fig. 4

where V_{i+1} and V_i are input voltages to the stage number $i+1$ and i, respectively, and V_R is the signal range. The first stage can be described simply:

$$V_1 = V_x .$$

Comparators give the digital output:

$$b = 1 \qquad \text{when } V_i > 0,$$
$$b = 0 \qquad \text{when } V_i < 0.$$

The simplified circuit of a building block is shown in Fig. 6.

It is to be mentioned that this algorithm can be realized also by microwave-carrier (11), where the baseband signal voltage is replaced by the carrier amplitude and the microwave-carrier phase subtitutes for the baseband signal polarity.

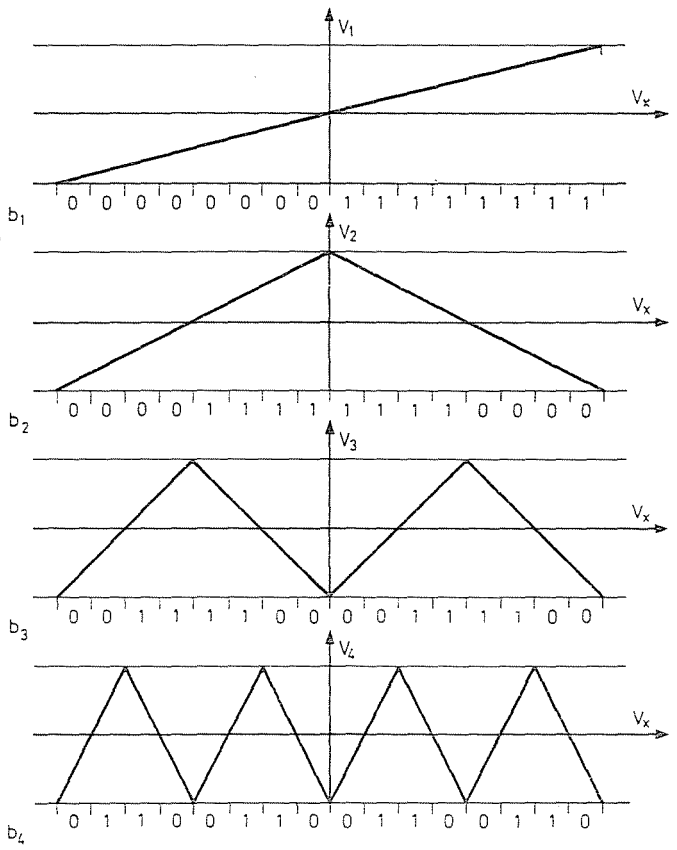
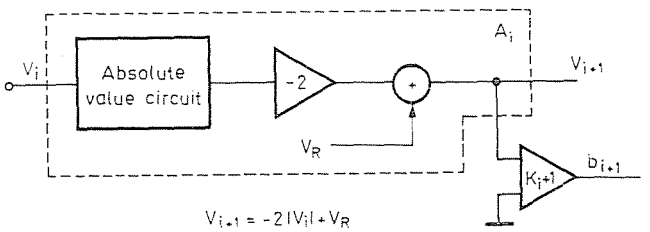


Fig. 5



$b_i = 1 \quad V_i > 0$

$b_i = 0 \quad V_i < 0$

Fig. 6

Conclusions

Owing to the fact that we do not dispose over proper monolithic technology, we had to choose from the second group of the principles.

Practical limitations of the settling-time of the operational amplifiers make the cascade converter unsuitable for very high-speed operation, however there are some solutions to improve performance (10).

The subranging method was chosen because it is functionally simple. The fundamental problem is the noise generated by the digital circuit. Practically ECL circuits have to be used in the logic part to avoid uncompensateable impulse noise in the analog lines. The solution of grounding and separation are the main developing problems.

References

1. ZUCH, E.: "Put video A/D converters to work" Electronic Design, August 2, 1978.
2. Quantisierer mit 100 MHz-Abtastrate Elektronik Informationen Nr. 5. 1982.
3. LAMMERT, M.—OLSEN, R. K. 1-um process shrinks and speeds up flash converter. Electronics, May 5, 1982.
4. LONSBOROUGH, M.: A 6-bit monolitic video flash converter. Microelectron Reliab. Vol. 21, No. 6. 1981.
5. ZUCH, E.: Video analog-to-digital conversion. Electronic Design, April 12, 1978.
6. KESTER, W. A.: PCM Signal Codecs for Video Applications. SMPTE J. November, 1979.
7. DR. DAVIES, C.: High-speed analogue-to-digital conversion techniques. Electronic Engineering, May, 1976.
8. 9-bit 20 MHz Video A/D Converter. Analog Dialogue, No. 3. 1982.
9. Dr. Er. TÜTÜNCÖOGLU, E.: Schneller 8-bit-ADU ohne D/A-Umsetzung. Elektronik 25/26. 1981.
10. FIEDLER, U.—SEITZER, D.: A High-Speed 8-bit A/D Converter Based on a Gray-Code Multiple Folding Circuit. IEEE Journal of Solid-State Circuits No. 3. 1979.
11. FISHER, R. E.: A 1200-Megabit per Second Microwave-Carrier Gray-Code Analog-to-Digital Converter. IEEE Transactions on Microwave Theory and Techniques No. 8. 1968.

Dr. József CSERNÁK H-1521 Budapest