SWITCHING PROCESSES IN THE METAL-INSULATOR-SEMICONDUCTOR THYRISTOR (MIST)

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Summary

The switching process in the MIST, having a metal-tunnel oxide-n layer-p layer structure, is discussed. The MIST is modelled as a two-active device structure, with a bipolar transistor and an amplifying MIS structure. The gate pulse startes the transient process of the bipolar transistor, the collector current of the transistor builds up the inversion charge of the MIS. The device switches in, if the inversion charge reaches its critical value. The delay time caused by the inversion charge is calculated and measured.

Introduction

About ten years ago Yamamoto presented a new semiconductor device, which consisted of a structure of metal-tunneling oxid-*n* type silicon-*p* type silicon. This device (called MISS) had an *S*-type negative resistance I—V characteristics [1]. Soon other research groups also presented their results in the investigation of the new device [2, 3, 4]. If an ohmic contact is made also to the *n*-type layer, the I—V characteristics can be influenced by biasing the *pn* junction into forward direction, and the device behaves like a thyristor [5—11]. Therefore this three-terminated device has been named metal-insulator-semiconductor thyristor (MIST). Relatively little attention have been paid, however, to the transient processes in the MISS devices [3, 12]. Some calculations for the transient processes in the MIST were presented but they were connected with the d.c. characteristics of the device, without discussing the physical processes taking place in it [13].

Theory of switching in MIST device

The structure and the band diagram of the MIST are shown on Fig. 1. The static I—V characteristics are shown in Fig. 2. The device has a high and a low impedance state. In the high impedance state at the surface there is a deep depletion layer, and the minority carriers (holes), generated in this layer, can

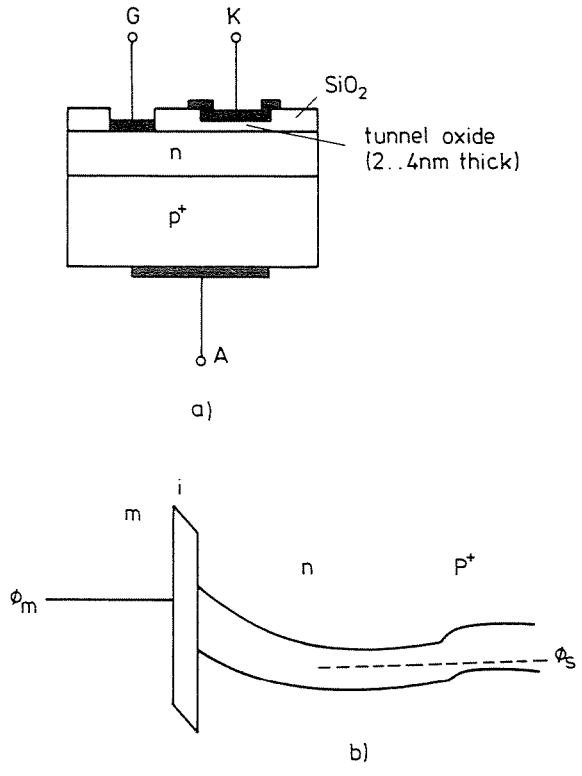

Fig. 1. Schematic structure and band diagram of the MIST

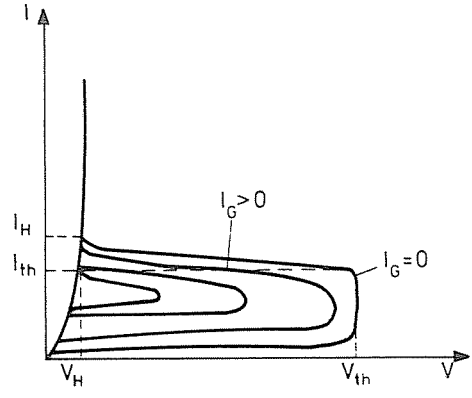

Fig. 2. I—V characteristics of the MIST

cross the oxide layer by tunneling. However, the majority carriers, generated in the depletion layer, flow to layer n, and bias junction pn into forward direction. If the surface depletion layer approximates junction pn, a large hole injection current starts to flow from the layer p^+ across the layer n, to the oxide-semiconductor interface. As this current is by many orders of magnitude higher than the thermal generation current, it forms an inversion layer at the oxide-semiconductor interface. As a result of the inversion layer charge, the field strength increases significantly in the oxide, which in turn leads to a high electron tunnel current from the metal into the semiconductor. These electrons bias junction pn even more into the forward direction etc. Thus a positive feedback loop is established and if the loop gain of this feedback loop is larger than unity, the surface depletion layer collapses and the device switches to the low impedance state.

In the low impedance state there are two significant charges of holes in the device. At the oxide-semiconductor interface there is an inversion charge, consisting of holes. In the neutral part of layer n the injection of holes from the layer p^+ produces a diffusion charge, which is proportional to the current flowing through the device. During the transient processes these charges must be built up at switch-on and must be eliminated during switch-off.

There are some possible methods to switch on the MIST

a) D. C. supply voltage on the cathode, and the gate is driven by a pulse;
b) D. C. voltage on the gate, and the cathode is driven by a pulse;
c) both gate and cathode are driven by a pulse.

The switching process in cases *b)* and *c)* are similar to the switching process in the two-terminal MISS device [12]. The case *a)* will be discussed in detail.

In order to be able to switch off the MIST after the gate pulse is off, the supply voltage and the load resistor must fulfill the condition:

$$\frac{V_{CC}-V_H}{I_H} < R_L < \frac{V_{CC}-V_H}{I'_H} \tag{1}$$

where V_{CC} is the supply voltage, V_H is the holding voltage, I_H the holding current at zero gate current and I'_H is the holding current reduced by the gate bias current. If Eq. (1) holds, the possible current across the device after terminating the gate pulse is smaller than the static holding current, therefore the device cannot stay in the low impedance state, but switches out after a while.

Applying a rectangular gate current pulse results in a cathode current shown in Fig. 3. First the current slowly rises. After a delay time t_d, the inversion layer reaches its critical value, and the device switches to the low impedance

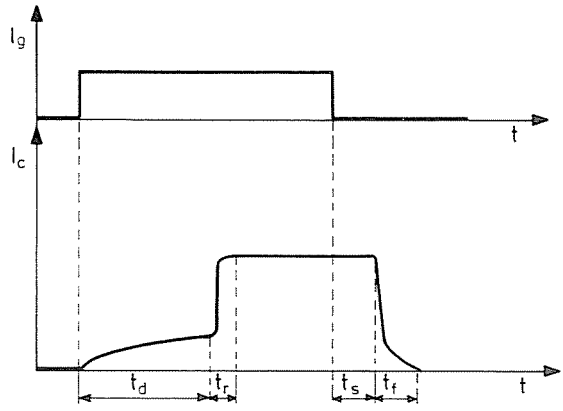

Fig. 3. Switching current waveform of the MIST with a pulse gate current drive

state. In the meantime, it is necessary to build up the diffusion charge and to increase the inversion charge. Therefore there is a rise time t_r, during which the current rises to the value corresponding to the on state. After switching off the gate current, the diffusion charge is reduced by recombination but this is partly compensated by the electrons tunneling from the metal into layer n. The inversion charge is decreased by the hole tunnel current across the oxide but this is partly compensated by the hole current injected from layer p^+ to the oxide-semiconductor interface. Therefore this saturation time is longer than it would follow from considering the recombination process alone.

After this time the device switches to the high impedance state (fall time t_f). The decrease of the current is first quicker, during this time the internal feedback loop switches off the device, then a slower second phase follows, where the current flow is mainly due to capacitive effects. In the followings a simplified calculation is presented to determine the first phase, the delay time.

The MIST can be considered as combination of two active devices: a bipolar transistor and an amplifying MIS diode [4]. The bipolar transistor is composed by the layer p^+ as emitter, the layer n as base and the surface depletion layer as collector. The gate pulse starts the switch-on process of this transistor. The collector current of this transistor charges the inversion layer capacitance. If the charge in the inversion layer reaches a critical value, the injection of electrons from the metal into the semiconductor, and thus also the regenerative feedback process starts and the delay time ends. For the diffusion charge, Q_B can be written as:

$$I_B = \frac{Q_B}{\tau_p} + \frac{dQ_B}{dt} \tag{2}$$

where I_B is part of the gate current effectively influencing the base diffusion charge. As the area of the emitting junction *pn* is much larger than the area of the collecting tunnel oxide, there is actually a parasitic diode connected parallelly to the MIST, and a large part of the gate current flows through this diode. The electron current injected into layer p^+ and into the depletion layer of junction *pn* reduces the value of I_B as well.

If $Q_B(o)=0$, that is, at the beginning of the switching process there isn't any diffusion charge, the solution of (2) is

$$Q_B(t)=I_B\cdot\tau_p(1-e^{-t/\tau_P}). \tag{3}$$

The collector current, that is, the hole current, collected by the surface depletion layer, is proportional to the (base) diffusion charge, as is it known from the theory of bipolar transistors:

$$I_C=\frac{Q_B}{T_C}=\frac{I_B\cdot\tau_p}{T_C}(1-e^{-t/\tau_P}) \tag{4}$$

where T_C is the collector time constant. It depends upon the thickness of the neutral part of layer *n*.

$$T_C=\frac{(W-W_s)^2}{2D_p} \tag{5}$$

where W is the total thickness of layer *n*, and W_s is the thickness of the surface depletion layer.

$$W_s=\left(\frac{2\varepsilon_s}{qN_D}\right)^{1/2}U_{CC}^{1/2} \tag{6}$$

where N_D is the donor concentration and ε_s the dielectric constant of the semiconductor. If U_{CC} is higher, T_C is lower and the increase of the collector current is quicker.

The inversion layer charge is increased by I_C and decreased by the hole tunnel current across the oxide. Let's suppose, that this tunnel current is approximately proportional to the inversion charge. Then for the inversion charge, Q_i can be written as

$$\frac{dQ_i}{dt}=I_C(t)-\frac{Q_i}{T_i} \tag{7}$$

using Eq. (4) for $I_C(t)$, and taking into account, that in equilibrium ($t\to\infty$) $I_C=B_1\cdot I_G$ where B_1 is the grounded emitter current amplification factor of the bipolar transistor, Eq. (7) can be rewritten as

$$B_1 \cdot I_G (1 - e^{-t/\tau_p}) = \frac{dQ_i}{dt} + \frac{Q_i}{T_i} \tag{8}$$

where it was used, that

$$\frac{I_B \tau_p}{T_C} = B_1 \cdot I_G . \tag{9}$$

Taking into account that at the beginning of the switching process there is already a possibility of a certain charge in the inversion layer, the solution of Eq. (8) is

$$Q_i(t) = B_1 \cdot I_G \cdot T_i \left(1 + \frac{\tau_p}{T_i - \tau_p} e^{-t/\tau_p} + \frac{T_i}{\tau_{p-T_i}} e^{-t/T_i} \right) + \\ + Q_i(o)\, e^{-t/T_i} . \tag{10}$$

Let's consider the case where at the given supply voltage, the device just reaches statically the switch in condition. ($I_G = I_{GH}$, where I_{GH} is the gate current, just enough to switch on the device at a given supply voltage.) In this case Q_i reaches Q_{TH}, the charge necessary to switch on the device after a very long time. After a long time $dQ_i/dt \approx 0$, $Q_i = Q_{TH}$, thus from Eq. (7) it can be written:

$$T_i = \frac{Q_{TH}}{I_C} = \frac{Q_{TH}}{B_1 \cdot I_{GH}} . \tag{11}$$

If $I_G > I_{GH}$, considering that $Q_i(t_d) = Q_{TH}$, with Eqs (10) and (11) it can be written:

$$\frac{I_{GH}}{I_G} = \frac{1 + \frac{\tau_p}{T_i - \tau_p} e^{-t_d/\tau_p} + \frac{T_i}{\tau_p - T_i} e^{-t_d/T_i}}{1 - \frac{Q_i(o)}{Q_{TH}} e^{-t_d/T_i}} . \tag{12}$$

t_d can be determined from Eq. (12) as a function of I_G. I_{GH} can be determined from the I—V characteristics. However, the values of $Q_i(o)$ and T_i are not known. Measuring t_d as a function of I_G, the theoretical curve given by Eq. (12) can be fitted to the measured values by a proper choice of τ_p, T_i and $Q_i(o)/Q_{TH}$.

Figure 4 shows the measured delay times (smooth line) versus the gate current for a MIST with the following parameters: $V_{th} = 11$ V, $I_{th} = 1$ mA, $V_H = 1{,}2$ V, $I_H = 1.5$ mA. The value of the series resistance was 9.2 kohm. The parameter of the curve was U_{CC}, the supply voltage. At $U_{CC} = 9$ V some points of the curve were calculated with the following values:

$\tau_p = 1.4\ \mu s$, $T_i = 2.8\ \mu s$, $Q_i(o)/Q_{TH} = 0.5$
$I_{GH} = 300\ \mu A$

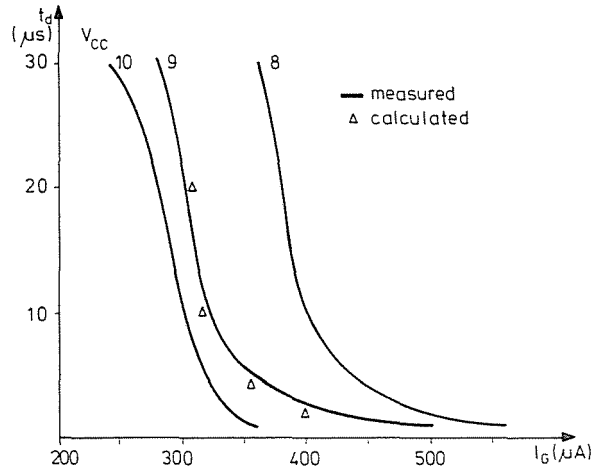

Fig. 4. Measured and calculated delay times for a MIST

These are realistic values. The calculated values of the delay time are denoted by little triangles. The measured and calculated values fit quite well, with the exception of very low and very high delay times. At high delay times (low value of gate current) the electron tunnel current and the surface generation current, omitted in the calculation, will not be negligible in comparison to the gate current, and reduce the delay time.

Increasing the gate current, the current of the bipolar transistor, that is, the current flowing across the device during the first phase of the transient waveform in Fig. 3 will increase, and can reach the maximum possible current across the device, before the inversion charge reaches its critical value. In this case the second phase t_r disappears, and the switch-on transient is determined by the bipolar transistor, with the well-known formula

$$t_d = t_r' = \tau_p \ln \frac{n-0.1}{n-0.9} \tag{13}$$

where n is the degree of current overdrive

$$n = \frac{I_{c\max}}{B_1 \cdot I_G}. \tag{14}$$

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