PRACTICAL EDUCATION IN IC TECHNOLOGY AT THE TECHNICAL UNIVERSITY, BUDAPEST

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Summary

Thirty lessons semiconductor technology laboratory exercises and pilot plant exercises for undergraduate students are described. The material of standard exercise is demonstrated. Some analysis is given of how it connects the given knowledge to the demands of industry.

Introduction

In the past ten years, the Department of Electronic Devices at this University had the possibility to build up a semiconductor technology laboratory sponsored by TUNGSRAM Co. The more important elements of our equipment park are:

2 four tube diffusion furnaces
1 mask aligner
5 laminar flow boxes
1 vacuum evaporator
1 sputter machine
1 Talystep measuring instrument.

The undergraduate students have to produce MOS IC by themselves during their laboratory exercises.

After introducing the students to the theoretical basis of semiconductor technology, — approximately the material presented by Gandhi, Donovan, Grove — the students get their silicon wafers, and they have the possibility to get into personal contact with the technical problems of MOS processing. The students have to do manually the process steps from checking the wafer till the last measurement on the packaged IC.

Two main types of laboratory exercises can be distinguished:

1. The standard exercise with invariable task — producing SSI MOS IC, 20 students a year.

2. The pilot plant exercises with different tasks for each of the 8 students a year.

The personal conditions are: 6 staff members of the chair, 1 technician, 3 laboratory assistants.

While the first-type exercises are done under supervision by teachers, in the second type the student only consults his (her) tutor. The standard exercise is done in semester 8, and the individual exercises are done by the more skilled students in semesters 9 and 10.

This time we want to present our activity and experiences, especially with the standard type, not mentioning the numerous diploma works, postgraduate (doctoral) and other research activities.

Standard laboratory exercise

In the last four years, the standard laboratory exercise has been to produce an SSI MOS IC, which also has been designed by students. The circuit diagram of a chip is shown in Fig. 1a.

One chip contains 2 four input NOR-gates, with different load transistors, and in the middle a four-segment MOS-transistor. The time required to complete this work is about 30 hours, divided to five parts i.e. five days.

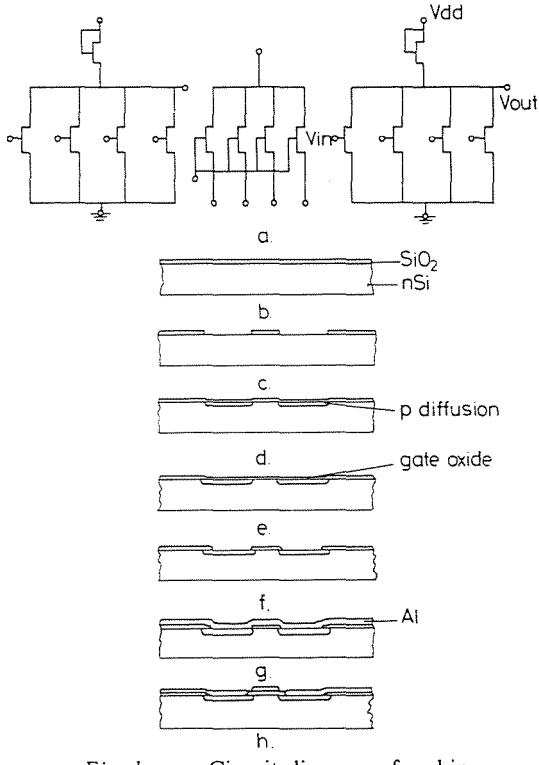

Fig. 1. a — Circuit diagram of a chip
b through h cross sections of a transistor in different phases of the process

The tasks of the exercises

1st day

Checking the resistivity and type of the wafers. First chemical cleaning. Field oxide growing (500 nm): Measuring the oxide thickness by Talystep and by the interference color scale.

Cross sections of a MOS on the chip are shown in Figs 1b to h. Actually see Fig. 1b.

2nd day

Photolitography and window etching for the source-drain diffusion by applying the first mask (Fig. 2. Also see Fig. 1c).

Predeposition of boron from BN diffusion source. Quality testing of predeposition by resistivity and junction depth measurements.

Drive-in diffusion (Fig. 1d).

Quality testing of diffusion as before.

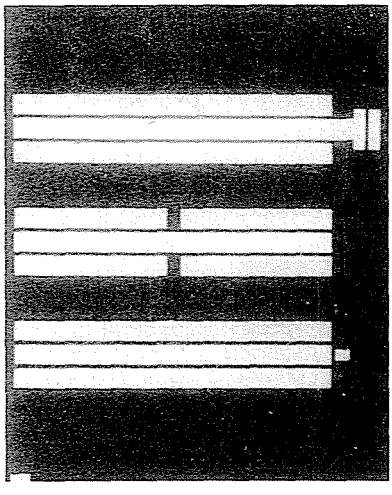

Fig. 2. Mask for diffusion

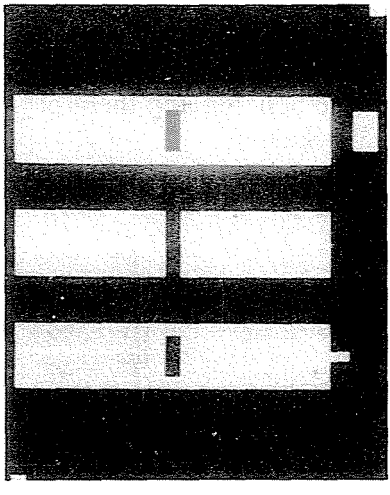

Fig. 3. Mask for the gate windows

3rd day

Photolithography and window etching for the MOS oxide applying the second mask (Fig. 3, also see Fig. 1d). Growing the gate-oxide (80 nm) in HCl cleaned quartz tube (Fig. 1e).

Annealing.

Investigation of C—V characteristics of the control wafer's MOS capacitors.

Evaluation of HF and quasi-static C—V curves. Using Götzberger curves, the students have to determine the flat-band capacitance, flat-band voltage, the doping concentration of the silicon surface, the oxide thickness and the density of surface states.

4th day

Photolithography and etching the contact windows by the third mask (Fig. 4 and Fig. 1f).

Evaporation of aluminium (Fig. 1g), photolithography and etching the metallization by the fourth mask (Fig. 5 and Fig. 1h).

5th day

Last annealing.
Transistor characteristic measurements on wafers.
Painting the faulty chips.
Scribing, breaking the wafers into chips.
Die bonding and thermocompression bonding.
Packaging.
Measuring the IC characteristics.
The photo in Fig. 6 shows an uncapped device.

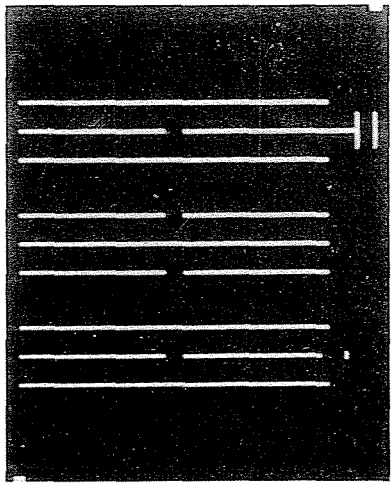

Fig. 4. Mask for the contact windows

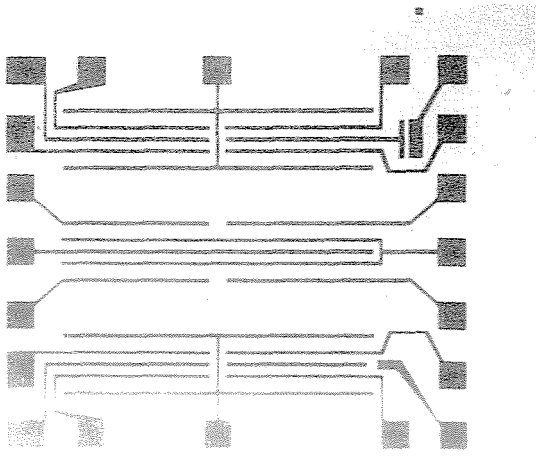

Fig. 5. Mask for the metallization

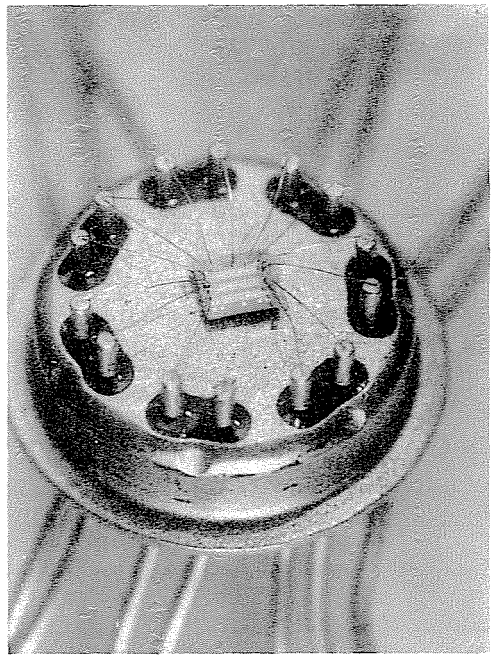

Fig. 6. A device after thermocompression

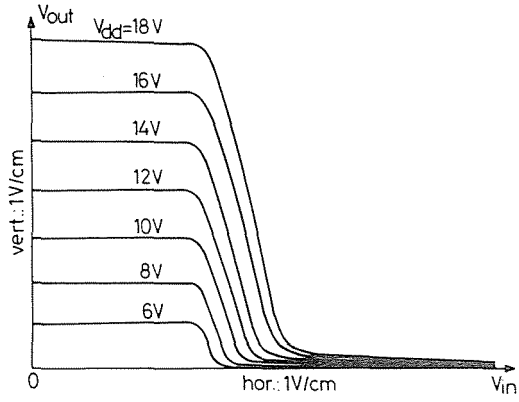

Fig. 7. Transfer characteristics of an inverter parametered by V_{DD}

In the last measurement the students have to determine the general MOS—FET parameters, the transfer characteristics of the inverter, and check the truth-table. They can find the threshold voltages of both transistors of the inverter from the transfer characteristics parametered by the supply voltage (Fig. 7).

Pilot plant exercises

After the 8th semester the students have to choose their task for the pilot plant exercise (9—10 hours a week).

Part of the students get a skill during the standard exercises. These participants have some practice in the field of different technological steps as:

Chemical cleaning;

Designing, doing, and checking the oxidation, the diffusion, evaporation, and photolithographic processes.

In the last few years the most interesting and effective topics were:

Development of sputter deposited tin dioxide layers as gas sensors;

Palladium gate MOSFET producing and calibration its hydrogen sensitivity;

Investigation of effects of chlorine incorporation into SiO_2 during thermal oxidation of silicon;

Examination of diffusion properties of polycrystalline silicon;

Schottky diode production;

MISS device research;

Pressure transducers;

pH-sensitive FET-s.

The students have to produce a written report and hold a 15-minute lecture about their work and results.

Conclusions

Utility of our laboratory exercises has been analyzed by:

1. Questioning graduate students engaged in semiconductor industry or research.
2. Conversations with graduate students working outside the semiconductor industry.
3. Conversations with the directors and middle-level managers of graduate students.

The results of our inquiry are as follows:

1. The absence of laboratory exercises would delay the good partnership between co-workers.
   The specialization of engineers in the industry prevents them from surveying the problematics of the whole technology in a short time, but some knowledge of the matter is desired. The knowledge of students transforms into more useable experience, strengthening the unity of theory and practice.
2. Those engaged in jobs apart from semiconductor technology use the skill acquired in exercises in the fields of microtechnics and pure material technique.

The teachers of the laboratory exercises find it a good pedagogical opportunity to suggest the students to do precise work. There are hundreds of elementary occasions to do one faulty step during the process, enough to a catastrophic issue.

In the past three years the average yield was about 60%. We are indebted to the assistants for their intentness during the exercises.

The university raises a feeling of gratification in the students by presenting them a part of good IC-s produced by themselves. Another part of IC-s is made use of in the semiconductor device measuring laboratory for exercises of younger students.

We finish with the last sentence of Senitzky's publication (1) "It is hoped that this knowledge will improve the professional competence of the student when he (she) graduates and becomes an electrical engineer".

Reference

1. SENITZKY, B.: "A Semiconductor Technology Course" IEEE Trans. Educ. E—23, pp. 213—218, November 1980.

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