# DESIGN PROBLEMS OF TRANSFORM CODERS FOR IMAGE TRANSMISSION

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## Summary

Some experiments have been undertaken with general coder circuit models. These experiments revealed the possibility that coders implemented by the use of adders only, are suitable for coding video signals in real-time operation. During the experiments the authors applied relatively small $N$ values, which is not always advantageous for transform efficiency. The applied components were of TTL-S and ECL-types. The parallel processing described in short in point 4, provides the possibility to code simultaneously a larger image section ($N$ above 4). In this way the development of VLSI integrated circuit, specially designed for transform coding purposes can be achieved. This type of development is being undertaken in several parts of the world.

## Introduction

The increasing information demand of society and the more economical utilization of transmission channels make more and more necessary the development of coding processes for digital transmission, that give relatively high bit rate compression factors. This problem is especially important for the transmission of video signals. A very promising process is the transform coding of video signals, which is essentially a given part of the more general field of image processing. Transform coding is in general a very complex process and only its real-time versions are appropriate for the purpose of digital image transmission. The realization of real-time operation is as yet in many cases only practicable by using parallel or pipeline processing. In this respect the importance to develop a fast algorithm is very great.

At present, especially for the digital transmission of TV-signals, the application of digital hybrid coders seems the most expedient. In these the nearly decorrelated transform coefficients are produced with a two-dimensional intraframe transform followed by interframe DPCM coding. The hybrid process promises bit rate compression ratios of about 1 : 40.

At the Department of Microwave Telecommunication of the Budapest Technical University an experimental work is under way to study the

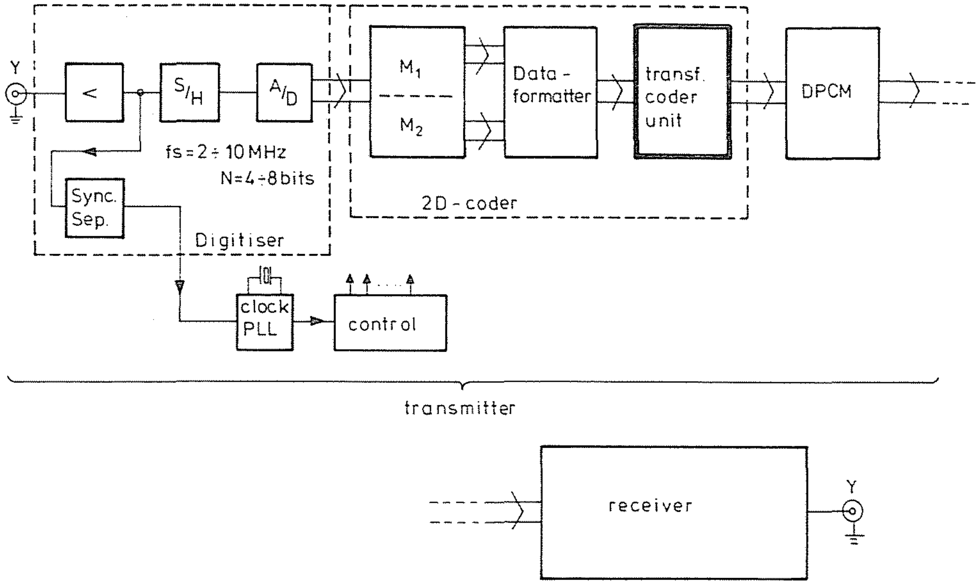


*Fig. 1*

practicable hardware of hybrid coders. The simplified block diagram of an experimental equipment is shown in Fig. 1. It is suitable to process colour — and monochromatic — TV-signals. Fig. 1 shows only the details of the transmitter side part of the intensity channel. In general the receiver side unit contains the same units, so it is sufficient to consider only the transmitter side. In the following only the designing problems of transform coding unit will be discussed. This has two fundamental parameters: the system complexity and/or the achievable operating speed. Both are determined essentially by

— the transform algorithm
— the architecture of the processor, and
— the employed technology/layout.

## Choice of the transform type

In the course of bandwidth reduction and/or bit rate compression let us assume for the applied transform coding process, that the $M \times M$ image array stored in a memory will be subdivided into $N \times N$ subarrays (Fig. 2) before transforming.

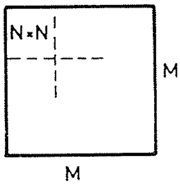


*Fig. 2*

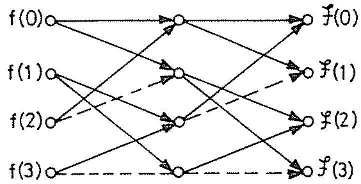


*Fig. 3*

In general, transforming requires numerous operations (addition, multiplication), that can be reduced by an appropriate algorithm. An alternatives to reduce the number of operations is to subdivide the total computation task into a series of repeatable computation steps. For Hadamard, transform, if $N=4$, this is:

$$\left.\begin{aligned}\mathfrak{f}(0)&=f(0)+f(1)+f(2)+f(3)\\ \mathfrak{f}(1)&=f(0)-f(1)+f(2)-f(3)\\ \mathfrak{f}(2)&=f(0)+f(1)-f(2)-f(3)\\ \mathfrak{f}(3)&=f(0)-f(1)-f(2)+f(3)\end{aligned}\right\}\quad \begin{array}{l}\text{the number of operations}\\ N(N-1)=12\end{array}$$

$$\left.\begin{aligned}a(0)&=f(0)+f(2) & \mathfrak{f}(0)&=a(0)+a(2)\\ a(1)&=f(0)-f(2) & \mathfrak{f}(1)&=a(0)-a(2)\\ a(2)&=f(1)+f(3) & \mathfrak{f}(2)&=a(1)+a(3)\\ a(3)&=f(1)-f(3) & \mathfrak{f}(3)&=a(1)-a(3)\end{aligned}\right\}\quad \begin{array}{l}\text{the number of operations}\\ N^{2}_{\log}N=8\end{array}$$

Fig. 3 shows the flow chart. Another alternative is the factorization of the transform matrix. For the previous case this is:

$$H_4=\begin{bmatrix}1&1&1&1\\1&-1&1&-1\\1&1&-1&-1\\1&-1&-1&1\end{bmatrix}=\begin{bmatrix}1&1&0&0\\0&0&1&1\\1&-1&0&0\\0&0&1&-1\end{bmatrix}\begin{bmatrix}1&1&0&0\\0&0&1&1\\1&-1&0&0\\0&0&1&-1\end{bmatrix}$$

In this case the number of operations is equal to one-half of the number of non-zero elements in the matrix factors. In Table 1 the number of required arithmetic operations for major transformations was collected, based on literary data.

The only one of the listed transform is the KLT which yields complete decorrelation among transforming coefficients. With the other transforms there is still a finite correlation between transform coefficients. Statistical analysis may point out, how far the individual transform process approximates

**Table 1**

| Transformation | Number of arithmetic operations | |
|---|---|---|
| | addition | multiplication |
| KLT Karhunen—Loeve | $N^2$ | $N^2$ |
| DFT discrete Fourier | $N^2_{\log}N$ | $N^2_{\log}N$ |
| HT Haar | $2(N-1)$ | $N/2$ |
| CHT complex Haar | $3N-4$ | $N+2$ |
| WHT Walsh—Hadamard | $N^2_{\log}N$ | – |
| ST Slant | $N^2_{\log}N+N/2-2$ | $2N-4$ |
| SHT Slant—Haar | $\updownarrow$ ... | ... |
| DCT discrete cos | $2N^2_{\log}N$ | $2N^2_{\log}N$ |
| | $\frac{3N}{2}({}^{2}_{\log}N-1)+2$ | $N^2_{\log}N-\frac{3N}{2}+4$ |
| | $\vdots$ | $\vdots$ |
| DST discrete sin | $2N^2_{\log}N$ | $2N^2_{\log}N$ |
| DSCT discrete sin – cos | $N^2_{\log}N$ | $N^2_{\log}N$ |

the optimal KLT. The results of such analyses are presented in Fig. 4 ([2], [3]). This is one of the essential view-points for the choice of transform.

For a single arithmetic operation the available time is:

$$t_0 = \frac{T_K}{\frac{M^2}{N^2} - L} \tag{1}$$

where $T_K$ is the frame time and $L$ is the number of operations to be completed. For parallel and pipeline processing the available time is more:

$$t = P \cdot t_0 \tag{2}$$

where $P$ is the number of simultaneously operating units. On the basis of this short summary it is obvious that with respect to the demand on real arithmetic operations and to convergence, the WHT and the DCT give the best realization conditions. With its discrete sawtoothlike basic vector, ST is suitable to represent gradual brightness changes in an image line and the number of its required operations is also advantageous. The DFT and the CHT require complex arithmetics.

Among arithmetic operations multiplication has a high time requirement, while addition has not. From the available procedures merely the *WHT* contains additions only. Thus for the realization of real-time coding units,

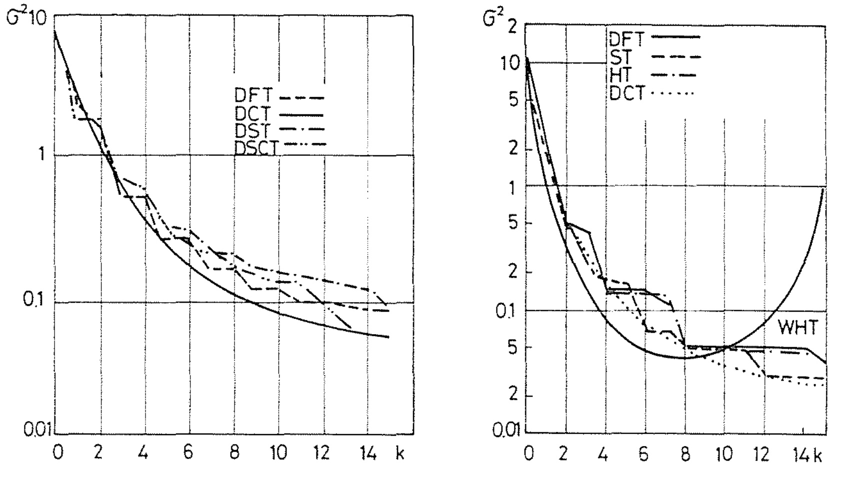


*Fig. 4*

either the development of an algorithm is needed which contains additions only, or the *WHT* has to be employed directly. In the case of an algorithm which contains also multiplications, only the realization of coders with parallel or pipeline processing makes real-time operation possible.

## Coder units realized with adders

In the following we will describe several coding processes and/or realizations of coders, which contain only adders. In the course of our experiments we implemented the circuit models of these.

### *WHT*

Walsh—Hadamard transform is based on Hadamard matrix, the value of its elements are plus and minus ones. The simplest construction of Hadamard matrix is

$$H_{2N} = \frac{1}{\sqrt{2}} \begin{bmatrix} H_N & H_N \\ H_N & -H_N \end{bmatrix} \tag{3}$$

where $H_N$ is Hadamard matrix of the $N \times N$ array for $N = 2^n$, if $n$ is an integer. The Hadamard matrix is orthogonal, that is:

$$H_N H_N^T = I \tag{4}$$

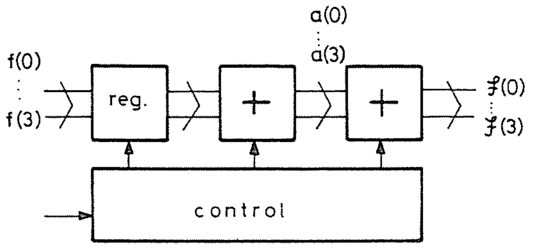


*Fig. 5*

The transform unit is realized by using blocks for $N=4$. In this case the transform matrix is identical with $H_4$ described in point 2. Fig. 2 shows the flow chart and Fig. 5 shows the block diagram of the coder unit. The ordered data is received by registers. The additions are realized in two-complement codes. The control unit provides the forming of two-complements and/or the setting of operations according to matrix elements. First 4 bit adders, type SN 7483, were used in the circuit model. This coder unit operated well up to an 8 MHz sampling frequency and it is suitable for processing video signals with a complete bandwidth if supplied with faster components (TTL-S, ECL; e.g.: SN 74S181, and/or MC 10181).

## *DCT*

Two procedures have been employed, both of them containing only adders and/or PROM's.

*Realization with the arcsin transform*

The DCT is defined as:

$$\mathfrak{f}(0)=\frac{1}{\sqrt{N}}\sum_{j=0}^{N-1} f(j) \tag{5}$$

$$\mathfrak{f}(k)=\sqrt{\frac{2}{N}}\sum_{j=0}^{N-1} f(j)\cos\frac{(2j+1)k\pi}{2N}; \quad k=0, 1, \ldots, N-1$$

and (6)

$$|f(j)|\leq 1$$

where $f(j)$ is the input data vector for $j=0, 1, \ldots, N-1$. Let us define vector $g(j)$, as

$$g(j)=\arcsin f(j) \tag{7}$$

then $f(j)$ can be written in the form

$$f(j) = \sin g(j) \tag{8}$$

substituting this into $f(k)$, we receive:

$$\mathfrak{f}(k) = \sqrt{\frac{2}{N}} \sum_{j=0}^{N-1} \sin\,[g(j)] \cos \frac{(2j+1)k\pi}{2N} \tag{9}$$

And using the trigonometric relation

$$\sin\alpha \cdot \cos\beta = \frac{1}{2}\,[\sin(\alpha+\beta) + \sin(\alpha-\beta)] \tag{10}$$

we receive:

$$\mathfrak{f}(0) = \frac{1}{\sqrt{N}} \sum_{j=0}^{N-1} \sin g(j)$$

$$\mathfrak{f}(k) = \frac{1}{\sqrt{2N}} \sum_{j=0}^{N-1} \left\{ \sin\left[ g(j) + \frac{(2j+1)k\pi}{2N} \right] + \sin\left[ g(j) - \frac{(2j+1)k\pi}{2N} \right] \right\} \tag{11}$$

According to the latter equation it is possible to realize the transform by the above-mentioned process using $4N-1$ real additions and $2N$ table lookups. Fig. 6 shows the block diagram of the unit. We used ECL components in the circuit-model (MC 10181, MC 10149).

*Realization with WHT*

Let the *DCT* and the *WHT* transforms of column-vector $f(j)$ be written in the following form:

$$\tilde{\mathfrak{f}}_{DCT}(k) = \tilde{C}_N \cdot f(j) \tag{12}$$

$$\tilde{\mathfrak{f}}_{WHT}(k) = \tilde{H}_N \cdot f(j) \tag{13}$$

where symbol ˜ stands for the bit-reversed order.

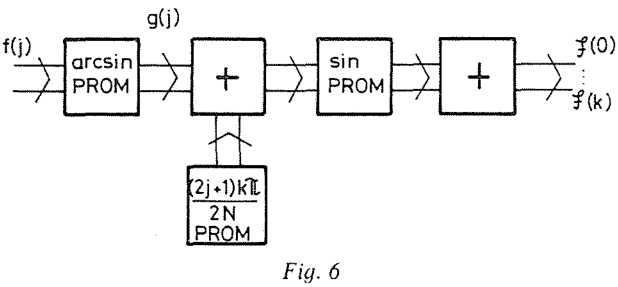


*Fig. 6*

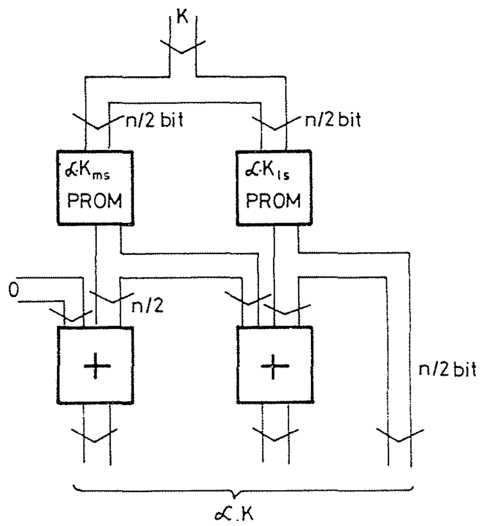


*Fig. 7*

Taking into account, that the Hadamard matrix is orthogonal, we can write

$$\tilde{f}_{DCT}(k)=\tilde{C}_N\tilde{H}_N^T\tilde{H}_N f(j)=\tilde{C}_N\tilde{H}_N^T\tilde{f}_{WHT}(k) \tag{14}$$

where

$$CT_N=\tilde{C}_N\tilde{H}_N^T$$

is the transform matrix. According to this form we can realize the *DCT* using the terms of *WHT*. We can use the following number representation to eliminate multiplications. Let us assume an $n$-bit integer, $K$, where most and least significant $n/2$ bit parts are $K_{ms}$ and $K_{ls}$ respectively. We can then write the number $K$, as:

$$K=K_{ms}\cdot 2^{n/2}+K_{ls} \tag{15}$$

Let $\alpha$ be an $r$-bit fractional binary number less than 1. The product of the two numbers is:

$$\alpha K=\alpha K_{ms}2^{n/2}+\alpha K_{ls} \tag{16}$$

In general the two parts on the right side are $(n/2+r)$-bit numbers with $r$ and $(r-n/2)$ fractional bits. Multiplication by $\alpha$ is performed by using PROM's, thus, this process is realized by using adders only, as is seen in Fig. 7. The required PROM-size is:

$$\left(mx2^{n/2}x\frac{3}{2}n\right)\text{bit} \tag{17}$$

where $m$ is the number of multiplications. The matrix $CT_N$ for $N=8$ is given by

$$CT_N=\begin{bmatrix} 1{,}0 & & & & & & & \\ & 1{,}0 & & & & 0 & & \\ & & 0{,}923 & 0{,}383 & & & & \\ & & -0{,}383 & 0{,}923 & & & & \\ & & & & 0{,}907 & -0{,}075 & 0{,}375 & 0{,}180 \\ & & 0 & & 0{,}214 & 0{,}768 & -0{,}513 & 0{,}318 \\ & & & & -0{,}318 & 0{,}513 & 0{,}768 & 0{,}214 \\ & & & & -0{,}180 & -0{,}375 & -0{,}075 & 0{,}907 \end{bmatrix}$$

There is another approach, where the matrix elements are integers:

$$C=\frac{1}{13}\begin{bmatrix} 13 & & & & & & & \\ & 13 & & & & 0 & & \\ & & 12 & 15 & & & & \\ & & -5 & 12 & & & & \\ & & & & 12 & 0 & 4 & 3 \\ & & 0 & & 0 & 12 & -3 & 4 \\ & & & & -4 & 3 & 12 & 0 \\ & & & & -3 & -4 & 0 & 13 \end{bmatrix}$$

In this case an integer arithmetic is sufficient and the PROM size is smaller. The same accuracy is achievable by using fewer bit numbers.

### *The simultaneous use of Hadamard and Slant matrices*

We can accomplish the orthogonal transform of video signals also by using Hadamard and Slant matrices simultaneously. In this case forming the elements of Slant matrices differing from $\pm 1$ is possible by using adders only ([5]), thus this process contains exclusively additions and is suitable for real-time coding.

## WHT with parallel processing

With the simultaneous use of several WHT transform units — described in the previous section — a simultaneous transform of a given image and/or image part is possible. Let us assume the $N \times N$ image array $P$ in Fig. 8.a subdivided into four subarrays, each of size $N/2 \times N/2$. The matrix $H_N/2$ can be used in each of the four subarrays, independently from each other and then the following transform steps are received:

$$
\begin{array}{llll}
H_{N/2} \cdot P_0 = A_0 & E_0 = A_0 + A_1 & E_0 H_{N/2} = X_0 & \mathscr{F}(0) = X_0 + X_1 \\
H_{N/2} \cdot P_1 = A_1 & E_1 = A_1 - A_3 & E_1 H_{N/2} = X_1 & \mathscr{F}(1) = X_0 - X_1 \\
H_{N/2} \cdot P_2 = A_2 & E_2 = A_0 - A_2 & E_2 H_{N/2} = X_2 & \mathscr{F}(2) = X_2 - X_3 \\
H_{N/2} \cdot P_3 = A_3 & E_3 = A_1 + A_3 & E_3 H_{N/2} - X_3 & \mathscr{F}(3) = X_2 + X_3
\end{array}
$$

In compliance with these steps a coder can be formed with the block diagram shown in Fig. 8.b. and a flow chart as seen in Fig. 9. The input data are ordered and stored memories $P_0 \ldots P_3$. From $P_0 \ldots P_3$ the data arrive into the four, identical form processors. The post-processor puts the position-bits into the transformed data.

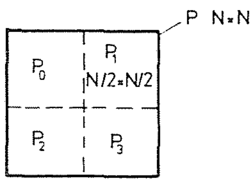


*Fig. 8.a*

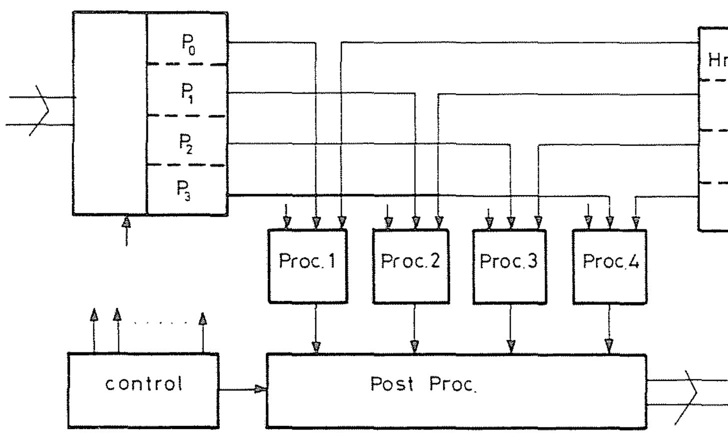


*Fig. 8.b*

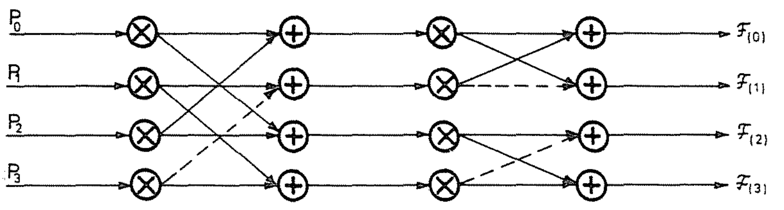


*Fig. 9*

The procedure can be extended by dividing the array $P$ into $4^k$ parts, with Hadamard matrix $(H_{N/2}K)$ having size $\frac{N}{2^k} \times \frac{N}{2^k}$. This procedure is suitable to transform simultaneously larger size image sections.

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