COMPUTER-AIDED DESIGN OF MOS/LSI CIRCUITS: DEVICE AND FUNCTIONAL MODELS

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1. Introduction

Nowadays, by the spreading of LSI circuits and microprocessors, special attention is paid also in this country to the methods of designing and producing MOS/LSI circuits. The computer-aided simulation of MOS circuits is one of the most important design methods. For this circuit simulation a circuit analysis program is needed with satisfactorily accurate built-in models of the required semiconductor devices — in this case, of the MOS transistors. Simulation of more complicated circuits, exceeding the efficiency of the usual circuit analysis programs, is only possible by substituting some well-known, related parts of the original circuit by functional macromodels.

In this paper a MOS transistor model is presented, taking also the second-order effects into consideration and then a functional model of the MOS R—S flip-flop, equivalent in describing its transistors to the MOS model but having more simple circuitry is shown. In order to demonstrate the application of the models, transient analysis results of more complicated MOS/LSI circuits are given. The models were integrated into the TRANZ-TRAN nonlinear circuit analysis program which was developed at the Department of Electron Devices some ten years ago and has been used in many computer centres in this country [1, 2]. The circuit analysis treated in this paper was executed by the TRANZ-TRAN variant adapted to the ICT 1905 computer of the Central Research Institute for Physics [3].

2. Short survey of the literature

The practical realization of MOS devices and the explanation of their functioning is especially the merit of HEIMAN and HOFSTEIN [4]. Solution of the basic physical equations in order to get the device characteristics was done first of all by IHANTOLA and MOLL [5] and by SAH [6]. Lot of papers

have been discussing the modelling problems of the MOS devices from the sixties till now. The works by MEYER [7], MERCKEL et al. [8] and JENKINS et al. [9] should be mentioned, the latter giving a good survey of the whole subject up to 1973. Later the models were made more exact [10—14]. A MOS-oriented circuit analysis program was also pub- lished [15] and some experiments on simple functional models reported [16—17]. In this country, the pioneering work by Tarnay and his group should be mentioned [18—23], looking back to more than ten years.

3. The TRANZ-TRAN MOS transistor model and its application

The TRANZ-TRAN circuit analysis program has had a built-in MOS transistor model from the beginning [1,2]. However, the model discussed here makes possible an exacter simulation. This model is valid first of all for enhancement-type MOS transistors, although — with other starting formulae and boundary conditions — a formally hardly different model can be applied for depletion-type MOS transistors, too.

Let us look at the MOS structure shown in Fig. 1.

For the charge-carriers moving in the channel the transport equation is valid, written in one dimension as:

$$J_n = -q\mu_n \cdot n \left(\frac{\partial U}{\partial x} - \frac{U_T}{n} \frac{\partial n}{\partial x} \right). \tag{1}$$

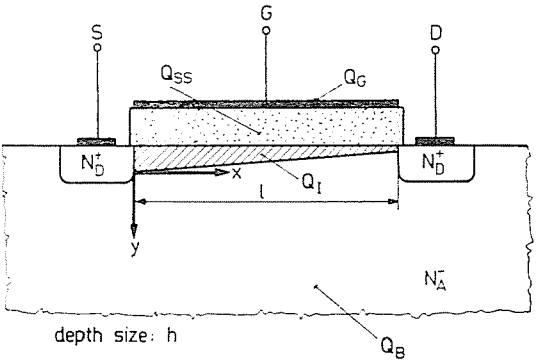

Fig 1. Section of the MOS transistor

Considering the high value of the electric field-strength, the diffusion member can be neglected and introducing the effective mobility [24] the differential equation of the MOS structure can be written as follows:

$$I_D = -q \cdot h \cdot \mu_{eff} \cdot Q_I \cdot \frac{dU}{dx} \tag{2}$$

where, because of charge equilibrium:

$$Q_I = -(Q_G + Q_{SS} + Q_B) \tag{3}$$

Introducing the specific gate capacitance, referred to the unity of surface and expressing the charges of the substrate in terms of the voltage across the depletion layer [25] the solution of (2) for the triode region of the MOS transistors, after some minor transformations can be given in the form:

$$I_D = F(U_{GS}) - F(U_{GD}) \tag{4}$$

where

$$F(U) = \begin{cases} I_0 \cdot (U - V_T^*)^2, & \text{when} \quad U > V_T^* \\ 0, & \text{when} \quad U \leq V_T^* \end{cases} \tag{5}$$

and

$$V_T^* = V_{T_0} + V_{TK} \cdot \frac{W_F}{U_{GS} - U_{GD}} \left[\left(\frac{U_{DB}}{2W_F} + 1 \right)^{3/2} - \left(\frac{U_{SB}}{2W_F} + 1 \right)^{3/2} \right] \tag{6}$$

The applied constants are:

$$V_{T_0} = 2W_F - U_K - \frac{Q_{SS}}{C_0} \tag{7}$$

(the ideal threshold voltage), and

$$V_{TK} = \frac{8}{3} \frac{\sqrt{q \cdot \varepsilon_H \cdot N_A^- \cdot |W_F|}}{C_0} \tag{8}$$

where

W_F is the doping-dependent Fermi-level of the semiconductor,
U_K the contact potential,
q the electron charge,
Q_{SS} the charge represented by the surface states,
ε_H the dielectric constant of the semiconductor,
N_A^- the doping concentration in the substrate,
C_0 the specific capacitance of the gate, referred to the unity of surface.

The boundary of the saturated region can be determined starting from the condition

$$\left. \frac{\partial I_D}{\partial U_{DS}} \right|_{U_{DS} = U_{DS\max}} \tag{9}$$

yielding the quadratic equation:

$$U_{DS\max}^2 - \left[2(U_{GS} - V_{T_0}) - \frac{9}{32} \frac{V_{TK}^2}{W_F} \right] \cdot U_{DS\max} +$$

$$+ (U_{GS} - V_{T_0})^2 - \frac{9}{16} \cdot V_{TK} \cdot \left(\frac{U_{SB}}{2W_F} + 1 \right) = 0. \tag{10}$$

Based on practical experiences with digital circuits, in this model the output conductance of the MOS transistors in the saturated region is considered to be zero as a first approximation by substituting in Eqs (4)—(6)

$$U_{DB} = U_{SB} + U_{DS\,\max} \tag{11}$$

and

$$U_{GD} = U_{GS} - U_{DS\,\max} \tag{12}$$

for $U_{DS} > U_{DS\,\max}$.

Eqs (4)—(12) furnished an expression for the channel current of the device, taking the known effect of the charges stored in the substrate upon the characteristics equations into consideration [26], by an apt modification of the threshold voltage.

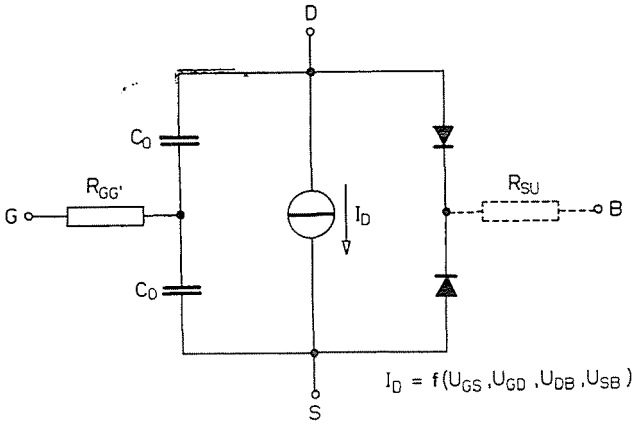

Fig. 2. TRANZ-TRAN MOS transistor model

This MOS transistor model [27], shown in Fig. 2. contains — besides the current generator representing the channel current, — also the gate resistance and gate capacitances (considered as constants) as well as the substrate source and substrate drain diodes (and their voltage-dependent capacitances). In the normal functioning of the MOS devices, these diodes are biased in reverse direction. Thus the model takes the breakdown phenomena of the substrate diodes into account, but neglects the gate channel and source drain breakdown. The model may also contain a series resistance towards the substrate. Not considering this latter resistance R_{SU}, the application of this model means one plus node and six plus branches for each MOS transistor in the circuit analysis program. The model assures a perfect drain source symmetry. The source current of its main current generator depends upon four symmetric input voltages U_{GS}, U_{GD}, U_{SB} and U_{DB}.

Expressions for the temperature dependence are:

$$I_0(T) = I_0(T_0) \cdot [1 + \alpha_I(T - T_0)] \tag{13}$$

$$V_T^*(T) = V_T^*(T_0) \cdot [1 + \alpha_U(T - T_0)] \tag{14}$$

In order to apply the model — besides certain data of the MOS transistor — it is necessary to indicate the parameters of the parasitic diodes (these, however, correspond to the data necessary for the simple *p-n* diode model in the TRANZ-TRAN program). The parameters necessary for the MOS transistor model are shown in Fig. 3. As an example for the application of the model the transient

R_S	I_S	$m \cdot U_T$	I_Z	U_L	n	data of parasitic diodes
τ	C_T	R_{th}	C_{th}	T_{max}	U_g	
W_F	V_{TK}	-	C_0	-	$m \cdot U_T$	
I_0	α_I	V_{T_0}	α_U	R_{SU}	1.0	
1.0	$R_{GG'}$	U_g	-	-	0.0	

Fig. 3. Catalogue data of the TRANZ-TRAN MOS transistor model

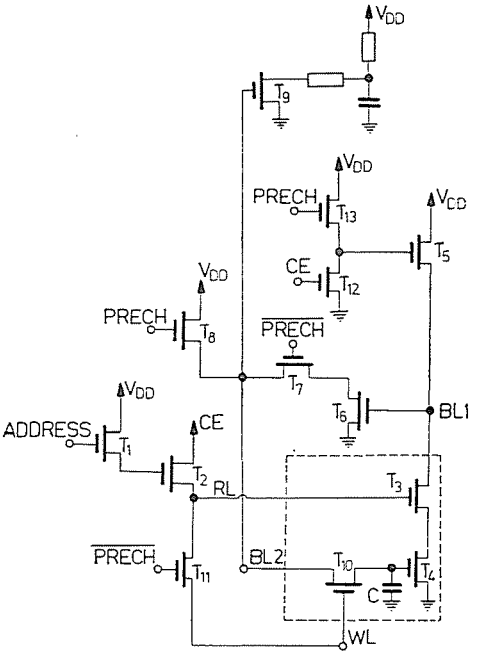

Fig. 4. Simplified SIGNETICS 1103 MOS RAM

analysis results of the SIGNETICS 1103 Silicon-gate MOS/LSI RAM are shown. The elementary storage cell is seen in Fig. 4, complete with the common circuit details [28].

In the analysis of the circuit containing 13 MOS transistors, the parasitic capacitances of the different lines (WL, RL, etc.) were taken into consideration in terms of constant capacitors in the circuit, omitted in Fig. 4, for the sake of simplicity. The transient analysis of this circuit containing 84 branches and 30 nodes in one transient moment took about 30 seconds on the ICT 1905 computer of the Central Research Institute for Physics. In order to illustrate the results, the ADDRESS, CHIP ENABLE and PRECHARGE control signals are shown in Fig. 5 and so are the time dependence of the voltage across the storage capacitance in the logical "0" and "1" state of the cell. The proper functioning of the rewriting process of the storage cell can be checked on the basis of Fig. 5.

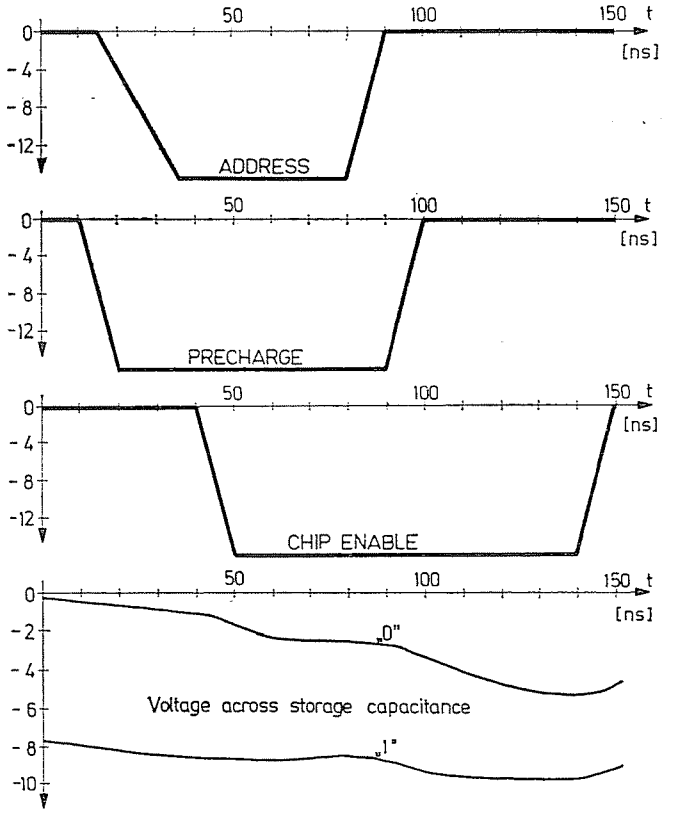

Fig. 5. Transient wave forms of the SIGNETICS 1103 MOS RAM (calculated by the TRANZ-TRAN program)

4. TRANZ-TRAN MOS R-S flip-flop functional model and its application

Let us look at the R-S flip-flop shown in Fig. 6.

The DC. functioning of the circuit can be followed in Fig. 7. This transfer characteristics surface was computed by the TRANZ-TRAN analysis program substituting every transistor by the model discussed earlier.

Often, however, the functioning of the designed matching circuits is more interesting than the flip-flop itself. Evidently, in this case it is better to construct a circuit diagram — a functional model — reflecting the inner functioning at just logical levels, but simpler than to describe the flip-flop at a great expenditure of computer time and storage capacity.

Let us look at Fig. 8, showing the simplified R-S flip-flop circuit, where the MOS transistors serving only as loads have been substituted by constant

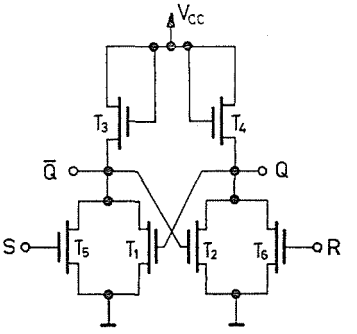

Fig. 6. MOS R-S flip-flop

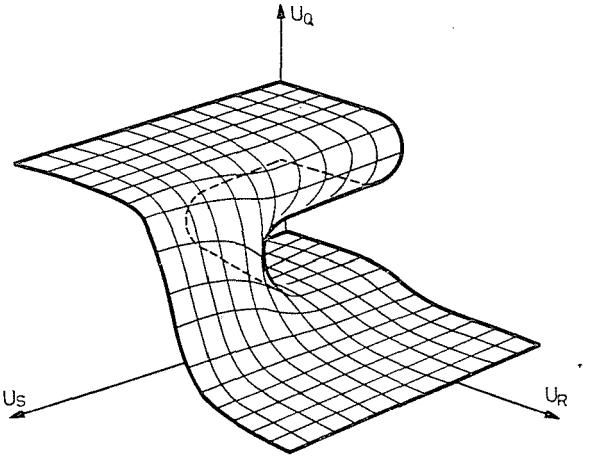

Fig. 7. DC. transfer surface of the MOS R-S flip-flop

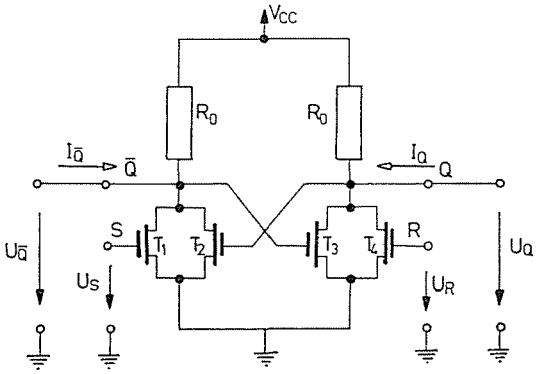

Fig. 8. Simplified MOS R-S flip-flop

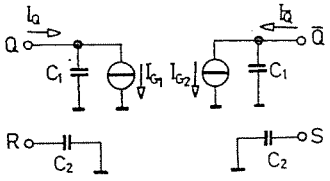

Fig. 9. MOS R-S flip-flop functional model

valued resistors. This circuit has two inputs U_R and U_S as well as two outputs U_Q and $U_{\bar{Q}}$. The output currents I_Q and $I_{\bar{Q}}$ are seen to depend upon only three input voltages besides the supply voltage, to be considered as constant. Accordingly the substituting circuit diagram of the R-S circuit is easy to draw (Fig. 9).

The basic equations of the model are (15) and (16) referring to the two current generators, to be completed by the current equations of the capacitances describing the transient behaviour [29].

$$I_{G_1} = f(U_R, U_{\bar{Q}}, U_Q) \tag{15}$$

$$I_{G_2} = f(U_S, U_Q, U_{\bar{Q}}) \tag{16}$$

$$I_Q = I_{G_1} + C_2 \cdot \frac{dU_Q}{dt} \tag{17}$$

$$I_{\bar{Q}} = I_{G_2} + C_2 \cdot \frac{dU_{\bar{Q}}}{dt} \tag{18}$$

$$I_R = C_1 \cdot \frac{dU_R}{dt} \tag{19}$$

$$I_S = C_1 \cdot \frac{dU_S}{dt} \tag{20}$$

This R-S functional model needs no excess node, only six excess branches (the original circuit involved six excess nodes and thirty-six excess branches). Derivation of the source currents of current generators and of the values of C_1, C_2 capacitances in Fig. 9 is shown in the following.

Symmetry of the circuit permits to analyze the half flip-flop alone shown in Fig. 10. It is a NOR-gate, and its transfer characteristic surface is seen in Fig. 11.

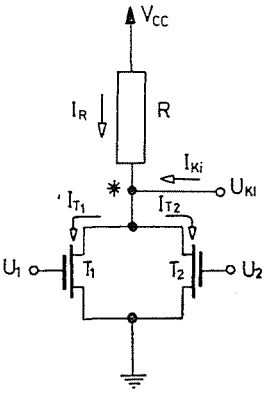

Fig. 10. Simplified MOS NOR-gate

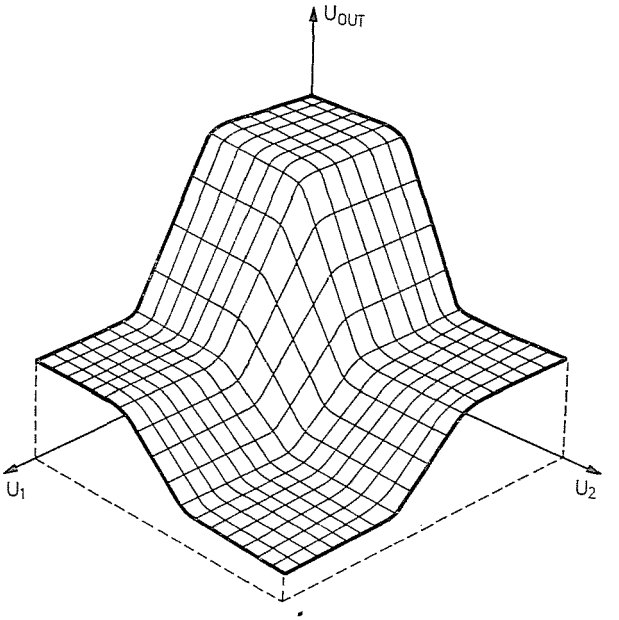

Fig. 11. DC. transfer surface of the MOS NOR-gate

The Kirchhoff equation for the node designated by * in Fig. 10:

$$I_{OUT} = I_{T_1} + I_{T_2} - I_R \tag{21}$$

gives the source current of the current generator $I_{Gl} = I_{ki}$. With the aid of Eqs (4)—(12) in the former item, the other currents in Eq. (21) can be written as follows:

$$I_{T_1} = F(U_1) - F(U_1 - U_{OUT}) \tag{22}$$

$$I_{T_2} = F(U_2) - F(U_2 - U_{OUT}) \tag{23}$$

$$I_R = G \cdot (V_{CC} - U_{OUT}). \tag{24}$$

By these equations the functions in Eqs (15) and (16) are given.

The capacitances C_1 and C_2 in Fig. 9 involve the capacitances between the inputs and the ground in the original circuit. Let us look at Fig. 12, where the capacitance network of the MOS transistors of the flip-flop is shown (on the basis of the model in Fig. 2). C_0 are gate capacitances, C_T are depletion layer capacitances of the substrate diodes (practically their maxima have to be taken into consideration), while the gate and substrate series resistances are neglected. To simplify the problem, however, it has been taken into account that the sources and substrates of all transistors are connected to the ground. Thus, the parasitic diodes of the source substrate junctions are shunted, and their space-charge capacitances have been meglected.

The resultant capacitances of the circuit at ① and at ② are C_2 and C_1. After some elementary transformations:

$$C_1 = C_0 + \frac{C_0 \cdot (2C_T + C_0 + C_K)}{2(C_0 + C_T) + C_K} \tag{25}$$

$$C_2 = 2C_T + \frac{3}{2} C_0 + C_K \tag{26}$$

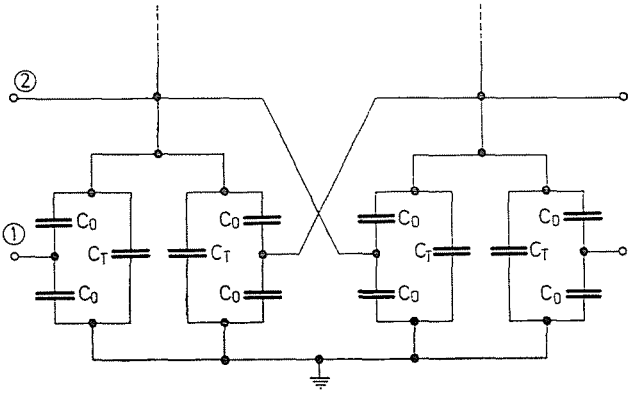

Fig. 12. Capacitance network of the MOS R-S flip-flop

where

$$C_K = \frac{2C_0\left(2C_T + \frac{3}{2}C_0\right)}{2C_T + \frac{7}{2}C_0} \tag{27}$$

The data necessary for the application of the model are summarized in Fig. 13.

The MOS R-S functional macromodel was tested on the ICT 1905 computer of the Central Research Institute for Physics by analyzing the transient

V_{CC}	G	C_1	C_2
V_{To}	V_{TK}	W_F	I_0

Fig. 13. Catalogue data of the MOS R-S functional model

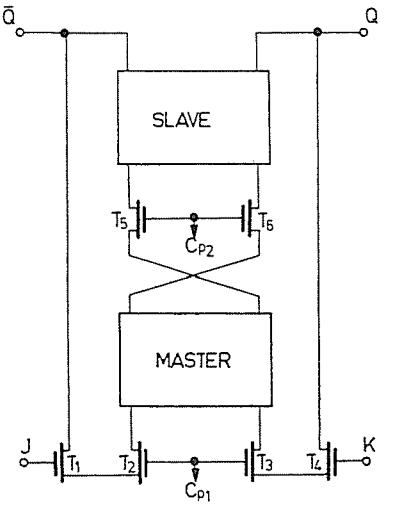

Fig. 14. Simplified MOS J-K master-slave flip-flop

behaviour of a J-K master-slave flip-flop. The circuit shown in Fig. 14 originally consisted of 29 nodes and 79 branches reduced to 14 and to 46 respectively, by applying the R-S functional model and the transient analysis of the whole circuit for one given transient moment was reduced in time to one-third, to about 12 sec. It should be noted that in the case of more complicated circuits an even better ratio can be reached. In final account, a reduction factor of about five in both time and storage capacity can be counted for.

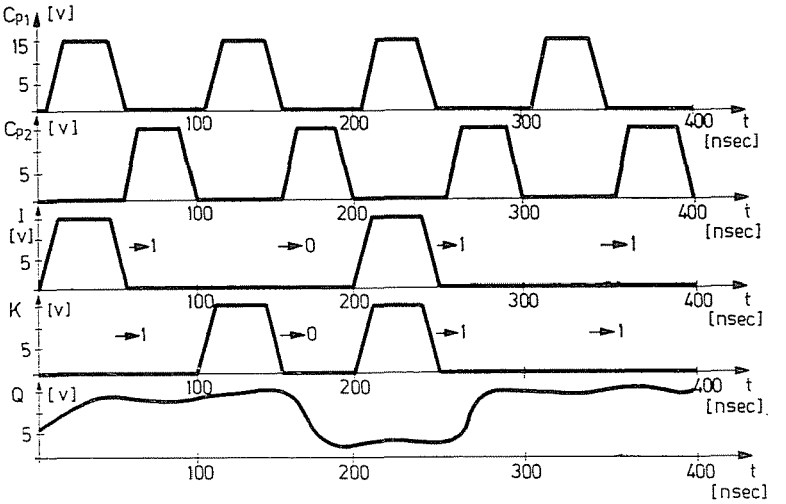

Fig. 15. Transient wave forms of the MOS J-K master-slave flip-flop

The transient analysis of four clock periods of the J-K master-slave flip-flop — computed by using the R-S macromodel — can be followed on Fig. 15, and the proper functioning of the circuit can be checked.

5. Possibilities for further development

a) *In the field of MOS transistor model*

The model can be extended to take second-order effects, such as field dependence of the mobility, variable values for the gate capacitances, channel-shortening, etc. into account. Among these the introduction of the channel shortening effect into the model in the range of saturation is under development.

b) *In the field of functional modelling*

The presented method yields a possibility to construct functional models of other MOS/LSI components.

Nevertheless, the solution of size problems in computer analysis of LSI circuits has to be attempted, beside applying functional macromodels, in developing circuit analysis programs suiting simultaneous analysis of circuits given partly by physical circuit description, partly by Boolean functions. Such an analysis involves to create interface between the physical and the logical parts of the circuits. The functional models — as intermediate steps — may be used in the solution of this problem.

Acknowledgements

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Summary

The computer-aided design of MOS/LSI circuits is very important for modern microprocessors. A MOS transistor model is introduced taking second-order effects into consideration, and an example is given for functional macromodeling. A MOS R-S flip-flop macromodel describing the inner functioning of the original flip-flop only at logical levels but equivalent to the original R-S circuit from the point of view of the outer circuit and having simpler circuitry than the original is presented. The models were integrated to the TRANZ-TRAN nonlinear circuit analysis program, and also some results of MOS/LSI circuit detail transient analyses are shown.

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