A NEW ALGORITHM FOR SIMULATING POWER SEMICONDUCTOR CIRCUITS

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Introduction

In the literature papers on analyzing and simulating power semiconductor circuits are often found. Most of these papers deal with individual circuits. In one part of them the presented programs contain the circuit equations corresponding to various conducting conditions of the semiconductors, and the program selects the proper equations for numerical integration from time to time. In a less frequent method the semiconductors are replaced by resistances (or inductances) of extremely high and low values.

There are general purpose programs for the mentioned task as well. As an example, MURAKAMI, KOSAKA and NISHIMURA [2] used a method where the non-conducting semiconductors were eliminated from the circuit, and the state equations were formed again at every mode change for numerical integration.

The program presented here is of general purpose, yet the simulation is based on a circuit of fixed configuration. The program using the concerned algorithm computes the voltages and currents as time functions of arbitrary electric circuits containing power semiconductor (diodes and thyristors). The semiconductors operate with line commutation. The program can well be used for computating the transients of power semiconductor circuits, as well as for determining the quasi stationary state of complicated power semiconductors circuits. The simulation can be started from the previously computed quasi stationary state, so the short transients can be computed, too. Essentially the simulation is numerical integration of the state equations of the circuit using fourth order *Runge-Kutta* algorithm. During the simulation, no solution of whatever nonlinear equations is necessary. The state equations of the circuit were formed by topological methods. In order to reduce the time of computation, two integrating step sizes can also be used, the smaller one near the mode changes. The program was written in ALGOL for the Soviet computer RAZDAN 3.

1. The essentials of the algorithm

The used semiconductor model is the following: in conducting condition its voltage is zero, but in nonconducting condition its current is zero. The holding current and the threshold voltage are zero, and the forward slope resistance can be set ($1 \div 10$ mΩ). In case of thyristors the recovery time is zero.

In addition to semiconductors the circuit to be simulated may contain uncontrolled (independent) voltage sources and current sources (constant and sinusoidal), and resistances, capacitances and self inductances of constant values. In first approximation the semiconductors are represented by uncontrolled voltage sources. The graph of the circuit is assumed to be connected. Besides the circuit is supposed to contain no excess elements [1], that is, in the circuit there are no loops composed only from voltage sources and capacitances, and there are no cutsets composed only from current sources and inductances. This assumption does not contradict to generality (see later), but has the significant advantage that the state equations are very simple [1].

The semiconductors are represented by voltage sources. This approach was introduced by K. P. KOVÁCS [4] and I. RÁCZ [5] in case of special circuits. Regarding the state equations these sources are uncontrolled, but regarding the operation of the program these are controlled—more precisely adjusted—sources. This adjustment means that the voltages of the voltage sources corresponding to conducting semiconductors are zero, but the voltages of the voltage sources corresponding to nonconducting semiconductors are set to cause zero current on the concerned voltage sources. This is the "method of adjusted voltage sources" [3]. So the computation of the voltages of the nonconducting semiconductors needs additional computation at every simulating point. The complexity of the simulation increases only with this computation in comparison with simulating linear circuits.

2. State variable representation of the circuit

The formulation of the state equations of circuits containing no excess elements is found in [1]. The definitions and results are enumerated because they will be used later. Superscript T denotes transposition. Every symbol denotes a vector, the matrices are denoted by thick letters.

The vectors of the branch voltages and branch currents can be divided into two parts according to the tree branches and links:

$$i=[i_1 \;\; I_2]^T$$
$$v=[V_1 \;\; v_2]^T \tag{1}$$

where subscripts 1 and 2 denote tree branches and links. The structures of these vectors are the following:

$$\begin{aligned} i_1&=[i_E\ i_C\ i_R]^T \\ I_2&=[I_G\ I_L\ J]^T \end{aligned} \qquad (2)$$

$$\begin{aligned} V_1&=[E\ V_C\ V_R]^T \\ v_2&=[v_G\ v_L\ v_J]^T \end{aligned}$$

where the letters E, C, R, G, L and J denote voltage sources, capacitances, tree resistances, link conductances, self inductances and current sources, respectively. The relationships between the tree branch and link variables are the following:

$$\begin{aligned} i_1&=-\mathbf{F}I_2 \\ v_2&=\mathbf{F}^T V_1 \end{aligned} \qquad (3)$$

where matrix $\mathbf{F}$ is the proper submatrix of the reduced incidence matrix corresponding to the fundamental cutsets. The state equations are:

$$\mathbf{M}z=\mathbf{A}x+\mathbf{B}u \qquad (4)$$

where

$$\begin{aligned} z&=[V_R\ I_G\ \mathrm{d}V_C/\mathrm{d}t\ \mathrm{d}I_L/\mathrm{d}t]^T \\ x&=[V_C\ I_L]^T \\ u&=[J\ E]^T. \end{aligned} \qquad (5)$$

Matrices $\mathbf{M}$, $\mathbf{A}$, and $\mathbf{B}$ can be formed on the basis of the values of the circuit elements and the matrix $\mathbf{F}$, see [1].

3. Derivation of the simulating equations

In our algorithm the state equations were modified as follows. Let us partition vectors E and i_E according to the actual (electromotive) and adjusted (corresponding to semiconductors) voltage sources.

$$\begin{aligned} E&=[E_e\ E_a]^T \\ i_E&=[i_{Ee}\ i_{Ea}]^T. \end{aligned} \qquad (6)$$

It is useful to relate vectors E_a and i_{Ea}. Using Eq. (4) we can write:

$$I_G=\mathbf{P}[V_C\ I_L\ J\ E_e\ E_a]^T \qquad (7)$$

where matrix $\mathbf{P}$ (and the new matrices found later) can be formed from matrices $\mathbf{F}$, $\mathbf{M}$, $\mathbf{A}$ and $\mathbf{B}$. Using Eqs (3) and (7):

$$i_{Ea}=\mathbf{Q}g+\mathbf{S}E_a \qquad (8)$$

where

$$g=[V_C\ I_L\ J\ E_e]^T. \qquad (9)$$

Let us partition vectors E_a and i_{Ea} according to the conducting and nonconducting semiconductors:

$$E_e=[E_{ac}\ E_{an}]^T$$
$$i_{Ea}=[i_{Eac}\ i_{Ean}]^T \tag{10}$$

where subscripts c and n denote conducting and nonconducting. Using Eq. (10), Eq. (8) can be written as follows:

$$\begin{bmatrix} i_{Eac} \\ i_{Ean} \end{bmatrix} = \begin{bmatrix} \mathbf{Q}_1 \\ \mathbf{Q}_2 \end{bmatrix} g + \begin{bmatrix} \mathbf{S}_{11} & \mathbf{S}_{12} \\ \mathbf{S}_{21} & \mathbf{S}_{22} \end{bmatrix} \begin{bmatrix} E_{ac} \\ E_{an} \end{bmatrix}. \tag{11}$$

Taking into consideration that:

$$i_{Ean}=0$$
$$E_{ac}=0 \tag{12}$$

the following results are reached:

$$E_{an}=-\mathbf{S}_{22}^{-1}\mathbf{Q}_2 g$$
$$i_{Eac}=\mathbf{Q}_1 g+\mathbf{S}_{12}E_{an}. \tag{13}$$

Eqs (13) gives the voltages of the nonconducting semiconductors and the currents of the conducting semiconductors. Nevertheless, vectors E_{an} and i_{Eac} can be computed according to Eq. (14) only if number and position of the link resistances of the circuit meet certain requirements. That is, in every cutset corresponding to an adjusted voltage source must be at least one link resistance which occurs in none of the other cutsets corresponding to other adjusted voltage sources. More precisely, this requirement must be fulfilled only for the adjusted voltage sources corresponding to nonconducting semiconductors. This is the "link resistance condition". The necessity of this condition results from physical considerations, but it can be proved, by examining —supposing a certain conducting condition—how matrix $\mathbf{S}_{22}$ can be formed from matrices **F**, **M**, **A** and **B**. It is noted that fulfilling the link resistance condition may need a slight supplement to the circuit.

According to Eqs (13), the logic of the simulation is the following:

— If during certain time period the conducting condition of the semiconductors does not change, then, at every simulating point of the concerned time period, E_{an} and i_{Eac} have to be computed using Eq (13) and this is followed by the computation of other variables to be displayed.

— If in certain moments the examination of the signs of E_{an} and i_{Eac}, as well as the firing conditions indicate change in the conducting condition of the semiconductors, then the matrices in Eqs (13) are to be computed again according to the new conducting condition, and this is followed by the computation of vectors E_{an} and i_{Eac} (but then these vectors correspond already to other semiconductors).

4. Notations

— The program can be extended to the case where the circuit contains excess elements, the state equations are found in [1]. In this case the state equations contain the derivatives of vectors E and J (because controlled sources do not exist). But these derivatives may cause trouble, because the derivative of E_a can be computed only at a delay and inaccurately. We concluded that it is not worth using this general method because the link resistance condition requires supplementing the circuit even in this case.

— The logic of a similar program can be stated also as follows: the semiconductors must be adjusted current sources. Namely the currents of the current sources corresponding to nonconducting semiconductors are zero, but the currents of the current sources corresponding to conducting semiconductors are set to cause zero voltages across the concerned current sources. It is seen that in this case the "tree branch resistance condition" must be fulfilled. This requires just the same supplementing of the circuit to be simulated, as the "adjusted voltage source logic", thus this shortcoming cannot be avoided even by using the new logic. So far no program has been prepared using this logic, but it is likely that this program would run more quickly. Namely using the "adjusted voltage source logic" the order of the matrix to be inverted at mode changes is equal to the number of the nonconducting semiconductors, but using the "adjusted current source logic" the order of the matrix to be inverted is equal to the number of the conducting semiconductors. In a circuit, however, there are more nonconducting than conducting semiconductors on the average. The two logics can be combined but it does not seem to be particularly advantageous.

— The program can be extended in several directions. A possible extension is computing short circuit transients, so the selective operation of the protecting elements can be controlled. Another extension is examining the effects of the parameters of the protecting RC elements on the course of the reverse voltages of the semiconductors. A perspective extension is the computation of the transients of power electronic systems and testing the proper setting of the regulators.

5. Examples

5.1. The simulated circuit is a three-phase diode bridge connection feeding resistance load with condensator filtering (see Fig. 1). The simulation was performed using five different ratios Z_s/R_l, while the value of Z_s was fixed. The value of the filtering capacitance C_l was chosen so that $R_lC_l=12$ msec. The forward slope resistance of the diodes were represented by the resistances R_{sd}. The resistances R_{ps} and R_∞ were placed in the circuit for the circuit not to contain excess elements and the link resistance condition to be fulfilled. The resistance R_i was placed merely in order to display the resulting load current. The graph of the circuit is seen in Fig 2,

$\hat{U}$ = 10 V
L_S = 10^{-3} H
R_{ps} = 10 Ω
R_S = 0,314 Ω
R_{sd} = 10^{-3} Ω
R_∞ = 10^4 Ω
R_i = 10^{-3} Ω
R_l = 2,21 ÷ 44,2 Ω
C_l = (0,27 ÷ 5,4)10^{-3} F
f = 50 Hz
(Z_S = 0,442 Ω)

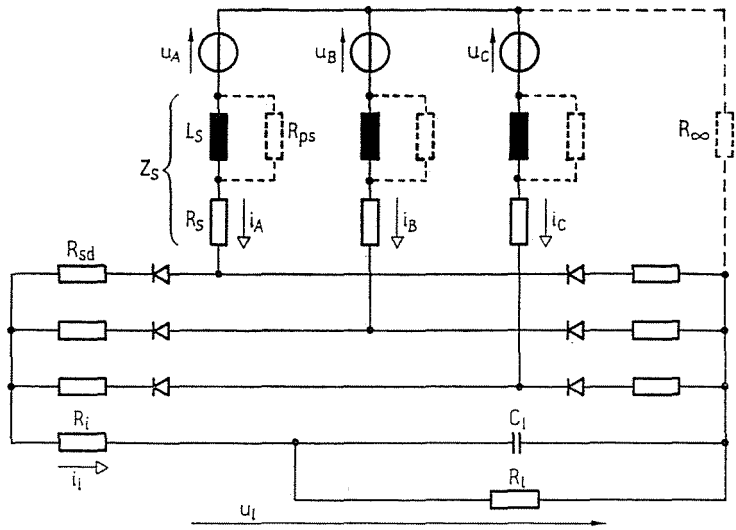

Fig. 1

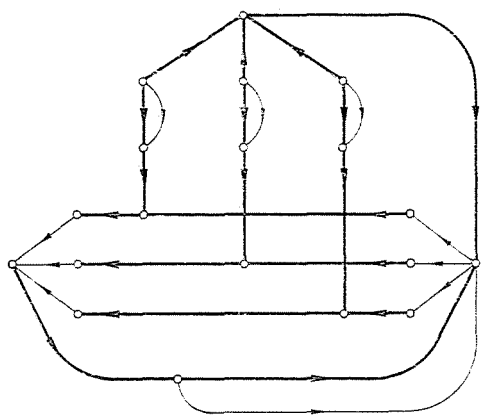

Fig. 2

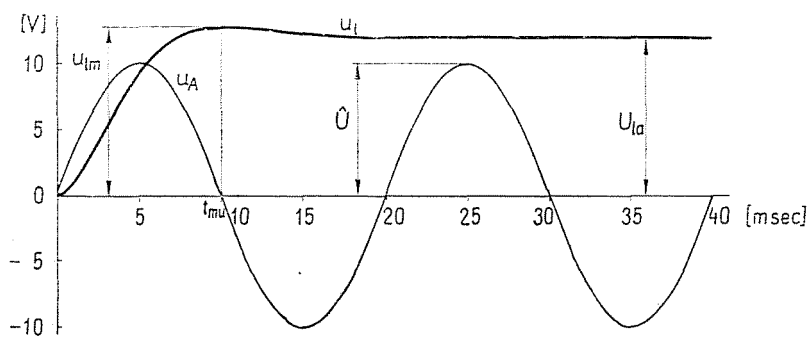

Fig. 3

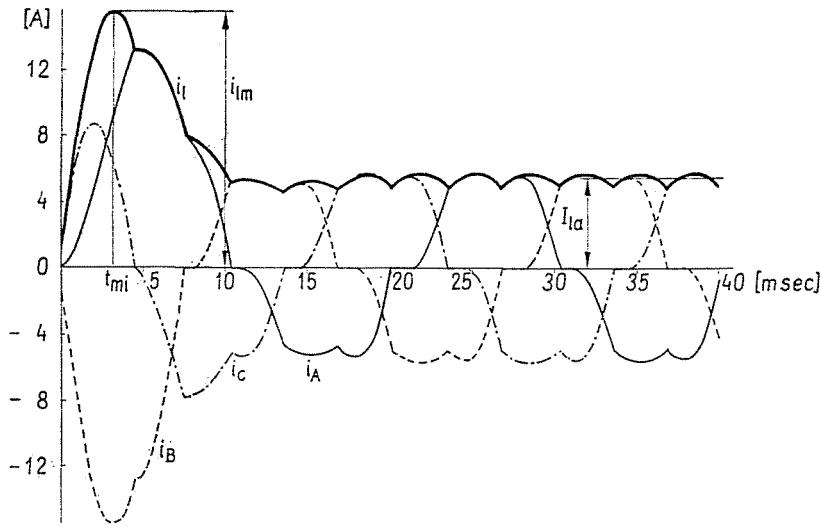

Fig. 4

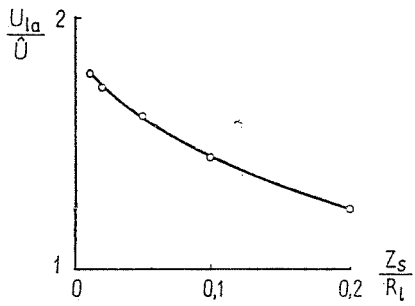

Fig. 5

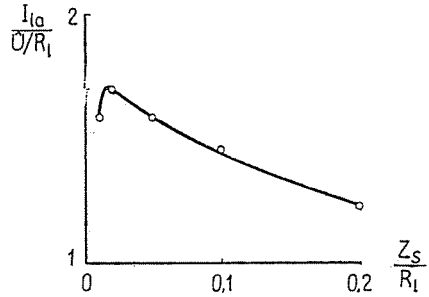

Fig. 6

where the heavy lines represent tree branches and the thin lines links. Figs 3 and 4 show the simulated waveforms for the ratio $Z_s/R_l=0.2$. Switching on the circuit has taken place at the positive zero-crossing of the voltage $u_A=U\sin\omega t$. In Figs 3 and 4 the maximum load voltage u_{lm}, the moment t_{mu} of this maximum, the maximum load current i_{lm}, the moment t_{mi} of this maximum, the average load voltage U_{la} and the average load current I_{la} are denoted.

Figs 5 to 9 show the relative values of the mentioned quantities versus Z_s/R_l. In case of $Z_s/R_l<0.02$ the load current has shown discontinuous conduction, otherwise continuous conduction.

The integrating step size was chosen as 10^{-4} sec. Regarding e.g. the ratio L_s/R_{ps} it is seen that the numerical instability is avoided. The choice of the value of R_∞ was found not to influence the stability of the integration, the value 10^4 may be useful.

5.2. Second, an example of testing will be shown, where the course of the variables is known. The simulated circuit is a three-phase bridge inverter and the

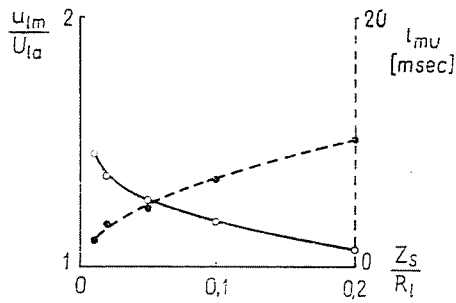

Fig. 7

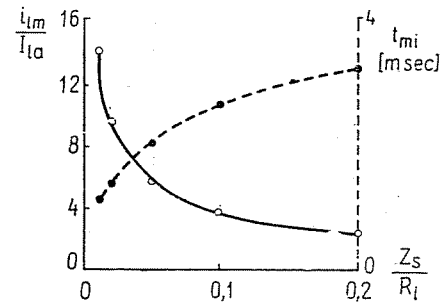

Fig. 8

U = 188,5 V
L_S = $34 \cdot 10^{-6}$ H
R_{ps} = 0,5 Ω
R_{St} = 10^{-3} Ω
R_{∞} = 10^{3} Ω
R_d = 0,1 Ω
U_b = 255 V
L_f = 10^{4}
R_{fp} = 10^{6} Ω
α = 150°
f = 50 Hz

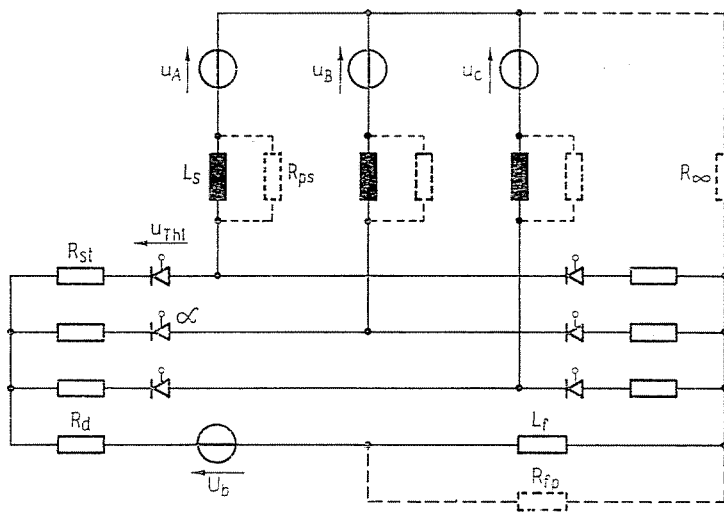

Fig. 9

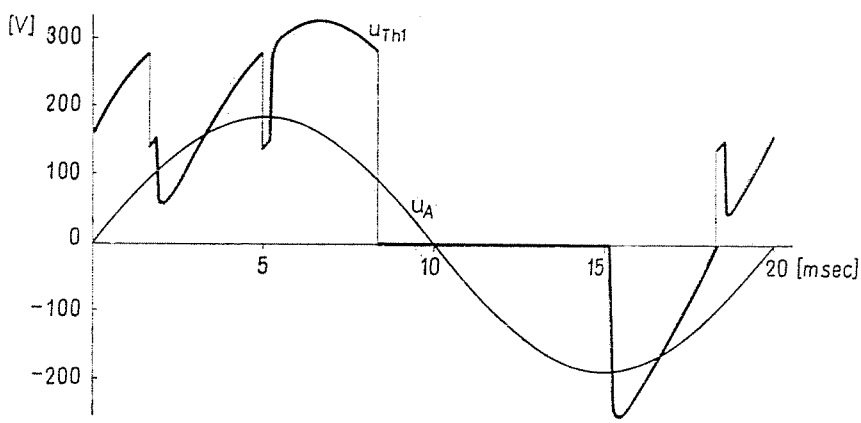

Fig. 10

course of the voltage across one of the thyristors is of interest in quasi-stationary state. The load inductance was chosen of a very great value for ensuring constant load current. In quasi-stationary state the load current can be computed theoretically, the initial currents of the inductors were set according to this value. The circuit is seen in Fig. 9, and the course of the thyristor voltage in Fig. 10. The integrating step size was $5 \cdot 10^{-5}$ sec.

6. Conclusions

The program presented here does not need reconstructing the state equations of the circuit at every mode change, in contrast e.g. with the program presented in [2], though both programs are of general purpose. Reconstruction would require the inversion of a matrix, the order of which is equal to the number of the no-source branches in the graph. But in the program presented here, the matrices of Eqs (13) are to be formed at every mode change and additional computations are necessary at every simulating point. Forming Eqs (13) requires the inversion of a matrix the order of which is equal to the number of the nonconducting semiconductors (that is, at most equal to the number of the semiconductors). So the matrix to be inverted is smaller than in [2].

A slight shortcoming of the method is that the circuit must not contain excess elements and the link resistance condition is to be fulfilled. As the examples show, these conditions may require slightly supplementing the circuit, but in most cases the caused error is insignificant.

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Summary

The paper describes an algorithm for simulating power semiconductor circuits on digital computers. The program using the concerned algorithm is of general purpose, yet the simulation is executed on the basis of circuits of fixed configuration. Essentially the simulation is the numerical integration of the state equations of the circuit, with some additional computations at the simulating points. The program can well be used for simulating the transients of power semiconductor circuits.

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