SETTLING TIME OF OPERATIONAL AMPLIFIERS WITH FEEDFORWARD COMPENSATION

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1. Introduction

The settling time of a given output signal of any circuit is interpreted as the period elapsing from a stepwise change of the excitation of the circuit or of one of its parameters to the time when the output signal approaches the asymptotic steady state value (after the stepwise change) within a prescribed error band in a way, that further on it will not step out of the error band.

The settling time of operational amplifiers is always defined for closed loop systems. The settling time of the output voltage will be examined by applying a step input voltage to the inverting (Fig. 1a) or noninverting (Fig. 1b) amplifier designed with a frequency-independent feedback network. The manufacturers usually specify the settling time of the operational amplifier for the worst case, i.e. they assume an input voltage step producing maximum output voltage and an amplifier with unity gain.

The settling time is one of the most important dynamic parameters of low-pass networks used in programmable analog electronic circuits. The possibility of applying analog networks controlled by digital signals produced by means of fast electronic analog switches (such networks as programmable gain amplifiers, multiplexers, sample-hold networks, analog circuits of A/D and D/A converters, the operational circuits of hybrid-analog computers, etc.) greatly depends on the time required for the error of the output signal to decrease, after a stepwise change, below the prescribed static error limit, generally in the order of 0.01 . . . 0.1 per cent. The settling time of programmable analog circuits is determined first of all by the own settling time of the feedback operational amplifiers — mainly of the unity gain amplifiers used for stepping up the loading impedance. This fact is due mainly to the necessity of using operational amplifiers having very good d.c. properties in order to decrease the static error. It is, however, very difficult to ensure excellent d.c. and dynamic properties simultaneously at the design of operational amplifiers. The problem is well known and hard to solve.

One of the more or less efficient solutions of the problem is the application of feedforward. Fig. 2 shows the three basic types of the operational amplifiers

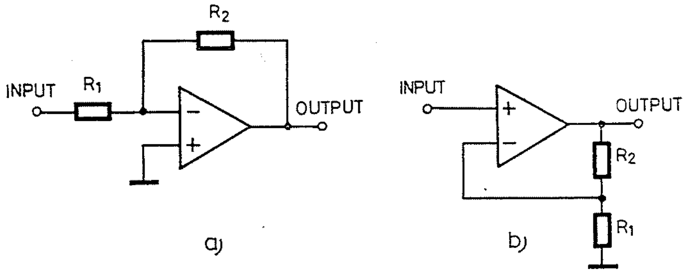

Fig. 1. Inverting (a) and noninverting (b) operational amplifiers

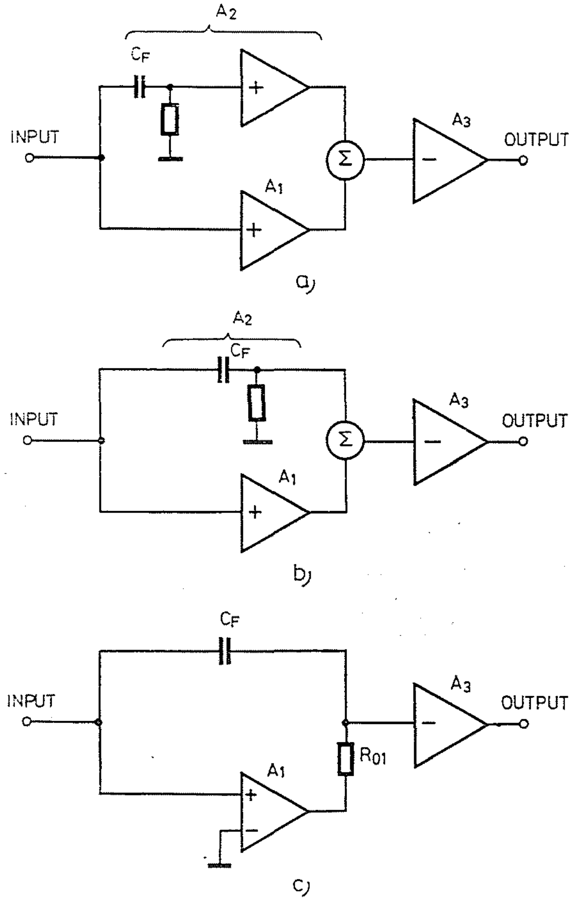

Fig. 2. Three main types of the application of feedforward with feedforward structure which can be applied only in the inverting amplifiers. In the operational amplifier with parallel channels (Fig. 2a), the first amplifier is a preamplifier with excellent d.c. but poor dynamic properties. On high frequencies the second amplifier assumes the role of the preamplifier. The gain of the second amplifier is lower, its d.c. error does not affect the d.c. properties of the whole amplifier, thus an amplifier with dynamically advantageous properties may be used. In this way the system unites the favourable d.c. properties of the first, and the favourable dynamic properties of the second amplifier. In Fig. 2b a simplified version of the circuit is seen where the role of the second amplifier is taken over by a passive high-pass network. Fig. 2c shows the feedforward compensation of the so-called second generation of the integrated operational amplifiers. This design differs from the solution according to Fig. 2b in that the signals of the first and second channel are not summed free of undesirable feedback.

The present paper aims at examining the problem of how much the settling time is affected by the feedforward undoubtedly advantageous from the point of view of other dynamic properties (e.g., rise time). In our study those of the factors determining the settling time will be considered that can be modified by feedforward. Thus certain phenomena, such as the effect of the thermal transient upon the settling time, or of the time constants of the feedback resistances, etc., will be disregarded. It will be assumed that the operational amplifier works in the linear domain during the settling time, i.e., no saturation occurs in any amplifier stage. The feedforward can be used also for eliminating the slew rate. This problem will be dealt with in a subsequent publication.

2. Relation between open-loop and closed-loop transfer functions and the settling time

The settling time of a linear low-pass two-port network can be computed if the relative error band h and the poles and zeros of the transfer function are known. The typical pole-zero configuration of the transfer function of feedback operational amplifiers is shown in Fig. 3. If the pole-zero configuration corresponds to Fig. 3, i.e., the root nearest to the origin is a pole (or a pair of complex conjugate poles) and no zero occurs in its immediate vicinity, the settling time is determined by the so-called dominant pole or pair of poles. If the dominant pair of poles is

$$p_{\mathrm{d}}^{*} = \sigma_{\mathrm{d}}^{*} + j\omega_{\mathrm{d}}^{*} \tag{1}$$

the settling time will be [1]

$$t_{\mathrm{s}} = \frac{\ln h}{\sigma_{\mathrm{d}}^{*}}, \tag{2}$$

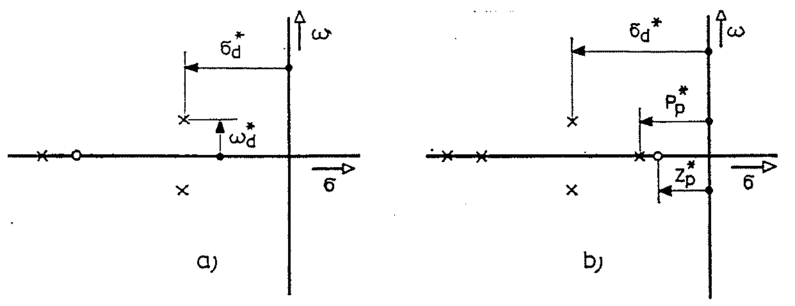

Fig. 3. A typical pole-zero configuration of the closed-loop transfer function of operational amplifiers

The inaccuracy of the approximation relationship is maximum, about 10 per cent, with double poles [1].

If the pole-zero configuration is of the type shown in Fig. 3b, i.e. when between the dominant pole (or pair of poles) and the origin there are a parasitic pole and a zero near to each other, then the settling time is greatly dependent on the place of the pole-zero pair and on the distance of pole and zero. It must be noted that this pole-zero configuration is generally produced by neutralizing the effect of the parasitic pole p_p with such a compensating network that, in principle, results in a zero z_p identical to the pole p_p (pole-neutralizing compensation); however, the two roots do not coincide, due to the component tolerance. As a consequence of incomplete pole neutralization, the pole-zero configuration of the open loop transfer function will be conform to Figs 4a or 4b, depending on the position of the parasitic zero and pole with respect to each other, and in the Bode plot of the loop gain a step will develop (Fig. 5). The place of the open loop pair of pole-zero can be characterized by the constant

$$a_1 = -\frac{p_p}{\omega_1} \tag{3}$$

and the extent of incomplete neutralization by the constant

$$a_2 = \frac{p_p - z_p}{z_p} \tag{4}$$

where ω_1 is the angular frequency belonging to unity loop gain, and z_p and p_p are the open-loop parasitic pair of pole-zero (the open-loop roots are considered to be real). Supposing a frequency-independent feedback and the inequalities

$$a_1 \ll 1 \quad \text{and} \tag{5}$$

$$a_2 \ll 1 \tag{6}$$

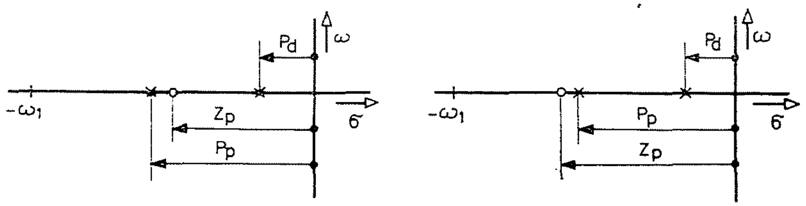

Fig. 4. Pole-zero configuration of the open-loop transfer function of operational amplifiers in the presence of a parasitic pole-zero pair

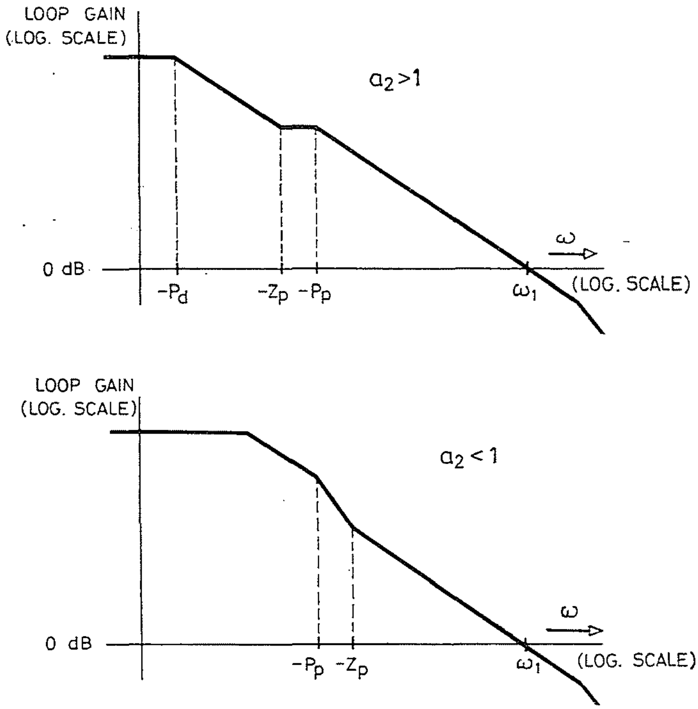

Fig. 5. Absolute value of the loop gain of operational amplifiers as a function of frequency, in the presence of a parasitic pole-zero pair

the relative distance of the closed loop pair of pole-zero with real roots will be [1]:

$$a_2^* = \frac{p_p^* - z_p^*}{z_p^*} = \frac{p_p^* - z_p}{z_p} = -\, a_1 \cdot a_2 \,. \tag{7}$$

If a step excitation is applied to the amplifier, an exponential signal component will appear which has a time constant determined by the closed-loop parasitic pole and a relative amplitude approximately identical with a_2. If the amplitude of this slowly changing component exceeds the prescribed error band h, the settling time may by orders of magnitude be longer than it is in the case of complete neutralization of the pole [1], [3].

It follows from all this that an incomplete neutralization of pole-zero does not affect the settling time if the condition

$$a_2^* < h$$

or

$$a_2 < \frac{h}{a_1} \tag{8}$$

i.e., the deviation of the open-loop pole and the zero is restricted. Though, due to the great component tolerance of operational amplifiers, the condition

$$a_2 \ll 1$$

is missed in most cases. Therefore the effect of the pole-zero pair to increase the settling time can be avoided with certainty in the case only when the condition

$$a_1 < h \tag{9}$$

is fulfilled, i.e., if no pole-zero pair is admitted in the domain between $h\omega_1$ and ω_1 [1].

If condition (8) is missed, the settling time will be determined by the parasitic pole p_p^* instead of the dominant closed loop pole p_d^*, and the settling time is given by the relationship

$$t_s = \frac{\ln \frac{h}{a_2^*}}{p_p^*} . \tag{10}$$

Depending on the value of a_1 the settling time computed this way may be by orders of magnitude longer than that of an otherwise identical amplifier containing no pole-zero pair (Eq. 2).

3. Settling time of operational amplifiers with feedforward structure

If the feedforward operational amplifier is applied in an inverting amplifier (Fig. 1), the open-loop amplitude response from

$$\omega = -p_d$$

to at least the frequency ω_1 must be designed to have a slope of -20 dB/D in order to achieve universal applicability. To this the dominant pole p_d must be produced in the 1st amplifier having unfavourable high-frequency characteristics. Let us suppose that the 2nd amplifier is of high-pass character (with a break frequency of $\omega = -p_F$). Then at the frequency where the gain of the 2nd amplifier becomes dominant instead of the 1st amplifier, a break frequency (pole p_d) has to be produced in the 3rd amplifier. The Bode plot of the loop gain will have a slope of -20dB/D, if the following conditions are fulfilled (see Appendix, App. 1):

$$p_F = p_d, \quad \text{and} \tag{11}$$

$$p_p = p_d \frac{A_{10}}{A_{20}} \tag{12}$$

where A_{10} is the d.c. gain of the 1st amplifier, and A_{20} the gain of the 2nd amplifier on high frequency.

If conditions (11) and (12) are fulfilled only approximately, there will be two pole-zero pairs both in the open-loop and in the closed-loop transfer function. The deviation from Eq. (11) results in a step of the amplitude response in the frequency region of

$$\omega = -p_d \approx L_0 \cdot \omega_1 \tag{13}$$

(L_0 is the d.c. loop gain).

Since, to ensure static accuracy,

$$L_0 > \frac{1}{h}, \tag{14}$$

the pole-zero pair does not increase the settling time (i.e., condition (9) is fulfilled).

A deviation from condition (12) causes a step in the Bode plot of the loop gain in the region of the frequency

$$\omega = -p_d \frac{A_{10}}{A_{20}} \approx \frac{1}{\beta_0 A_{20} A_{30}}. \tag{15}$$

Here β_0 is the frequency-independent feedback factor, and A_{30} the d.c. gain of the 3rd amplifier. Thus the place of the pole-zero pair is

$$a_1 = \frac{1}{\beta_0 A_{20} A_{30}} \tag{16}$$

and for an inverting amplifier with unity gain:

$$a_{11} = \frac{2}{A_{20}A_{30}} \,. \tag{17}$$

while in a most unfavourable case, with 100 per cent feedback (e.g., in an integrator circuit):

$$a_{1\,\mathrm{min}} = \frac{1}{A_{20}A_{30}} \,. \tag{18}$$

Thus, in the case of inadequate design, the feedforward may lead — with the improvement of other dynamic properties (limiting frequency of 3dB, and rise time) — to a large-scale increase of the settling time.

From condition (9) it follows that the feedforward improves the settling time at any rate, if

$$\beta_0 A_{20} A_{30} > \frac{1}{h} \,. \tag{19}$$

If an operational amplifier is specified also for the settling time, the fulfilment of condition (19) must be regarded as a basic principle of the design. If condition (19) is missed, then a careful control of p_d, p_p and the ratio A_{10}/A_{20} have to ensure the fulfilment of the inequality

$$a_2 < \beta_0 A_{20} A_{30} h \tag{20}$$

corresponding to condition (8).

For two typical cases (amplifier A : $A_{10} = 10^3$, $A_{20} = 1$ and $A_{30} = 10^3$; amplifier B : $A_{10} = 10^3$, $A_{20} = 10$ and $A_{30} = 10^3$) the effect of the pole-zero pair upon the settling time was determined also by numerical analysis (Appendix, App. 3). The place of ω_1 (and by it also of p_p) was fixed and the effect of the deviation of the parameter p_d from the value prescribed in Eq. (12) examined.

Fig. 6 shows the interrelation of the relative distances a_2 and a_2^* of the open-loop and closed-loop parasitic pole-zero pair. In Fig. 7 the settling time defined for the error bands of 0.1 per cent and 0.01 per cent is plotted vs. a_2. The asymmetry of the diagram and the deviation of the results from the previous relationships arise from the fact that on the one hand, condition (5) is missed near the edge of the domain examined, and on the other hand, a change of a_2 involves also that of a_1 (during the examinations the frequency ω_1 was kept constant because of the so far neglected further time constants).

If conditions (11) and (12) are completely fulfilled, the pole-zero pair is similarly present, supposed that there is a further pole p_0 in the transfer

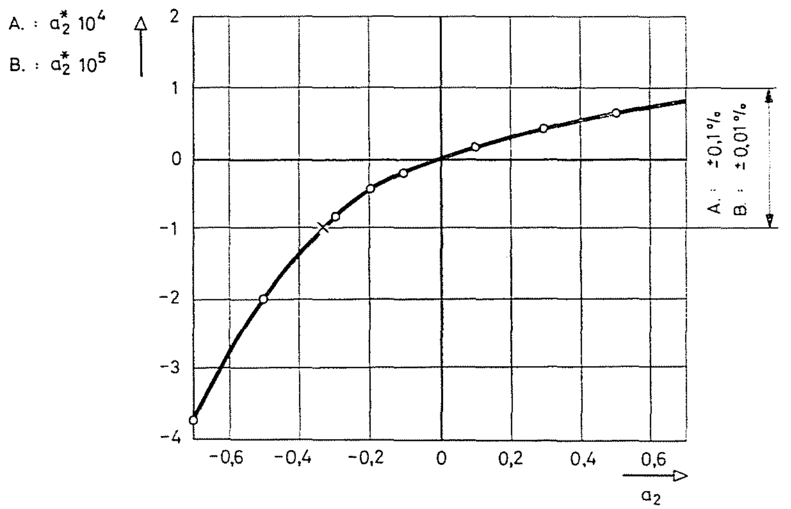

Fig. 6. Interrelation between the relative distances of the parasitic open-loop and closed-loop pole-zero pairs of feedforward operational amplifiers

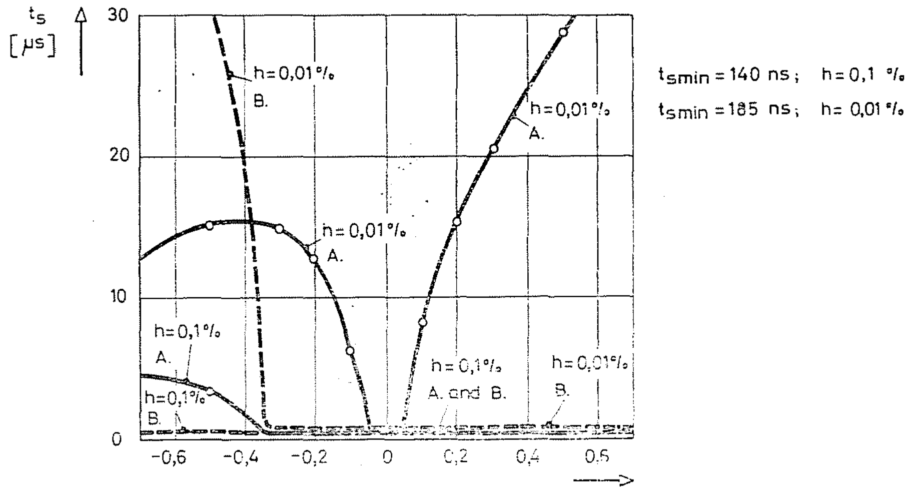

Fig. 7. Settling time of feedforward operational amplifiers as a function of the distance of the open-loop pole-zero pair

function of the 1st amplifier. This pole must, however, not be neglected, since the feedforward is applied just to eliminate its effect. If the feedforward branch is considered as independent of frequency, the open loop transfer function (Eq. App. 15) will have again two zeros (App. 17). If the break frequency produced by pole p_0 lies in the frequency range decisively determined by the feedforward branch — as it is desirable — i.e., if

$$l = \frac{p_d}{p_0} \ll k < 1 . \tag{21}$$

the two zeros will be

$$z_1 \simeq \frac{p_d}{l} \cdot \frac{k-l}{k} \tag{22}$$

$$z_2 \simeq \frac{p_d}{k} = p_p . \tag{23}$$

Provided that requirement (9) is fulfilled, the effect of the pole-zero pair produced by the fulfilment of equality (23) can be neglected. However, the pole-zero pair $p_0 - z_1$ will come about, for which condition (9) is not fulfilled. Following from (4) and (23),

$$a_2 \simeq \frac{l}{k} , \tag{24}$$

The relative distance of the closed-loop pole-zero pair decreases proportionally to the absolute value of the loop gain. On the frequency determined by the pole p_0 the loop gain is

$$|L|_{\omega=-p_0} \simeq l \cdot L_0 , \tag{25}$$

and thus

$$a_2 = \frac{1}{k \cdot L_0} = \frac{1}{\beta_0 A_{20} A_{30}} \tag{26}$$

i.e., the relative distance of the closed-loop pole-zero pair is constant for a given amplifier and independent also of A_{10} and p_0. Numerical computations have demonstrated that this statement is valid with a good approximation also in the range

$$l \leq k < 1 ,$$

which is milder than (21). From relationship (26) it follows that the high frequency parasitic pole of the 1st amplifier increases the settling time in the case only if condition (19) is fulfilled.

4. Feedforward compensation of the "second generation" integrated operational amplifiers

The operational amplifiers belonging to the "second generation" of the integrated operational amplifiers (their typical representatives are the operational amplifiers of type *741* and *748*) are not of feedforward structure. In the types having an external compensation network (e.g., in type *748*), however, one can apply feedforward compensation (Fig. 8), if they are used as inverting amplifiers. This way a larger band-width and a shorter rise time can be achieved (2).

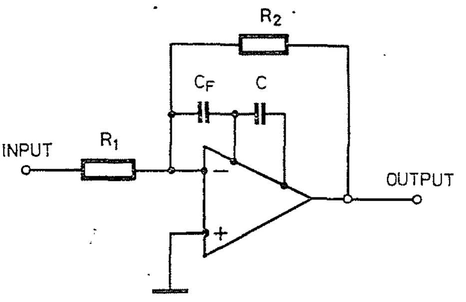

Fig. 8. Inverting amplifier with an integrated operational amplifier of feedforward compensation

From the results of chapter 3, it can be expected that this compensation will not reduce the settling time defined for the narrow error band, but considerably increase it instead, since in these types

$$A_{20} = 1$$

and

$$A_{30} < 10^3 .$$

Thus condition (19) will be missed in the case of an error band of 0.1 per cent or less.

The feedforward compensation of this type has a more complicate effect than has the type of Fig. 2a: here the summation of the output signals of the 1st and 2nd amplifiers involves an undesirable feedback (Fig. 2c). Feedforward capacitor C_F implies also considerable feedback, thus the zero and pole places of the transfer function depend also on the resistance of the generator.

Fig. 9 shows the simple linear model of the circuit illustrated in Fig. 8. The time constant $R_0 \cdot C_0$ simulates the pole of the input stage and, under consideration of the Miller effect, the capacitor C_d simulates the effect of the external capacitor C_c.

The numerator of the loop transfer function of the model is of second degree, its denominator of third degree (see Appendix, App. 2.). It can be demonstrated that the amplitude plot of -20 dBD cannot be achieved, i.e., it is impossible to make the two zeros coincide with the two poles. For this reason, also in the closed loop transfer function there will always be two pole-zero pairs in the region of the zero places identical with the open loop value also after feedback. The presence of these pole-zero places does not affect the settling time (which thus, due to feedforward, will be shorter than in the case without feedforward), if the relative distance a_2 between the closed loop pole and zero is smaller than the relative error band h. If this condition cannot be fulfilled, the settling time will increase in dependence on the place of the pole-zero pair.

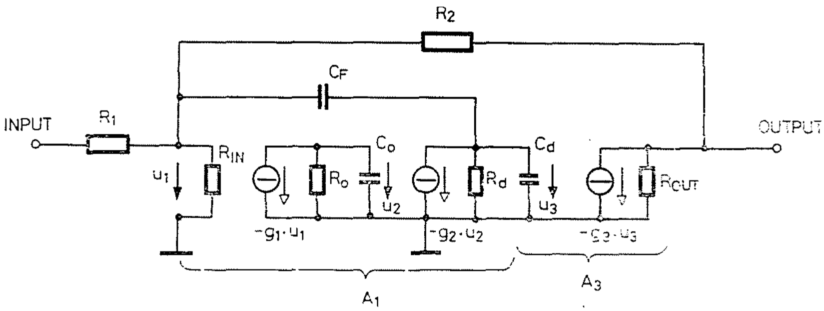

Fig. 9. Linear model of the circuit shown in Fig. 8

The high-frequency asymptote of the open-loop transfer function is

$$\frac{\omega_1}{s} \approx \frac{1}{s} \beta_0 A_0 \frac{a_2}{b_3} = \frac{1}{s} \cdot \frac{\beta_0 A_{20}}{R_g C_d} \tag{27}$$

and its place is bound by the time constants not considered here (input and load capacitances etc.). Consequently, the time constant $R_g \cdot C_d$ from the external parameters has to be chosen with a value certainly inhibiting oscillation. To minimize the settling time one can change the feedforward capacitance C_F and one of the elements $R_g C_d$. With the typical model parameters of the amplifier type *748* (App. 2) numerical analysis was carried out to determine the settling time and the closed-loop pole-zero configuration (Appendix, App. 3).

The results are summed up in Figs 10 to 15. The closed loop zeros depend practically on capacitor C_F alone (Fig. 10). With $C_F = 48$ pF a double zero occurs at $p_0/2$. At capacitances over this value the zeros are real, while one of the zeros is approaching the origin and the other the pole at p_0. For chosen value (8 kohm) of R_g the pole loci were plotted (Fig. 11). The closed loop pole-loci exhibit much similarity to the zero loci. The decisive feature is, of course,

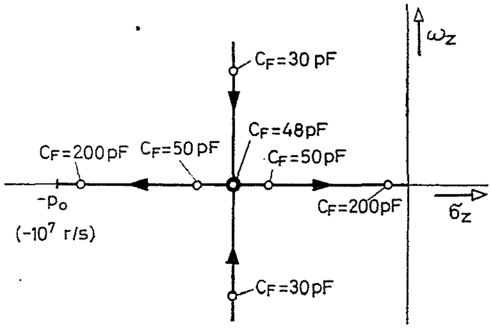

Fig. 10. Zero loci of the closed-loop transfer function of the amplifier type *748* with feed-forward compensation

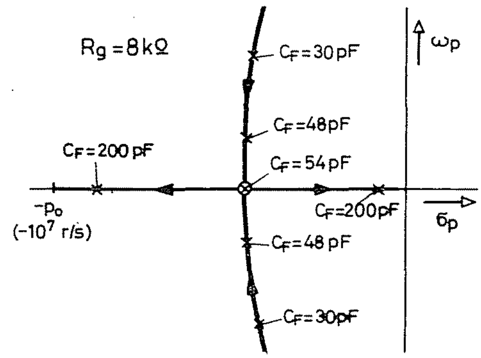

Fig. 11. Zero loci of the closed-loop transfer function of the amplifier type *748* with feed-forward compensation ($R_g = 8$ kohm)

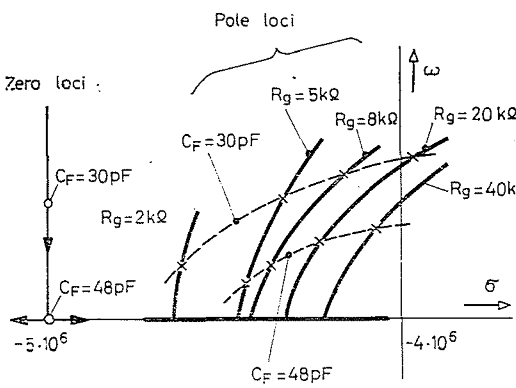

Fig. 12. Root loci of the closed-loop transfer function of the amplifier type *748* with feed-forward compensation. An enlarged detail

how much the zero and pole loci coincide, which cannot be evaluated from a comparison of Figs 10 and 11 because of the rough scaling. For this reason the positive imaginary branches of the complex conjugate pole and zero curves were plotted in a special enlarged diagram for several R_g values (Fig. 12).

It is clearly seen that although in this domain the complex conjugate pole-zero pair is relatively far from the origin and so the settling time is not increased by orders of magnitude, but no coincidence of the roots can be attained. Thus the settling time is determined by the pole-zero pair developing in the vicinity of $p_0/2$.

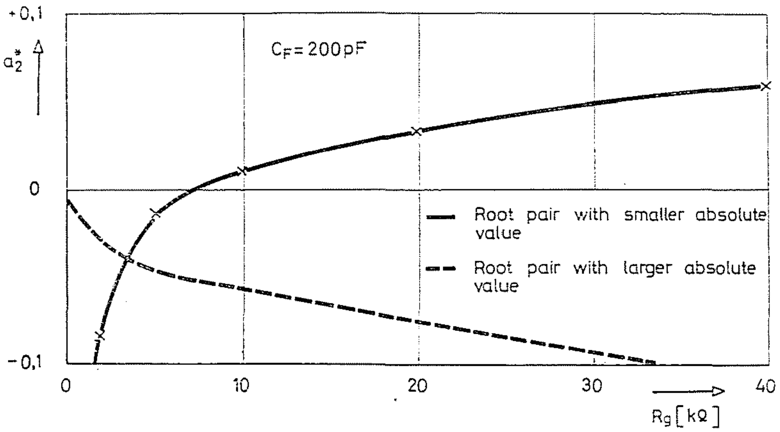

Fig. 13. Relative distances of two closed-loop pole-zero pairs of the amplifier type *748* with feedforward compensation, as a function of the generator resistance ($C_F = 200$ pF)

In Fig. 13 the relative distance a_2^* of the pole-zero pairs has been drawn with a value (200 pF) of C_F as a function of R_g in the domain of the real roots. The root pair of smaller absolute value plotted with continuous line is seen to coincide at about $R_g = 8$ kohm. At the same time, however, the deviation of the root pair of larger absolute value exceeds 1 per cent. Similar results were obtained from investigations into other values of C_F.

Nevertheless, it appears useful to examine the changes in the value of the settling time instead of any further analysis of the pole-zero configuration. The change of the settling time defined for the error band of 0.1 per cent has been plotted in Fig. 14 for various values of C_F, as a function of R_g. The figure shows that wherever the roots of smaller absolute values coincide, the settling time has a minimum. In these cases the settling time is determined by the pole-zero pair having a larger real part and lying nearer to p_0. When the relative distance of the pole-zero pair with lower absolute value exceeds the error band, the settling time is determined by the parasitic root pair, and thus it increases considerably. The minimum of the settling time slightly decreases with the increase of capacitance C_F. With small values of C_F producing a complex conjugate root pair, the value of the minimum is relatively large, but the curve of the settling time is considerably flattened.

Without feedforward, the frequency ω_1 of amplifier *748* must be chosen, because of p_0, lower than in the above example. To obtain the double closed-

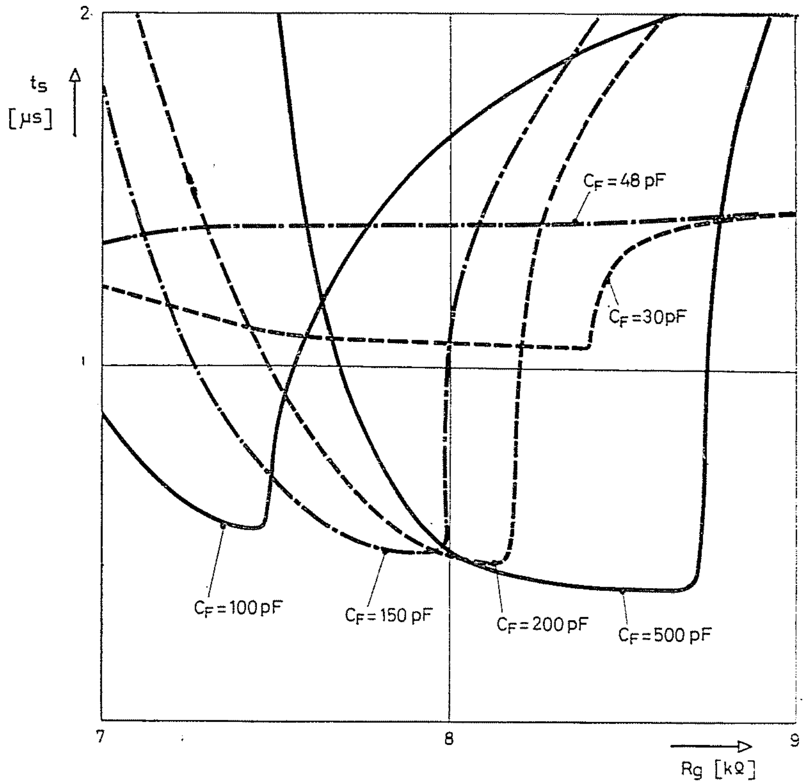

Fig. 14. Settling time of a unity gain inverting amplifier with the operational amplifier type *748* of feedforward compensation

loop dominant pole optimal from the viewpoint of the settling time [1]:

$$\omega_1 = p_0/4$$

and then:

$$p_d^* = p_0/2 \, ,$$

i.e., the settling time defined in our example for the error band of 0.1 per cent will be:

$$t_s = 1.38 \ \mu s \, .$$

A comparison of the results in Fig. 14 with the above values shows that the settling time can, in principle, be reduced to about its one third by the application of feedforward. This requires the adjustment of R_g to its optimum value. The optimum value of R_g and the minimum of the relevant settling time are shown in Fig. 15. It must be noted that the diagram was made with the data of a typical amplifier *748*. Namely the optimum value of R_g greatly depends on the parameters of the operational amplifier. It is also seen that a greater deviation of R_g from the optimum value may lead to a considerable increase of the settling time. Therefore a threefold reduction of the settling time can only be achieved by individual adjustment of each piece. If no individual adjustment is feasible, it is advisable to choose a small feedforward capacitance. This way, however, a slight improvement of the settling time can be expected.

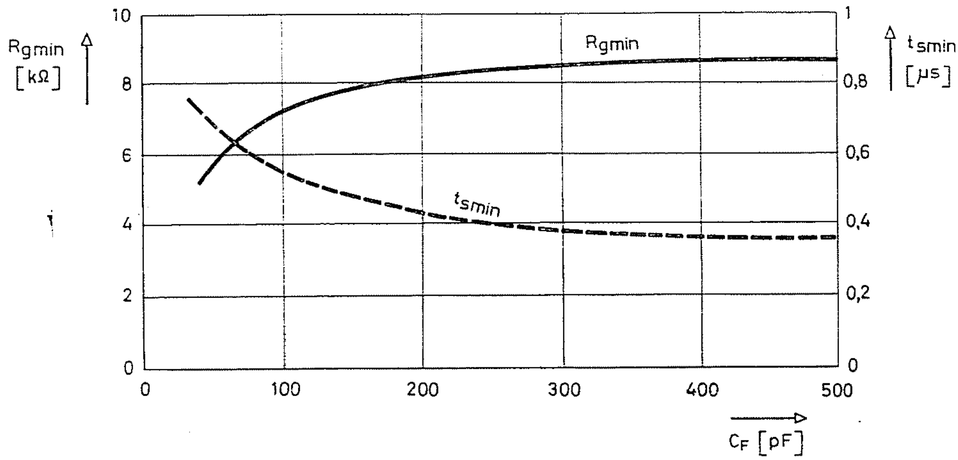

Fig. 15. Optimum generator resistance and minimum settling time vs. feedforward capacitance C_F

In the case of an error band below 0.1 per cent, the distance of the closed-loop zero-pole pair with smaller absolute value decreases below the error band in the smaller region of R_g, thus no individual adjustment is possible, for the settling time may then considerably increase as compared with the case without feedforward.

Even in the most favourable cases, the extent of the decrease of the settling time is smaller than that of the improvement of other dynamic parameters. For if the effect of the pole-zero pairs upon the settling time was neglected, a settling time of

$$t_s = 0.28 \ \mu s$$

ought to be obtained for the error band of 0.1 per cent, with the assumption of an angular frequency $\omega_1 = 2.5 \cdot 10^7$ r/s and an ideal slope of -20 dB/D as the absolute value of loop gain.

Summary

The paper examines how much the feedforward design improving the other dynamic features of inverting operational amplifiers reduces the settling time in the linear domain range. The undesirable pole of the preamplifier, which is the main barrier of the dynamic properties in the cases without feedforward, was found to produce a parasitic pole-zero pair in the closed-loop transfer function in the case of feedforward. A similar parasitic pole-zero pair resulted in the closed-loop transfer function from the parameter deviations of the elements adjusting the required frequency response in the individual amplifying stages. The presence of parasitic pole-zero pairs, on the other hand, may lead to a considerable increase of the settling time. Feedforward was seen to improve the settling time in the case only if the value of the low frequency loop gain produced by disconnecting the preamplifier was higher than the reciprocal of the relative error band. From an examination of the feedforward compensation of the second generation integrated operational amplifiers it could be stated that the settling time defined for the error band below 0.1 per cent cannot be reduced by feedforward compensation, on the contrary, a feedforward may considerably increase the settling time in the linear domain. The settling time defined for the error band of 0.1 per cent can be decreased by individual adjustment.

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APPENDIX

App. 1. *Open-loop transfer function of the feedforward amplifier (Fig. 2a)*

The transfer functions of the different stages of feedforward amplifiers shown in Fig. 2a, under consideration of the primary time constants important for the resulting frequency response:

$$A_1 = A_{10} \cdot \frac{1}{1 - \frac{s}{p_F}} \qquad \text{(App. 1)}$$

$$A_2 = A_{20} \cdot \frac{\frac{s}{p_F}}{1 - \frac{s}{p_F}} \qquad \text{(App. 2)}$$

$$A_3 = A_{30} \cdot \frac{1}{1 - \frac{s}{p_p}} \qquad \text{(App. 3)}$$

After introducing thy symbol

$$k = \frac{A_{20}}{A_{10}} \qquad \text{(App. 4)}$$

the transfer function of the open loop amplifier will be of the form:

$$A = (A_1 + A_2) \cdot A_3 = \underbrace{A_{10} \cdot A_{30}}_{A_0} \cdot \underbrace{\frac{1 - \frac{s}{p_F}(1 + k) + \frac{s^2}{p_d \cdot p_F} k}{\left(1 - \frac{s}{p_d}\right)\left(1 - \frac{s}{p_F}\right)\left(1 - \frac{s}{p_p}\right)}}_{a(s)} \qquad \text{(App. 5)}$$

The loop gain will be:

$$L = \beta_0 A = \beta_0 A_0 a(s) = L_0 a(s)\,, \tag{App. 6}$$

where, supposing the feedback resistance to be frequency independent, and neglecting the input impedance of the operational amplifier — the relationship

$$\beta_0 = \frac{R_1}{R_1 + R_2} \tag{App. 7}$$

is valid for the inverting amplifier according to Fig. 1a. Above the angular frequency

$$\omega = -p_{\mathrm{d}}$$

determined by the dominant open loop pole, the frequency characteristic of the loop gain will have a slope of -20 dB/D if the zeros z_1, z_2 of $a(s)$ coincide in sequence with a pole each, i.e.,

$$z_1 = p_{\mathrm{F}} \tag{App. 8}$$

$$z_2 = p_{\mathrm{d}} \tag{App. 9}$$

where

$$z_{1,2} = \frac{1+k}{2k} \cdot p_{\mathrm{d}} \left(1 \mp \sqrt{1 - \frac{4k}{(1+k)^2} \cdot \frac{p_{\mathrm{F}}}{p_{\mathrm{d}}}}\right). \tag{App. 10}$$

Disregarding now the solution $p_{\mathrm{F}} = 0$, the conditions of the ideal frequency response, on the basis of Eqs (App. 8 to App. 10) will be:

$$p_{\mathrm{F}} = p_{\mathrm{d}} \tag{App. 11}$$

$$p_{\mathrm{p}} = \frac{p_{\mathrm{d}}}{k} = \frac{A_{10}}{A_{20}} \cdot p_{\mathrm{d}}. \tag{App. 12}$$

If a further pole p_0 is taken into consideration in the 1st amplifying stage, i.e.,

$$A_1 = A_{10} \frac{1}{\left(1 - \frac{s}{p_{\mathrm{d}}}\right)\left(1 - \frac{s}{p_0}\right)} \tag{App. 13}$$

then the open loop transfer function will be of the form:

$$A = A_0 \cdot \frac{1 - \frac{s}{p_{\mathrm{p}}}(1+k) + \frac{s^2}{p_{\mathrm{F}}\,p_{\mathrm{d}}} k \left(1 + \frac{p_{\mathrm{d}}}{p_0}\right) - \frac{s^3}{p_{\mathrm{F}}\,p_{\mathrm{d}}\,p_0} \cdot k}{\left(1 - \frac{s}{p_{\mathrm{d}}}\right)\left(1 - \frac{s}{p_0}\right)\left(1 - \frac{s}{p_{\mathrm{F}}}\right)\left(1 - \frac{s}{p_{\mathrm{d}}}\right)}. \tag{App. 14}$$

Neglecting the effect of p_F i.e., introducing the substitution $p_{\mathrm{F}} = 0$ then:

$$A = A_0 \cdot \frac{1 + k - \frac{s}{p_{\mathrm{d}}} \cdot k(1+l) + \frac{s^2}{p_{\mathrm{d}}} \cdot l \cdot k}{\left(1 - \frac{s}{p_{\mathrm{d}}}\right)\left(1 - \frac{s}{p_0}\right)\left(1 - \frac{s}{p_{\mathrm{p}}}\right)} \tag{App. 15}$$

where the pole p_0 is characterized by the relationship

$$p_0 = \frac{p_{\mathrm{d}}}{l}\,. \tag{App. 16}$$

Accordingly, the zeros are obtained from the equation:

$$z_{1,2} = \frac{1+l}{2} p_{\mathrm{d}} \left(1 \pm \sqrt{1 = \frac{4(k+1) \cdot l}{k(1+l)^2}}\right). \tag{App. 17}$$

App. 2. *The open-loop transfer function of the integrated operational amplifier type 748 in the case of feedforward compensation*

A typical representative of the "second generation" of the integrated operational amplifiers is the amplifier type *748*, the simplified model of which with inverting feedback is shown in Fig. 9. Under consideration of the equivalent generator resistance

$$R_g = R_1 \times R_2 \qquad \text{(App. 18)}$$

the open-loop transfer function of the amplifier obtained by simple computation [1] will be:

$$A = A_0 \cdot \frac{1 + a_1 s + a_2 s^2}{1 + b_1 s + b_2 s^2 + b_3 s^3} \qquad \text{(App. 19)}$$

where

$$a_1 = \frac{R_d \cdot C_F}{A_{10}} \qquad \text{(App. 20)}$$

$$a^2 = -a_1 \cdot \frac{1}{p_0} \qquad \text{(App. 21)}$$

$$b_1 = -\left(\frac{1}{p_{d0}} + \frac{1}{p_0}\right) + C_F \, [R_d - R_g(A_{10} - 1)] \qquad \text{(App. 22)}$$

$$b_2 = \frac{1}{p_{d0}\, p_0} - C_F \left[\frac{1}{p_{d0}} R_g + \frac{1}{p_0}(R_g + R_d)\right] \qquad \text{(App. 23)}$$

$$b_3 = \frac{C_F \cdot R_g}{p_{d0} \cdot p_0} \qquad \text{(App. 24)}$$

and

$$p_0 = -\frac{1}{R_0 \cdot C_0}$$

$$p_0 = -\frac{1}{R_d\, C_d}$$

$$A_{10} = g_1 \cdot g_2 \cdot R_0 \cdot R_d \, .$$

The typical model parameters of the operational amplifier on the basis of data sheets and own measurements [1]:

$R_{IN} = 2$ Mohm; $g_1 = 0.1$ A/V; $R_0 = 10$ kohm; $C_0 = 10$ pF

$g_2 = 0.12$ mA/V; $R_d = 5$ Mohm

$g_3 = 3.33$ A/V; $R_{OUT} = 75$ ohm;

and thus :

$A_{10} = 600$; $A_{20} = -250$; $A_0 = A_{10} A_{20} = 150{,}000$; $p_0 = -10^7$ r/s.

App. 3. *Numerical analysis of operational amplifiers*

The linear network analysis program ANP3 [4] was used for examining the model of the unity gain inverting circuit constructed with $R-C$ elements and a voltage-controlled current generator. The model accomplished the transfer functions (App. 1 to App. 3) and (App. 13) of the feedforward amplifier shown in Fig. 2a.

Technical data of the amplifiers of type A and B chosen as examples:

Amplifier A	Amplifier B
$A_0 = 10^6$	$A_0 = 10^6$
$A_{10} = 10^3$	$A_{10} = 10^3$
$A_{20} = 1$	$A_{20} = 10$
$A_{30} = 10^3$	$A_{30} = 10^3$
$k = 10^{-3}$	$k = 10^{-2}$
$p_{\mathrm{did}} = -10^2$ r/s	$p_{\mathrm{did}} = -10^2$ r/s
$p_{\mathrm{F}} = -10^2$ r/s	$p_{\mathrm{F}} = -10^2$ r/s
$p_{\mathrm{p}} = -10^5$ r/s	$p_{\mathrm{p}} = -10^4$ r/s

The relative distance of the open-loop and closed-loop parasitic pole-zero pair was determined in the range $a_2 = -0.7 \div + 0.7$ by changing p_d. The settling time defined for the relative error bands $h = 0.1\%$ and $h = 0.01\%$ was also determined by an analysis of the time domain. The results are contained in Figs 6 and 7.

The effect of the pole p_0 of the 1st amplifier was examined with the value $p_d = p_{\mathrm{did}}$ in the domain

$$p_0 = p_{\mathrm{p}} \div (-\omega_1).$$

The operational amplifier type *748* in the configuation of an inverting amplifier with unity gain was analysed by means of the model shown in Fig. 9 with the typical data given in App. 2. During the examinations the product $R_g \cdot C_D$ was kept constant (so as to ensure $\omega_1 \simeq 2.5 \cdot 10^7$ r/s). By means of the ANP3 program the closed-loop pole-zero configuration was determined for different values of R_g and C_F, further the settling time by means of the APLAC2 transient analysis program [5] completed with a program segment determining the settling time (SETIME program). Since the settling time is intricately related with the free parameters, a simple three-parameter optimizing program (SETOPT) was elaborated, using a simple version of the steepest descent. The basic segment of the program is APLAC2, or rather its variant SETIME suitable for determining the settling time. With a fixed value of $R_g \cdot C_D$ the program was used for determining the optimum of the settling time by search with one and two parameters.

Numerical analyses were carried out by a UNIVAC 1108 computer (ANP3), and partly by a HP 2000 F computer (APLAC2, SETIME, SETOPT) in the Computing Centre of the Helsinki University of Technology.

References

1. Telkes, B.: Programvezérelhető analóg elektronikus áramkörök beállítási tulajdonságainak optimalizálása (Optimization of the Settling Time of Programmable Analog Electronic Circuits). Cand. Eng. Sci. Thesis, Budapest 1972.
2. Dobkin, R. C.: Feedforward Compensation Speeds Op. Amp. National Semiconductor LB—**2**, 1969.
3. P. R. Gray—R. G. Meyer: Recent Advances in Monolithic Operational Amplifier Design. IEEE Transaction on Circuits and Systems, Vol. CAS—**21**, No. 3, May 1974.
4. Sorensen, E. V.: ANP3 — A Linear Semisymbolic Circuit Analysis Program Based on Algebraic Eigenvalue Technique. Report 4/10—72, Institute of Circuit Theory and Telecommunication, Technical University of Denmark.
5. Valtonen, M.: APLAC2 — A Flexible DC and Time Domain Circuit Analysis Program for Small Computers. Helsinki University of Technology. Radiolaboratory, Report S **56**, 1973.

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