ON THE GATE CURRENT OF JUNCTION FIELD EFFECT TRANSISTORS

By

A. AMBRÓZY

Department of Electron Valves and Semiconductors,
Technical University, Budapest

(Received March 31, 1970)

Presented by Prof. Dr. I. P. VALKÓ

Recently, several papers [1—4] discussed an "anomalous" component of the gate current of a JFET or the substrate current of an IGFET at higher drain voltages. Some differences exist, however, in the presentation, and mainly in the explanations of the observed results. FOWLER [1] observed that at moderately high drain voltages (beyond pinch-off) the gate current of n-channel devices becomes approximately linear dependent on drain current, and increases rapidly with drain voltage. No p-channel device showed this phenomenon at and above room temperature.

RYAN [2] investigated this gate current component at low temperatures and showed its existence in p-Ge, n-Si and p-Si. He found the I_G/I_D ratio to be *nearly* constant over a wide range of values of I_D, supposing V_{DG} = constant. He used pulsed bias voltages for avoiding self-heating of the device. However, the pulse technique is inherently less accurate, particularly taking into consideration the transients caused by the drain-gate capacitance, especially at low gate current levels. In these cases the self-heating does not introduce considerable error.

If we attribute this current to impact ionization effects due to majority carriers moving with saturated drift velocity [5] then the above mentioned linear relationship between I_G and I_D should rigorously exist, assuming constant probability of impact ionization. To verify this and to separate the various components of the gate current, more refined experimental technique, specially designed for this purpose, is necessary.

Circuit

Since I_D is the independent variable, it should not be influenced by V_{DG}, V_{GS}, ambient temperature, etc. A very simple and adjustable current source was chosen: for n or p channel JFETs, npn or pnp bipolar transistors were used, respectively, in common base configuration. Except of $V_{GS} = 0$

($I_D = I_{DSS}$) the collector-base junction is sufficiently reverse biased and even $V_{CB} = 0$ does not considerably deteriorate the output resistance of the bipolar silicon transistor. If extremely high output resistance (i.e. complete independence on V_{GS}) is required, a FET-bipolar combination [6] may be used.

The gate current component considered here increases very rapidly with V_{DG}. Therefore voltage drops in the drain and gate leads should be minimized.

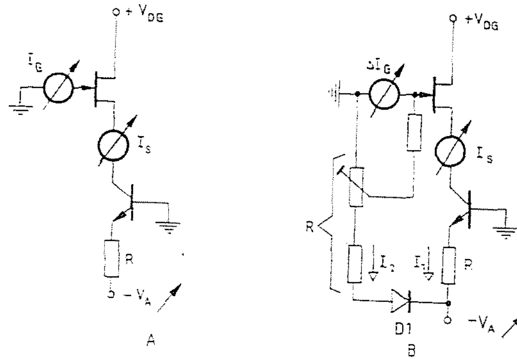

Fig. 1. A. Circuit for measuring gate current; B. Modified version for compensating I_G

It requires a very low resistance ammeter in the drain circuit or, even better, to measure I_S instead of I_D, since $I_G \ll I_D$ (Fig. 1A).

I_D is adjustable by a variable auxiliary voltage source. This may be used also for compensating I_G; in the circuit of Fig. 1B the meter ΔI_G indicates only the deviation from the linear relationship between I_G and I_D. Also the voltage drop accross the meter is zero or negligible. Diode D1 provides the similarity of I_1—V_A and I_2—V_A curves.

Experimental results

At first the gate-channel current components I_{GS} and I_{GD} with the drain and source floating, respectively, were checked at room temperature with different reverse biases in order to indicate whether the structure of the FET is symmetrical or not. A few devices showed slight asymmetry probably in surface leakage component, but even their pinch-off voltages were invariant to reversing drain and source. Two typical structures are shown in Fig. 2.

Fig. 3 shows typical log I_G *vs.* log I_D curves of n and p channel devices at room temperature. The slopes of the best fit straight lines are indicated. Good linearity has been found for n-channel devices, but for p ones generally

$$I_G = cI_D^m \tag{1}$$

holds (at least in a decade of I_D), where m ranges from a small negative value to about $+0.5$ depending on V_{DG}. This indicates clearly that in p devices at room temperature I_G exhibits the I_D dependent increase only at very high channel fields and I_G is caused mainly by thermally generated minority carriers.

By cooling down the devices the thermally generated component of I_G disappears and the other one gradually increases. Fig. 4 shows typical I_G/I_D

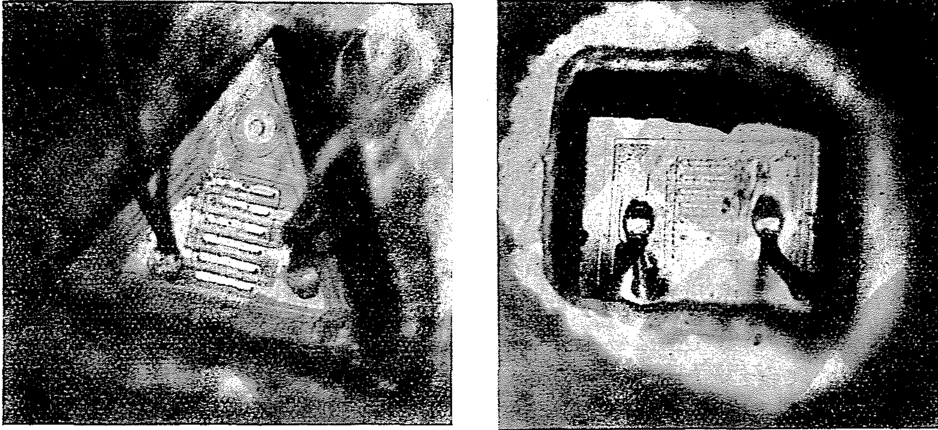

Fig. 2. Microphotograph of an A) n-channel. B) p-channel JFET

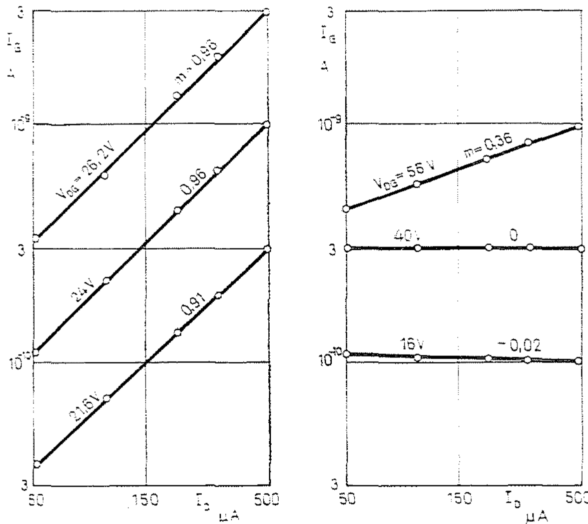

Fig. 3. Gate current *vs.* drain current of A) a typical n device, B) a typical p device

vs. T curves of n and p devices. All curves were measured at $I_D = 0.5$ mA and the slopes m of Eq. (1) are also indicated in Fig. 4 for 50 μA $< I_D <$ 500 μA. Log (I_G/I_D) *vs.* log T may well be approximated by straight lines having slightly different slopes for different devices of the same channel type but these slopes range generally between —2.7 . . .—3.7 for n and —1.4 . . .—2.6 for p devices.

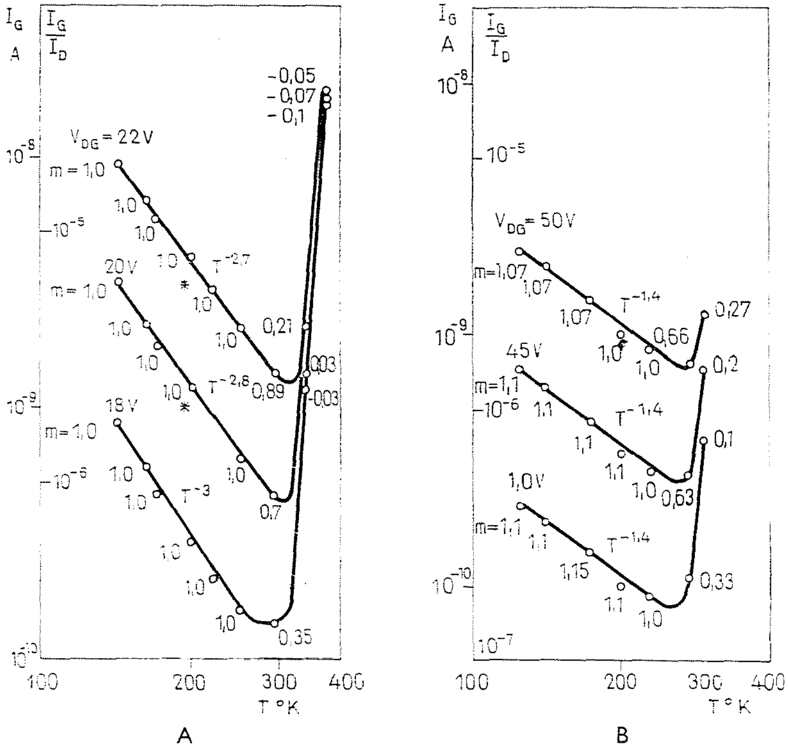

Fig. 4. I_G/I_D *vs.* absolute temperature of A) a typical n device, B) a typical p device

In some cases (when V_{DG} was not switched off during the cooling) n devices showed a decrease of I_G and an irregular increase of V_{GS} below —20 °C (typical points marked by* in Fig. 4A). Considering Fig. 1A, an irregular increase of V_{GS} (keeping I_D constant) is possible only if a leakage is formed between drain and source. The oxidized surface of a planar processed transistor generally contains a low density of positive ion impurities having temperature-dependent mobility; if they are collected by the high electric field around the gate (Fig. 5) and are immobilized by the cooling, an n-type inversion layer can be formed under the oxide, shunting the bulk-channel between drain and source. No p-device showed this irregularity indicating one type of surface impurity.

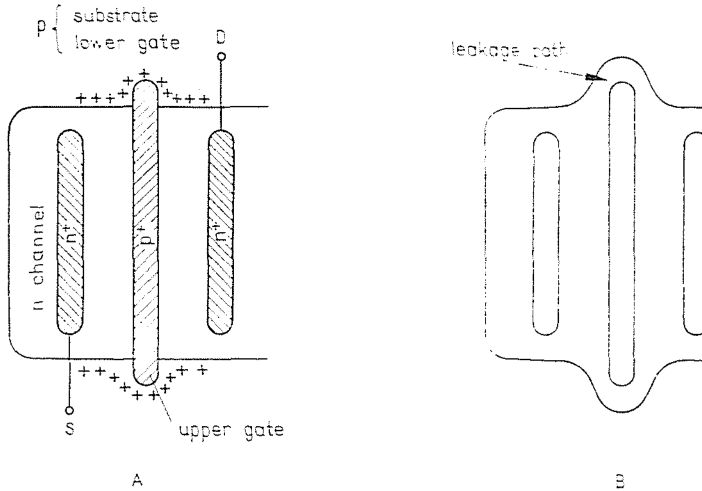

Fig. 5. Electrodes and positive charges A) on the surface, B) under the oxide forming a leakage path

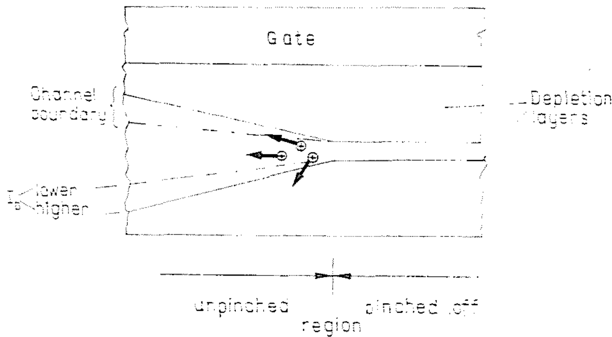

Fig. 6. Drain-current dependent channel geometry

Discussion

The similarity of the dependence of I_G/I_D on T and V_{DG} for both n and p JFETs (compare Fig. 4A and B) does not support the model proposed by FOWLER [1] namely hole emission from the drain to the channel. This seems to be improbable [7] since in the heavily doped drain electrode the minority carrier density is much less than in the channel. The negative temperature coefficient of the *current* also contradicts the emission theory. Moreover there is no explanation of the different phenomena observed in n and p devices at room temperature (Fig. 3).

Assuming that the impact ionization model proposed by RYAN [2] is valid with some refinements, let us try to explain the experimental results.

Fig. 4 indicates clearly that both types of devices have at least two components of I_G : I_{G1} attributed to impact ionization (neg. temp. coeff.) and I_{G2} attributed to thermal generation (pos. temp. coeff.). At room temperatures and at lower values of V_{DG}, $I_{G2} \gg I_{G1}$ for p-channels. The small negative slope of Fig. 3B for $V_{DG} = 16$ V, $T = 300$ °K (and the same for n devices at about 370 °K, see Fig. 4A) is the consequence of the volume variation of the depletion layer. Assuming that the minority carriers are thermally generated within the depletion region the increase of I_D is associated with a larger channel volume and therefore the volumes of the depletion layers decrease. On the other hand, the drain current dependence of I_{G1} overcompensates I_{G2} at $V_{DG} = 56$ V.

According to Fig. 4, $I_{G1} \propto T^{-s}$ where $s_p \neq s_n$. It is believed that this difference gives better insight into the interaction between lattice vibration and majority carriers travelling with drift velocity. RYAN [2] suggested that $s_n = s_p = 3/2$, however, his Fig. 3 shows rather exponential relationship. Since holes have lower mobility and lower limiting velocity than electrons, the probability of impact ionization will be less, which explains the lower contribution of I_{G1} to I_G of p devices at room temperature.

If the field strength along the pinched-off channel were constant and known, the I_G/I_D ratio would give directly the ionization probability α in function of E and T, approximated by GUNN [8] as

$$\alpha = A \exp\left(-\frac{B}{E^2 l^2 (T, E)}\right) = \alpha(T, E) \tag{2}$$

well below the avalanche region, where A and B are material constants, different for electrons and holes and l is the mean free path between two collisions. All minority carriers generated by impact ionization have the chance to leave the pinched-off region without recombination since the length of that region is in the order of a few microns and the drift velocity is about 10^7 cm/s; the transit time is in the order of 10^{-10} s, much less than the average lifetime.

Despite the big efforts to calculate the field distribution in the FET channel, it is still unknown. Careful investigation of the gate current, however, may lead to a different approach of the problem. The observed deviations from $m = 1$ at low temperatures where only I_{G1} is important are certainly related to the *shape* of the channel. Assume that the field strength is sufficient for impact ionization before the majority carriers reach the "entrance" of the pinched-off region (Fig. 6). The minority carriers generated in this particular narrowing edge may be collected either by the gate or the source. Lower I_D involves narrower unpinched region of the channel and less probability of a source-collected minority current, resulting in a relative increase of the gate current ($m > 1$).

The impact ionization model is also in agreement with the observations regarding the unwanted surface inversion layer. In that case, if the bulk channel current is partly shunted, I_{G1} should decrease. This is verified experimentally as asterisks show in Fig. 4*a*.

*

The work reported in this paper was done during the visit of the author at the Eindhoven University of Technology, The Netherland. He is indebted to Prof. H. Groendijk and Dr. M. M. Abu-Zeid for the many helpful discussions and to Mr. H. Moerman for the technical assistance.

Summary

The gate current of *n* and *p* JFETs was experimentally investigated in a wide temperature range. Besides the thermally generated minority current another component exists which can be quite large at low temperatures. Different temperature coefficients were found for *n* and *p* channel devices. The observed phenomena may lead to a better understanding of the impact ionization mechanism and/or of the field distribution in a FET.

References

1. Fowler, E. P.: Effect of operating conditions on reverse gate current of junction FETs. Electronics Letters **4**, 216–217 (1968).
2. Ryan, R. D.: The gate currents of junction field effect transistors at low temperatures. Proc. IEEE **57**, 1225–1226 (1969).
3. Nakahara, M. & al.: Anomalous enhancement of substrate terminal current in n-channel MOST. Proc. IEEE **56**, 2088–2090 (1968).
4. Ryan, R. D.: Substrate current in silicon p-channel MOS transistors. Proc. IEEE. **57** 1424–1425 (1969).
5. Grebene, A. B.—Gandhi, S. K.: Pinched mode operation of field effect transistors. Proc. IEEE **57**, 230–231 (1969).
6. Ambrózy, A.: Current source with infinite internal resistance. Electronics Letters **3**, pp 68–69 (1967).
7. Dacey, G. C.: —Ross, I. M.: The field-effect transistor. Bell Syst. Techn. J. **34**, 1158 (1955).
8. Gunn, J. B.: High electric field effects in semiconductors. Progress in Semiconductors. Vol. 2. pp 213–247, London, 1958, Heywood.

Prof. Dr. András Ambrózy, Budapest XI. Műegyetem rkp. 9. Hungary