NEW EXCLUSIVE OR CIRCUITS USING CONTROLLED TRANSISTOR INVERTERS

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Introduction

The definition of Exclusive OR operation:

$$x_1 \oplus x_2 = x_1\bar{x}_2 + \bar{x}_1 x_2 \tag{1}$$

The definition of equivalence operation:

$$x_1 \odot x_2 = x_1 x_2 + \bar{x}_1 \bar{x}_2 \tag{2}$$

Both operations are associative; that is:

$$(x_1 \oplus x_2) \oplus x_3 = x_1 \oplus (x_2 \oplus x_3) \tag{3}$$

$$(x_1 \odot x_2) \odot x_3 = x_1 \odot (x_2 \odot x_3) \tag{4}$$

Both operations are commutative, that is:

$$x_1 \oplus x_2 = x_2 \oplus x_1 \tag{5}$$

$$x_1 \odot x_2 = x_2 \odot x_1 \tag{6}$$

Relations between the Exclusive OR and equivalence operations:

$$x_1 \oplus x_2 = \overline{x_1 \odot x_2} = x_1 \odot \bar{x}_2 = \bar{x}_1 \odot x_2 \tag{7}$$

$$x_1 \odot x_2 = \overline{x_1 \oplus x_2} = x_1 \oplus \bar{x}_2 = \bar{x}_1 \oplus x_2 \tag{8}$$

The output of an n input Exclusive OR gate:

$$x_1 \oplus x_2 \oplus x_3 \ldots \oplus x_i \ldots \oplus x_n = \begin{cases} 1 & \text{if } k = 2p \quad \cdot 1 \\ 0 & \text{if } k = 2p \end{cases} \tag{9}$$

where: k = the number of logical variables x_i equal to 1
$n-k$ = the number of logical variables x_i equal to 0
p = positive integer

The relation (9) shows that the logical value of the output function of n variables can be obtained by the examination of parity.

The output of an n input equivalence gate:

a) If $n = 2m$, then:

$$x_1 \odot x_2 \odot x_3 \ldots \odot x_i \ldots \odot x_n = \begin{cases} 1 \text{ if } k = 2p \\ 0 \text{ if } k = 2p-1 \end{cases} \tag{10}$$

b) If $n = 2m+1$, then:

$$x_1 \odot x_2 x_3 \ldots \odot x_i \ldots \odot x_n = \begin{cases} 1 \text{ if } k = 2p-1 \\ 0 \text{ if } k = 2p \end{cases} \tag{11}$$

where: k = the number of logical variables x_i equal to 1
$n-k$ = the number of logical variables x_i equal to 0.
m, p = positive integers

The relations (9), (10), (11) can easily be proved by the definitions and identities in (1) through (8).

In consequence of the relations (9) and (11):

$$x_1 \oplus x_2 \oplus x_3 \ldots \oplus x_i \ldots \oplus x_{2m+1} =$$
$$x_1 \odot x_2 \odot x_3 \ldots \odot x_i \ldots \odot x_{2m+1} \tag{12}$$

In consequence of the relations (9) and (10):

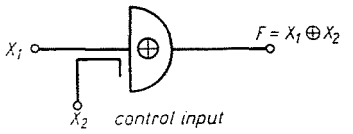
$$x_1 \oplus x_2 \oplus x_3 \ldots \oplus x_i \ldots \oplus x_{2m} = \tag{13}$$
$$= \overline{x_1 \odot x_2 \odot x_3 \ldots \odot x_i \ldots \odot x_{2m}}.$$

Let the controlled inverter be defined as a two input one output logical circuit, which operates either as an inverter or a follower between the other input and the output depending on the value of logical variable at the control input.

It is easy to demonstrate, comparing the definition of controlled inverter and the definitions in (1), (2), that both the Exclusive OR and the equivalence operations can be realized by controlled inverter.

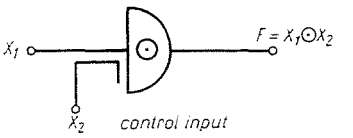
The symbol for a controlled inverter realizing the Exclusive OR operation and its operation table are shown in Fig. 1.

The symbol for a controlled inverter realizing the equivalence operation and its operation table are shown in Fig. 2.



X_1	X_2	Operation	F
0	0	Follower	0
1	0	Follower	1
0	1	Inverter	1
1	1	Inverter	0

Fig. 1



X_1	X_2	Operation	F
0	0	Inverter	1
1	0	Inverter	0
0	1	Follower	0
1	1	Follower	1

Fig. 2

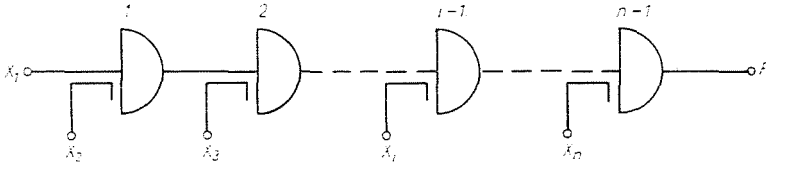


Fig. 3

The difference between the two controlled inverters is that the control logical variables belonging to the same operation are the complements of each other.

Since both the Exclusive OR and the equivalence operations are associative, in the case of n input logical variables $(n-1)$ controlled inverters connected in cascade realize the output logical function F, as it is shown in Fig. 3.

The realization of controlled inverter

The operation of the described circuits is based on the fact that the transistor gains also if the emitter and the collector are commuted mutually, although its inherent current gain drops off.

These circuits form negative logic, but positive logic can be realized as well, if the transistor types are changed from PNP to NPN.

A possible controlled inverter circuit realizing the Exclusive OR operation is shown in Fig. 4.

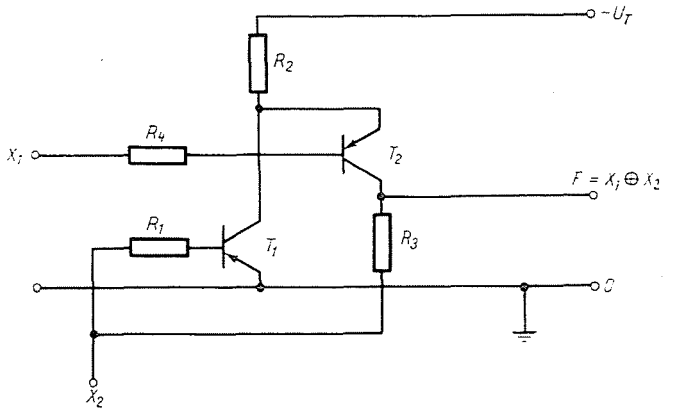


Fig. 4

The operation of principle of the circuit in Fig. 4

Let "non" level be at the control input x_2. In that case transistor T_1 is cut off, the emitter of transistor T_2 is connected to negative voltage by resistor R_2, the collector of transistor T_2 is connected to zero volts by resistor R_3. Thus the transistor T_2 operates as a follower between the input x_1 and the output F.

Let "yes" level be at the control input x_2. In that case transistor T_1 goes into saturation and switches the emitter of transistor T_2 to a voltage of about zero volts, the collector of transistor T_2 is connected to the negative voltage at the control input x_2 by resistor R_3. Thus the transistor T_2 operates as an inverter between the input x_1 and the output F.

In this circuit the current gain of transistor T_2 is low, when it operates as a follower, and high, when it operates as an inverter.

Another possible controlled inverter circuit realizing the Exclusive OR operation is shown in Fig. 5.

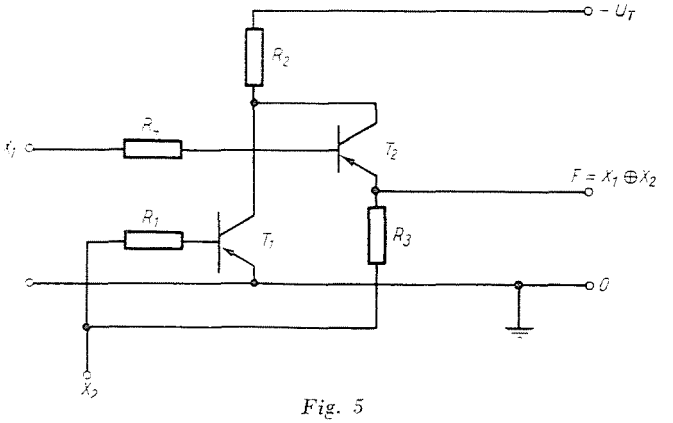


Fig. 5

The operation of principle of the circuit in Fig. 5

Let "non" level be at the control input x_2. In that case transistor T_1 is cut off, the collector of transistor T_2 is connected to negative voltage by resistor R_2, the emitter of transistor T_2 is connected to zero volts by resistor R_3. Thus the transistor T_2 operates as a follower between the input x_1 and the output F.

Let "yes" level be at the control input x_2. In that case transistor T_2 goes into saturation and switches the collector of transistor T_2 to a voltage

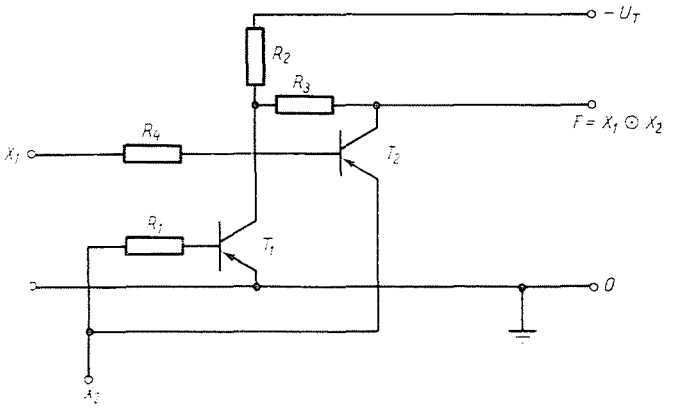


Fig. 6

of about zero volts, the emitter of transistor T_2 is connected to the negative voltage at the control input x_2 by resistor R_3. Thus the transistor T_2 operates as an inverter between the input x_1 and the output F.

In this circuit the current gain of transistor T_2 is high, when it operates as a follower, and low, when it operates as an inverter.

A possible controlled inverter circuit realizing the equivalence operation is shown in Fig. 6.

The operation of principle of the circuit in Fig. 6

Let "non" level be at the control input x_2. In that case transistor T_1 is cut off, the collector of transistor T_2 is connected to negative voltage by resistors R_2 and R_3, the emitter of transistor T_2 is connected to zero volts. Thus the transistor T_2 operates as an inverter between the input x_1 and the output F.

Let "yes" level be at the control input x_2. In that case transistor T_1 goes into saturation and switches the collector of transistor T_2 to a voltage of about zero volts through resistor R_3, the emitter of transistor T_2 is connected to the negative voltage at the control input x_2. Thus transistor T_2 operates as a follower between the input x_1 and the output F.

In this circuit the current gain of transistor T_2 is high, when it operates as an inverter, and low, when it operates as a follower.

Another possible controlled inverter circuit realizing the equivalence operation is shown in Fig. 7.

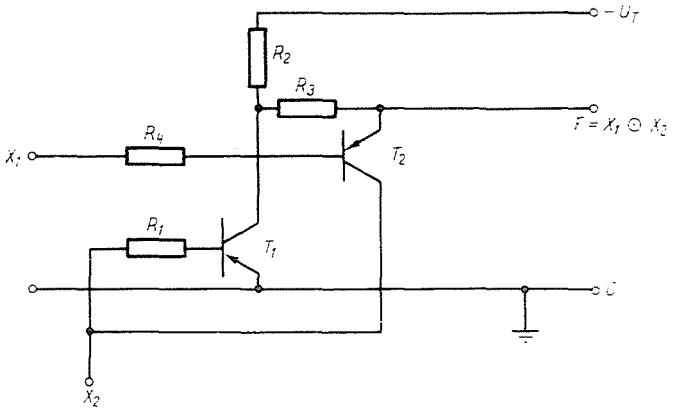


Fig. 7

The operation of principle of the circuit in Fig. 7

Let "non" level be at the control input x_2. In that case transistor T_1 is cut off, the emitter of transistor T_2 is connected to negative voltage by resistors R_2 and R_3, the collector of transistor T_2 is connected to zero volts. Thus, transistor T_2 operates as an inverter between the input x_1 and the output F.

Let "yes" level be at the control input x_2. In that case transistor T_1 goes into saturation and switches the emitter of transistor T_2 to a voltage of about zero volts through resistor R_3, the collector of transistor T_2 is connected to the negative voltage at the control input x_2. Thus, transistor T_2 operates as a follower between the input x_1 and the output F.

In this circuit the current gain of transistor T_2 is low, when it operates as an inverter, high, when it operates as a follower.

In all the four circuits the function of resistor R_4 is to increase the low output resistance of the controlled inverter, when it operates as a follower and the low input resistance of the controlled inverter, when it operates as an inverter.

Any one of these circuits connected in cascade as it is shown in Fig. 3 requires a signal standardization, because of the less than one voltage gain of the controlled inverters operating as followers.

The design of controlled inverter

As an example let an $n = 8$ input Exclusive OR gate be designed. Let the type-circuit in Fig. 6 be chosen.

The number of necessary controlled inverters:

$$n - 1 = 7$$

In consequence of Eq. (13) the circuit standardizing the output signal will be an inverter.

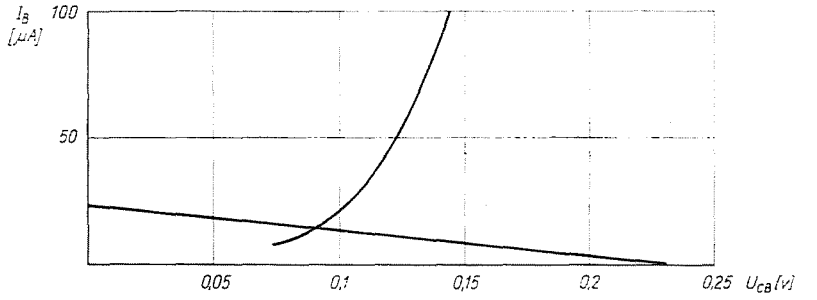


Fig. 8

The drop of logical level is the highest, when all the seven controlled inverters operate as followers. As 1.4 V is sufficient to have the output inverter operated, the permissible drop of logical level across the seven controlled inverters:

$$U_d = U_{\log} - 1.4\ \text{V} = 3\ \text{V} - 1.4\ \text{V} = 1.6\ \text{V}$$

where: $U_{\log}$ = the logical "yes" level

The permissible drop of logical level across one controlled inverter:

$$U_{d/1\ \text{stage}} = \frac{1.6}{7}\ \text{V} = 0.23\ \text{V}$$

Let this value be regarded as the highest permissible voltage drop across any one of the seven controlled inverters.

The following transistors are chosen:

T_1 = OC 1045

T_2 = OC 1044

The characteristics of transistor T_2 must be measured, commuted the emitter and the collector of transistor.

The characteristics $I_B = I_B(U_{CB})$ is shown in Fig. 8, the directions of currents and polarity of voltages are shown in Fig. 9.

The characteristics $I_E = I_E(I_B)$:

$$I_E = \beta\, I_B$$

where $\beta = 2$, if $U_{CE} = 0.2$ V

$\beta = 2-3$, if $U_{CE} = 0.2$ V $-$ 3 V

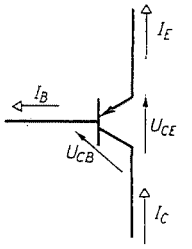


Fig. 9

The transistor OC 1044 enduring a base current of about 280 μA, the value of resistor R_4 can be 10 kΩ. So, if anyone of the seven controlled inverters operates as a follower, the following one as an inverter, the base current will be:

$$I_B \approx \frac{U_{\log} - U_{d/\text{1stage}}}{R_4} \approx \frac{2.8\ V}{10\ k\Omega} = 280\ \mu A$$

The value of resistor R_4 being given, the characteristics of resistor R_4 can be drawn in the characteristics $I_B = I_B(U_{CB})$.

Segments:

$$U_{CB} = U_{d/\text{1stage}} = 0.23\ V$$

$$I_B = \frac{U_{CB}}{R_4} = \frac{0.23\ V}{10\ k\Omega} = 23\ \mu A$$

The point of intersection of the two characteristics:

$U_{CB} = 0.09$ V

$I_B = 14\ \mu$A

The emitter current calculated by an average value $\beta = 2.5$

$I_E = \beta\, I_B = 2.5 \cdot 14\ \mu\text{A} = 35\ \mu\text{A}$

The collector current:

$$I_C = I_E + I_B$$

For the transistor T_2 of the following controlled inverter also consumes base current, the collector current will be:

$$I_C = I_E$$

Thus the value of resistor R_3:

$$R_3 = \frac{U_{\log} - U_{d/1\text{stage}}}{I_C} = \frac{3V - 0.23\,V}{0.035\,mA} = 80\,k\Omega\,.$$

If in all the seven controlled inverters the value of resistor R_3 is 80 kΩ, the voltage drop across one controlled inverter will not be constant, it is the highest across the first and the lowest across the seventh controlled inverter.

The value of resistor R_1 is chosen so that the logical "yes" level at the control input x_2 saturates transistor T_1. The base current necessary to saturate transistor T_1:

$$I_B \approx 150\,\mu\text{A}$$

Thus:

$$R_1 = \frac{3V}{0.15\,mA} = 20\,k\Omega$$

Let the value of resistor R_2 be:

$$R_2 = 10\ \text{k}\Omega$$

Thus U_{CE} is practically zero volts for $U_T < 20$ V.

The evaluation of supply voltage

If both transistors T_1 and T_2 are cut off, the current through resistors R_2, R_3, R_4 should be sufficient to the saturation of transistor T_2 of the following controlled inverter, which operates as an inverter. The base current necessary to the saturation of transistor T_2:

$I_B \approx 100\,\mu\text{A}$

Thus the supply voltage:

$$U_T = I_B(R_2 + R_3 + R_4) = 0.1\ \text{mA}\ (10 + 82 + 10)\ \text{k}\Omega$$

$$U_T = 10\ \text{V}$$

Summary

This paper reports on four new circuits realizing the Exclusive OR operation. The circuits are based on the fact, that the transistor also gains, when the emitter and collector are commuted mutually. Therefore the usual inverter operates as a follower, if the polarity of supply voltage is changed.

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