A NEW NOT-AND-EXCLUSIVE OR GATE

By

L. CSANKY

Department of Process Control, Technical University, Budapest

(Received November, 1, 1968)

Presented by Prof. Dr. A. FRIGYES

Introduction

The technique of expressing Boolean functions in terms of EXCLUSIVE OR and AND operations has been examined by REED [1] and MULLER [2, 3]. Both have shown that a function of n logical variables may be expressed in the following canonical form:

$$F(x) = h_0 \oplus h_1 x_1 \oplus \ldots \oplus h_n x_n \oplus h_{n+1} x_1 x_2 \oplus \ldots \ldots \oplus h_{2n-1} x_1 x_2 \ldots x_n \tag{1}$$

For example the canonical form for a three-variable logical function is:

$$F(x) = h_0 \oplus h_1 x_1 \oplus h_2 x_2 \oplus h_3 x_3 \oplus h_4 x_1 x_2 \oplus \oplus h_5 x_2 x_3 \oplus h_6 x_1 x_3 \oplus h_7 x_1 x_2 x_3 \tag{2}$$

COHN [4] has shown that the replacement, consistently throughout such a form, of any variable by its complement should yield an equally valid canonical form. The coefficients h_i for a given function may be altered.

If all the variables are replaced by their complements, the canonical form will be:

$$F(\bar{x}) = h_0 \oplus h_1 \bar{x_1} \oplus \ldots h_n \bar{x_n} \oplus h_{n+1} \bar{x_1}\bar{x_2} \oplus \ldots \oplus h_{2n-1} \bar{x_1}\bar{x_2} \ldots \bar{x_n} \tag{3}$$

Consequently, any logical function can be realized by the NOT-AND-EXCLUSIVE OR gate.

The logical realization of the NOT-AND-EXCLUSIVE OR gate

The logical diagram of the gate is shown in Fig. 1.

The output logical function F:

$$F = \overline{x_1 \oplus (x_{21} + x_{22} + \ldots + x_{2n})} \tag{4}$$

As

$$\overline{a \oplus b} = \bar{a} \oplus b = a \oplus \bar{b} \tag{5}$$

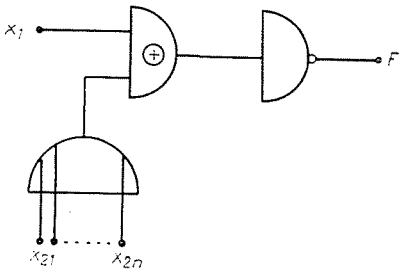

Fig. 1

Thus

$$F = x_1 \oplus (\overline{x_{21} + x_{22} + \ldots + x_{2n}}) \tag{6}$$

Applying the De Morgan theorems

$$F = x_1 \oplus \overline{x_{21}}\,\overline{x_{22}} \ldots \overline{x_{2n}} \tag{7}$$

Thus the gate in Fig. 1 operates as a NOT-AND-EXCLUSIVE OR gate. Let the symbol in Fig. 2 stand for the NOT-AND-EXCLUSIVE OR gate.

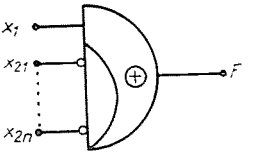

Fig. 2

If such gates are connected in cascade by the input x_1 and the output F, as shown in Fig. 3, then the output function will be:

$$F = x_1 \ominus \overline{x_{21}}\,\overline{x_{22}} \ldots \overline{x_{2n}} \oplus \overline{x_{31}}\,\overline{x_{32}} \ldots \overline{x_{3n}} \oplus \overline{x_{41}}\,\overline{x_{42}} \ldots \overline{x_{4n}} \oplus \ldots \ominus \overline{x_{k1}}\,\overline{x_{k2}} \ldots \overline{x_{kn}} \tag{8}$$

Noticeably the algebraic form for the output F (8) is conformable to the canonical form (3), hence any logical function of not more than n variables can be realized by the gates in Fig. 3.

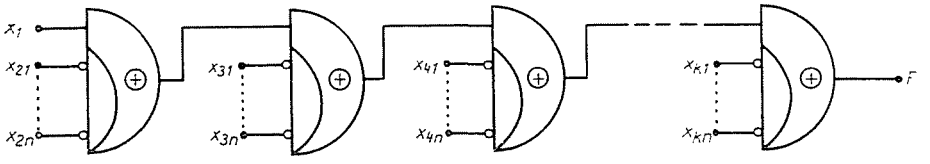

Fig. 3

The realization of the NOT-AND-EXCLUSIVE OR gate

The circuit realizing the NOT-AND-EXCLUSIVE OR gate is shown in Fig. 4.

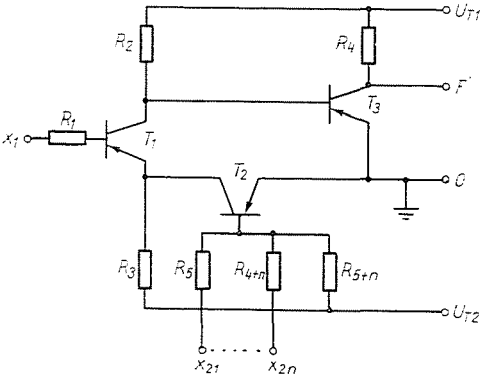

Fig. 4

The operation of the circuit:

Transistor T_3 operates as an output inverter and in addition performs the signal standardization.

Transistors T_1 and T_2 form an EXCLUSIVE OR circuit, in which transistor T_2 is so arranged that it can operate as an OR-NOT gate too. The EXCLUSIVE OR circuit is shown in Fig. 5.

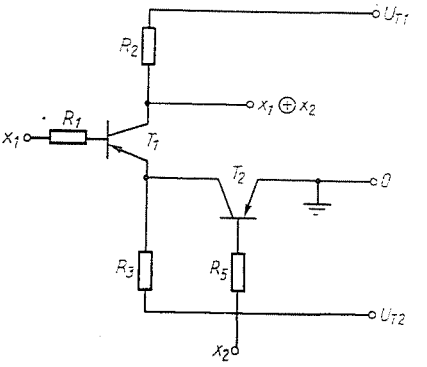

Fig. 5

The operation of the EXCLUSIVE OR circuit:

Let "not" level (0V) be at the input x_2. In that case transistor T_2 is cut off, hence transistor T_1 goes into saturation independently of the x_1 value, and the value of x_1 appears at its collector. Thus transistor T_1 operates as a follower.

Let "yes" level (—3V) be at the input x_2. In that case transistor T_2 goes

into saturation and switches the emitter of transistor T_1 to zero volts. Thus transistor T_1 operates as an inverter.

The operation of the OR-NOT gate formed from the transistor T_2 and the operation of the output inverter is of common knowledge.

The design of the NOT-AND-EXCLUSIVE OR gate

The following transistors are chosen:

T_1 = OC 44 K

T_2 = OC 44 K

T_3 = OC 1072

Be:

$U_{\log} = -3\text{V}$

$U_{T1} = -7.5\text{V}$

$U_{T2} = +7.5\text{V}$

The design method of the OR-NOT gate formed from transistor T_2 is well known.

The design of the EXCLUSIVE OR circuit

If transistor T_1 operates as an inverter and is cut off, then the current through resistor R_2 should be sufficient for the saturation of transistor T_3.

According to the characteristics of the transistor T_3, $-I_B = 0.2$ mA is sufficient for the saturation, if $R_4 > 1$ kΩ.

Thus

$$R_2 = \frac{U_{T1}}{I_B} = \frac{-7.5\text{ V}}{-0.2\text{ mA}} = 37.5\text{ k}\Omega$$

The restriction on the value of resistor R_4 is realized if the value

$R_2 = 33$ kΩ

is chosen.

If transistor T_1 operates as an inverter, and there is "yes" level at the input x_1, then the value of resistor R_1 is restricted by the maximum base current of transistor T_1.

$$R_1 \geq \frac{U_{\log}}{I_{BM}} = \frac{-3\text{ V}}{-0.3\text{ mA}} = 10\text{ k}\Omega$$

Let the value

$$R_1 = 10 \text{ k}\Omega$$

be chosen.

If transistor T_1 operates as a follower, and there is "not" level at the input x_1, then the restriction on the collector voltage of transistor T_1:

$$U_C \geq 0$$

Transistor T_1 operating as a follower may be regarded as a short circuit in first approximation, as shown in Fig. 6.

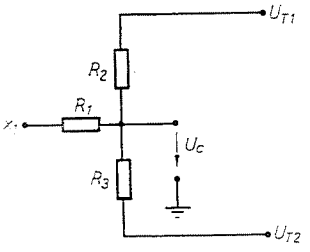

Fig. 6

If the value

$$R_3 = 27 \text{ k}\Omega$$

is chosen, the restriction (9) is realized.

If transistor T_1 operates as a follower and there is "yes" level at the input x_1, then U_C be sufficient for the saturation of transistor T_3.

In that case:

$$U_c = U_{\log} \frac{R_2 \times R_3}{R_1 + R_2 \times R_3} - U_{T1} \frac{R_1 \times R_3}{R_2 + R_1 \times R_3} +$$

$$+ U_{T2} \frac{R_1 \times R_2}{R_3 + R_1 \times R_2} = -1.5 \text{ V}$$

The internal resistance:

$$R_b = R_1 \times R_2 \times R_3 = 6 \text{ k}\Omega$$

Thus the base current of transistor T_3:

$$I_B = \frac{-1.5 \text{ V} - U_{BE}}{6 \text{ k}\Omega} \approx \frac{-1.5 \text{ V} + 0.2 \text{ V}}{6 \text{ k}\Omega} = -0.217 \text{ mA}$$

And this is sufficient to saturate transistor T_3, if $R_4 > 1 \text{ k}\Omega$.

The design of the output inverter:

The value of resistor R_4 is chosen under the condition that the NOT-AND-EXCLUSIVE OR gates can be connected into cascade.

If transistor T_1 operates as an inverter and is in saturation:

$$R_4 + R_1 = \frac{U_{T1}}{I_{BM}} = \frac{-7.5\ \mathrm{V}}{-0.3\ \mathrm{mA}} = 25\ \mathrm{k}\Omega$$

Thus

$R_4 = 15\ \mathrm{k}\Omega$.

If transistor T_1 operates as a follower and transistor T_3 of the previous stage is cut off:

$$U_C = \frac{U_{T1}R_3 + U_{T2}R_2 \times (R_1 + R_4)}{R_3 + R_2 \times (R_1 + R_4)} = -2.33\ \mathrm{V}$$

$$R_5 = (R_1 + R_4) \times R_2 \times R_3 = 9.35\ \mathrm{k}\Omega$$

Thus the base current of transistor T_3 is:

$$I_B = \frac{-2.33\ \mathrm{V} - U_{BE}}{9.35\ \mathrm{k}\Omega} \approx \frac{-2.33\ \mathrm{V} + 0.2\ \mathrm{V}}{9.35\ \mathrm{k}\Omega} = -0.277\ \mathrm{mA}$$

And this is sufficient to saturate transistor T_3, because $R_4 > 1\ \mathrm{k}\Omega$. So the value of resistor R_4 may be:

$R_4 = 15\ \mathrm{k}\Omega$

Summary

This paper reports on a new circuit realizing the NOT-AND-EXCLUSIVE OR gate. The relatively economical solution was obtained by the multiple exploitation of the transistors.

References

1. Reed, I. S.: A class of multiple-error-correcting codes and the decoding scheme. Trans. Inst. Radio Engrs IT-4 38—49 (1954).
2. Muller, D. E.: Metric properties of Boolean algebra and their application to switching circuits. Univ. of III., Digital Computer Lab., Internal Report No. 43, 1953.
3. Muller, D. E.: Applications of Boolean algebra to switching circuits design and error detection. Trans. Inst. Radio Engrs EC-3 6—12 (1954).
4. Cohn, M.: Inconsistent canonical forms of switching functions. Trans. on Electronic Computers 284—285 (1962).

László Csanky, Budapest XI., Műegyetem rkp. 9. Hungary.