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RESEARCH ARTICLE

DLF control for high efficiency grid connected PV converters

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Abstract

Nowadays there are several grid connected converters in the grid system. These grid connected converters are generally the converters of renewable energy sources, industrial four quadrant drives and other converters with DC link. These converters are connected to the grid through a three phase bridge. The standards prescribe the maximal harmonic emission which could be easily limited with high switching frequency. The high switching losses can be reduced to the half with the utilization of the well-known Flat-top modulation. The suggested DC Link Floating (DLF) control method is an extension of the Flat-top modulation with which the switching losses could be further reduced.

Keywords

Photovoltaic converter · renewable energy · DC link floating

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1 Introduction

The improvement of power semiconductors and signal processors led to the new generation of power converters and control strategies. During the last years depending on grid connected converter types there were some hardware [1]-[4] solutions developed for increasing the efficiency. The energy, especially the renewable energy, is quite expensive yet, so the efficiency is one of the most critical parameters of a grid connected system. One possible method to increase the efficiency is reducing the switching losses. At high power grid connected PV converters the most frequent main circuit arrangement is the three phase bridge [5][6]. In the new converters the developers do everything to reduce the switching losses of the semiconductors. The main circuit is usually unchanged hence the changing cost is quite high. However, with a well designed software solution on the same power circuit arrangement it is possible to reduce the switching losses with up to 75%. Further critical points are the harmonic emission and power factor correction. In this point of view there are two different types of converters. When the harmonic emission is under the limit but the current waveform is not sinusoidal the converter is called “grid-care”. In the opposite case when the waveform is also sinusoidal it is called “grid-friend” converter [7][8]. In many countries the transformer is mandatory between the converter and the grid to avoid DC current injection and to establish galvanic isolation. When a transformer is used for galvanic isolation, we can freely set the common mode voltage of the converter. In this case the efficiency can be improved by flat-top or discontinuous PWM where the switching losses can be reduced by 50%. Further improvement may be reached – especially at low power – utilizing the three state current control (3SC) as described in [9]-[14].

2 The structure of the converter

The efficiency of the newly developed DLF method was investigated on the main circuit which can be seen in Fig. 1. The main parts of the investigated converter are the PV array, which converts the solar energy to DC power, the Boost DC/DC converter raises the voltage level of the PV array to the voltage level of the three phase inverter and the three phase inverter

with filters which converts the DC power to nearly sinusoidal AC power.

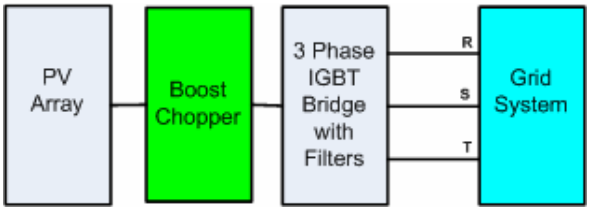

Fig. 1. Topology of the converter

The control of the boost chopper algorithm includes the maximal power point tracking method (MPPT). The high order harmonics of the output current are filtered out by common mode and differential mode passive L-C low-pass filters. The detailed main circuit arrangement can be seen in Fig. 2. The D diode is the booster diode, the $4L$ IGBT is the switch of the booster, L_b is the booster inductor, C_b is the booster capacitor and C_pv is the filter capacitor of the PV array. Due to the floating of the DC link the C_b capacitor is much smaller than the usually applied capacitance.

In Fig. 2 U_PV is the voltage of the PV array, i_b is the input current of the booster, i_dc is the DC link current, U_dc is the output voltage of the booster, i_c is the current of the booster capacitor, i_i is the input DC current of the three phase inverter and u_ga, u_gb, u_gc are the symmetrical grid voltages. Before the detailed presentation of the DLF control a short summary is given about the traditional d-q control in the next section.

3 The traditional d-q control

There are several control methods for grid connected PV converters. Most of them consist of an outer control loop for the DC voltage and an inner current control loop. The outer control loop is responsible for the constant DC link voltage. The control of the booster includes the Maximal Power Point Tracking (MPPT) method. For the inner current control loops we use the grid voltage oriented current control. This control structure is very similar to the field oriented control (FOC) of AC machines. The controllers work here also in a rotating frame, but this rotating frame is connected to the grid voltage vector, so we may name this control system as grid voltage oriented control (GVOC). The current component in the direction of the grid voltage vector is named as current "d" and is proportional to active power, while the orthogonal current component is named as current "q" and is proportional to reactive power. In this arrangement there is no zero order current, so it is enough to measure only two currents. The phase currents are transformed to the rotating d-q coordinate-system [2]. For the current control the currents are sampled at symmetry point(s) of PWM cycle (e.g. at the peaks of the up-down counter), so the sampled current is close to the average value for a given switching period. The reference value of the "d" current controller is coming from the outer voltage controller while the reference value of the "q" current is usually zero. The outputs of the current controllers are the voltage references in the rotating frame which should be transformed back to the stationary coordinate system. The voltage references divided by the available DC voltage results the duty cycles for each phase. Because our main circuit has a transformer we have freedom to choose the common mode voltage of the converter. Many modulation techniques are used in the practice from which the "Flat-top" modulation is presented in this paper. The DLF control is based on the Flat-top modulation which will be presented in details in Section 4.

4 The suggested control method

The developed inverter control has to satisfy two groups of requirements. On one hand the DC source energy should be feedback to the AC network with an efficiency as high as possible. On the other hand the prescriptions of the standards must be fullfilled for the utility compatibility. According to the standards, the AC currents should be nearly sinusoidal, and the power factor should be greater than 0.95. By reduction of switching losses with the proposed method we may increase the efficiency while maintaining the limitations of standards. In case of PV converters the efficiency can be calculated as the weighted average of efficiencies measured at the 10%, 20%, 30%, 50% and 90% of nominal power [7]. Our method is based on the Flat-top modulation therefore in the followings a brief summary is given about it. The main aim of this modulation type is to decrease the switching losses of the inverter. The switching losses are nearly proportional to the switched voltage, the switched current and the switching frequency. The switched voltage is defined by the DC voltage, which should be controlled to the possible minimal value to minimize the switching losses. We still have the multiplicand of the switched current and switching frequency. With other words we should avoid switching in a phase as much as possible, when the current in that phase is large. For the grid-connected inverters the power-factor is close to one (should be above 0.95), so the curve of the phase voltage is nearly proportional to the curve of the current. As a result we avoid switching in the phase which has the highest voltage absolute value in the next switching period. The shape depends on the modulation depth. In Fig. 3 and in Fig. 4 the duty cycle in each phases is the switching-on time of the upper IGBTs divided by the switching period.

At the limit of modulation depth for the sinusoidal output the Park-vector amplitude of duty cycle is $1/\sqrt{3}$, hence the DC link voltage equals to peak line voltage of the grid (see Fig. 3).

Under the sinusoidal limit the shapes look according to Fig. 4.

With the Flat-top modulation the switching losses could be reduced by nearly 50% (see Section 4). A drawback arises with small modulation depth, hence in that case the spectra of the common-mode voltage is pretty wide, which could result complicated and expensive EMI filters. However, this operation mode is not used in a well-designed photovoltaic converter. In the followings the description of the DLF control method is presented.

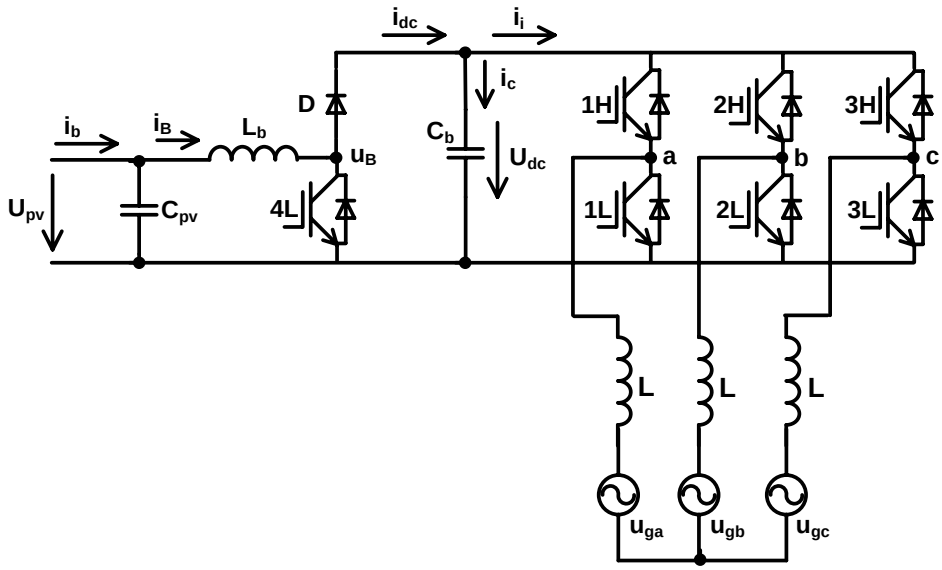

Fig. 2. The detailed main circuit

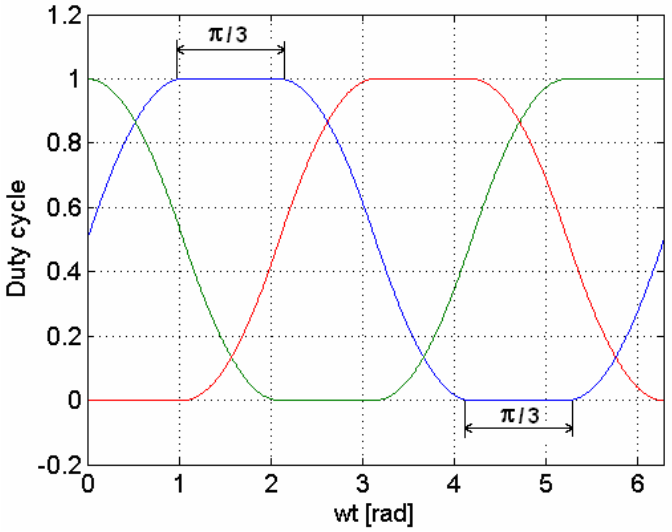

Fig. 3. Flat-top PWM, 100% modulation depth

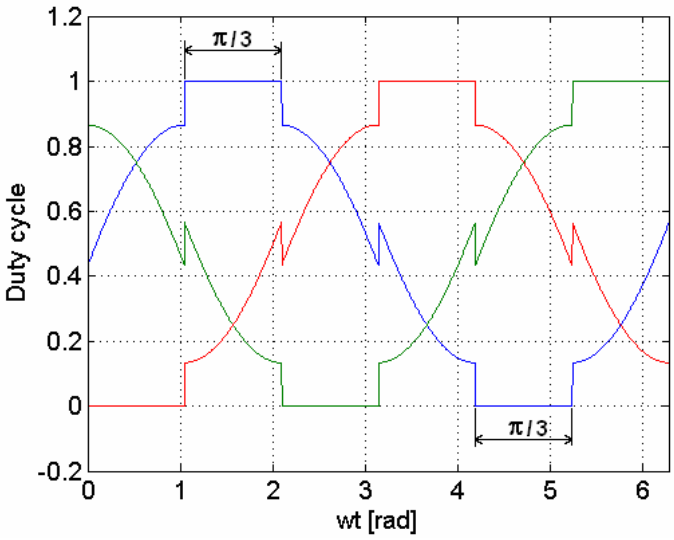

Fig. 4. Flat-top PWM, 90% modulation depth

4.1 The base idea

The DLF method tries to reduce the switching losses with the floating of the DC link voltage. The available voltage vectors of a voltage source inverter can be seen in Fig. 5 when the DC link voltage is constant. The arrows represent the available voltage vectors the curve (U_1) is the locus of the maximal base harmonic sinusoidal output voltage vector while the dotted hexagon is the available output voltage vector path with the weighting of the voltage vectors.

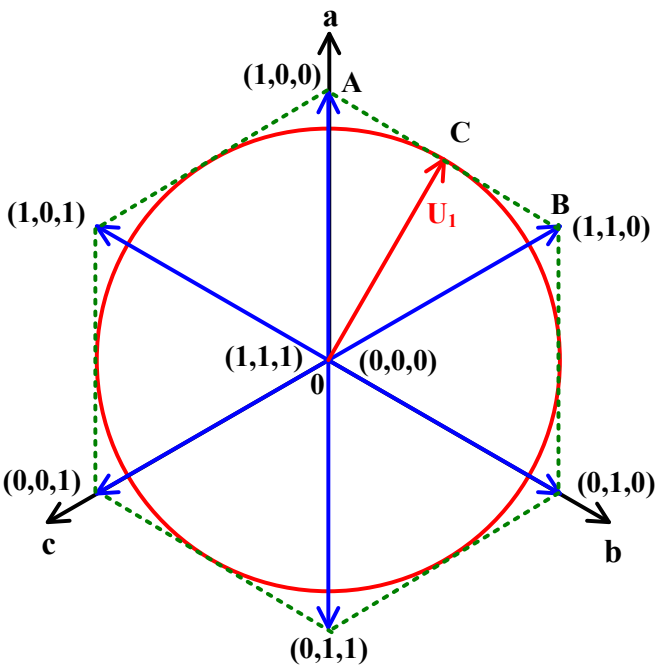

Fig. 5. Voltage vectors in case of constant DC link voltage

Let us assume that the DC link voltage is constant and the output voltage vector is inside the triangle bounded by points 0, A and B. In this section the output voltage can be created with the weighting of vectors (1,0,0), (1,0,1) and (1,1,1) or (0,0,0). If the U_1 output voltage vector is on the A-B line then only the IG-

BTs of the third leg have to be switched in which the current is almost zero, so from point of view of switching losses it is better than the traditional Flat-top modulation. Assuming constant DC link voltage and sinusoidal modulation point C has this advantage, as well. With the changing of the DC link voltage this positive properties of point C can be extended. Around point C with small DC link voltage change the U_1 output voltage vector can be kept on section A-B.

If we could modulate the DC link voltage in order that it approaches the base harmonic inverter output voltage in a big amount of the grid period, the switching losses would be much smaller than with the standard control methods. The DLF method uses such the aforementioned floating. In the next section the implementation of the DLF control and the switching losses are investigated in details.

4.2 The modulation method

In point A the magnitude of the inverter output voltage vector is higher with 13.4% than the magnitude of the output voltage vector in point C. If we modulate the DC link voltage in this point, the 13.4% voltage change would be able to remove the PV array from its maximal power point (MPP). We estimated that 6% voltage change (it is about 30V in case of European 400V grids) is small enough to keep the PV array in MPP. With 6% DC link modulation the non switching area will be longer with α_1, which angle can be calculated as follows:

$$\alpha_1 = \arccos(1 - 0.06) \approx \frac{\pi}{9}, i.e. 20^\circ \tag{1}$$

In the next step the switching losses are estimated in case of sinusoidal, Flat-top and Flat-top-DLF hybrid modulation. It is assumed that the switching losses are proportional to the switched current at constant switching frequency. Furthermore it is assumed that the switching losses are symmetrical during the grid period, so the switching losses are estimated for the one fourth of the grid period. In the next step we will introduce the relative switching loss for some modulation methods.

The relative switching loss (P_{sw}) of the sinusoidal modulation can be calculated as follows:

$$P_{\mathrm{sw}} = \int_0^{\pi/2} \sin(\omega t)\,\mathrm{d}\omega t = [-\cos(\omega t)]_0^{\pi/2} = 1. \tag{2}$$

In Eq. (2) it is assumed that the IGBTs are switched in the whole of the grid period.

In case of Flap-top modulation the IGBTs are not switched in that $\pi/3$ part of the grid period where the phase current is maximal. In this case the switching losses are:

$$P_{\mathrm{sw}} = \int_0^{\pi/3} \sin(\omega t)\,\mathrm{d}\omega t = [-\cos(\omega t)]_0^{\pi/3} = 0.5. \tag{3}$$

From Eq. (3) it is seen that with Flat-top modulation the half of the switching losses can be saved.

With the Flat-top-DLF hybrid modulation the aforementioned $\pi/3$ area is extended with a $\pi/9$ non switching area, so the switching losses can be calculated as follows:

$$P_{\mathrm{sw}} = \int_0^{\frac{\pi}{3}-\frac{\pi}{9}} \sin(\omega t)\,\mathrm{d}\omega t = [-\cos(\omega t)]_0^{\frac{\pi}{3}-\frac{\pi}{9}} = 0.23. \tag{4}$$

With this modulation technique compared to the Flat-top modulation about further 50% switching loss decrease can be reached.

4.3 The converter control

There are two possible methods to control the converter.

In the first case the booster tries to keep the PV array in the maximal power point and the inverter floats the DC link voltage. When the switching frequency of the booster is high enough, then the current of the L_{b} inductor will be nearly constant. In this case the value of the DC link current (see i_{dc}in Fig. 2) depends only on the DC link voltage and the power. Assuming lossless booster the following equation is valid:

$$U_{\mathrm{PV}} i_{\mathrm{b}} = U_{\mathrm{dc}} i_{\mathrm{dc}}. \tag{5}$$

From Eq. (5) the DC link current can be calculated as follows:

$$i_{\mathrm{dc}} = \frac{U_{\mathrm{PV}} i_{\mathrm{b}}}{U_{\mathrm{dc}}}. \tag{6}$$

If the inverter floats the DC link voltage with about 6% of nominal voltage and the current of the booster inductor and the voltage of the PV array is nearly constant, then from Eq. (6) it is seen that the DC current should be also changed with 6% of the nominal current. Due to the six-side symmetry there will be an about 6% of nominal current 5^{th} and 7^{th} order current harmonics on the AC side. In case of PV converters the standard prescribes that the maximal total harmonic distortion (THD) of the grid current has to be less than 5% of the nominal current. If the converter floats the DC link voltage the THD of the current is unsupportable.

In the second case the booster floats the DC link voltage. The floating only in that case works properly when the capacitor of the PV array (C_{pv}) is much greater than the booster capacitor (C_{b}). In the standard control strategy the booster controls the MPP and the inverter tries to control nearly constant DC voltage. In case of Flat-top-DLF hybrid modulation the booster controls the current in the inverter legs in which the current is maximal, while the current of the third leg is controlled by the inverter. We observe that in the third phase in this area the current reference otherwise is almost zero.

In case of DLF modulation the DC link voltage changes which affect on the booster inductor current which will also change. Due to the current ripple of the booster inductor the voltage of the C_{PV} capacitor will also change. However, with the proper calculation of the C_{PV}capacitor the voltage change will not affect on the Maximal Power Point of the PV array. We assume that with the 6% floating of the DC link the loss due to the floating in the MPP is less than the saved switching losses on the inverter side.

4.4 Possible modulation techniques

There are three modulation modes which can be used in this case.

- Standard Flat-top modulation, half of the switching losses can be saved.
- Flat-top-DLF hybrid modulation (in the third leg there is not special modulation). Further 25% of the switching losses can be saved.
- Flat-top-DLF-3SC hybrid modulation. The aforementioned hybrid modulation is completed with 3SC modulation in the 3^{rd} leg. The 3SC (three state current control) is a special method for increasing efficiency which tries to decrease the switching losses with the utilization of discontinuous current mode [9]-[14].

The DC link floating can also be used in the maximal power point tracking methods, however, due to the relatively high floating frequency (about 300Hz) the MPP sensors have to have good dynamic properties.

5 The mathematical model

In this section the mathematical description of DLF modulation technique is presented.

The available voltage vectors and the control sections of the DLF method can be seen in Fig. 6, where the curve is the maximal sinusoidal base harmonic voltage vector (U_1), the vectors are the available output voltage vectors and the dotted curve is the available output voltage with the weighting of the voltage vectors. In case of DLF control the first section (from point A to point B) is divided into further three subsections.

Subsections I and III represent the DLF non switching area (see Fig. 6) while in subsection II the standard Flat-top modulation is used.

In the followings the applicable modulation technique is investigated in each control sections. In first step let us assume that the DC link voltage (U_{dc}) is constant. In this case the maximal sinusoidal base harmonic voltage amplitude is the following:

$$\left|\overline{U}_{\max}\right| = \frac{U_{\mathrm{dc}}}{\sqrt{3}} \frac{1}{\cos\rho}, \tag{7}$$

where ρ is the actual angle of the grid voltage, which is measured from the beginning of subsection I (Fig. 6).

When the base harmonic voltage is constant then the DC voltage can be calculated as follows:

$$U_{\mathrm{dc}} = \sqrt{3} U_1 \cos\rho. \tag{8}$$

In the next step let us investigate that what kind of DC link voltage would be the best in each of the subsections.

The determined DC link voltage can be seen in Fig. 7. Curves I and III are joined through curve II with continuous gradient.

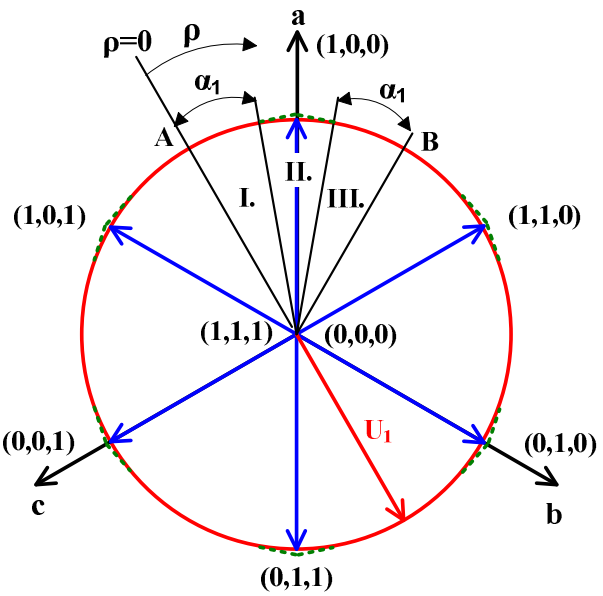

Fig. 6. Voltage vectors in DLF

In subsection I the DC voltage reference (U_{dcref}) should be the followings:

$$U_{\mathrm{dcref}} = \sqrt{3} U_1 \cos\rho. \tag{9}$$

In subsection III the voltage reference is similar to the voltage reference in subsection I and can be calculated as follows:

$$U_{\mathrm{dcref}} = \sqrt{3} U_1 \cos\left(\rho - \frac{\pi}{3}\right). \tag{10}$$

In section II a DC voltage reference curve has to be fitted to Eq. (9) and Eq. (10). The parametric form of fitting reference curve is the following:

$$U_{\mathrm{dcref}} = A - B\cos\left(\rho - \frac{\pi}{6}\right). \tag{11}$$

The parameters can be determined from the following conditions:

- The voltage reference curve at α_1 has to be equal to Eq. (9) and Eq. (10) at $\pi/3$-α_1.
  - The change of rate of the voltage reference curve at α_1 has to be equal to the rate of change of (9) and (10) at $\pi/3$-α_1.

From the aforementioned conditions and from Eq. (11) the parameters can be determined with the following expression:

$$\begin{aligned} A &= \sqrt{3} U_1 \left(\cos\alpha_1 - \frac{\cos\left(\alpha_1 - \frac{\pi}{6}\right)\sin\alpha_1}{\sin\left(\alpha_1 - \frac{\pi}{6}\right)}\right) \\ B &= -\frac{\sqrt{3} U_1 \sin\alpha_1}{\sin\left(\alpha_1 - \frac{\pi}{6}\right)} \end{aligned}. \tag{12}$$

The time function of the DC voltage reference is already known. The DC voltage is controlled by booster, so in next step the control of the booster will be investigated.

The booster capacitor current (see Fig. 2) from Eqs. (9)-(11) can be calculated as follows:

$$i_c(t) = C_B \frac{dU_{\mathrm{dcref}}(t)}{dt}. \tag{13}$$

Assuming constant power generation on the inverter side the DC current supplying inverter is the following:

$$i_i(t) = \frac{P}{U_{\text{dcref}}(t)}, \tag{14}$$

where P is the power transferred into the grid.

The booster output current (i_{dc}) is the sum of Eqs. (13) and (14):

$$i_{\text{dc}}(t) = \frac{P}{U_{\text{dcref}}(t)} + C_B \frac{dU_{\text{dcref}}(t)}{dt}. \tag{15}$$

The u_{B} potential between the D diode and IGBT 4L (see Fig. 2) is the following:

$$u_B = (1-d)U_{\text{dcref}}(t), \tag{16}$$

where d is the duty cycle of IGBT 4L. Assuming lossless booster the input side and output side power have to be equal, so the current of the booster inductance (L_{b}) can be calculated as follows:

$$i_B = \frac{1}{1-d} i_{\text{dc}}(t). \tag{17}$$

The voltage of the booster inductance can be calculated as follows:

$$U_{\text{PV}} - U_B = i_B R_B + L\frac{di_B}{dt}, \tag{18}$$

where R_{B} is the resistance of the booster inductor. From Eqs. (16-18) the rate of change of the booster inductance's current can be calculated as follows:

$$\frac{di_B}{dt} = \frac{1}{L_B}\left(U_{\text{PV}} - \frac{i_{\text{dc}} U_{\text{dcref}}}{i_B} - i_B R_B\right). \tag{19}$$

The efficiency of the DLF control was verified with some simulations. Depending on the booster inductance there are two different control methods of the booster. If the booster inductance is high and the stored energy of the inductance is not negligible then the DC link voltage reference has to be pre-calculated offline for each one sixth grid period according to Eq. (19). In the other case the stored energy of the booster inductor is negligible and the traditional cascade voltage control structure can be used with inner current control. In the simulation the second case is assumed. The results are presented in the next section.

6 Simulation results

In this section simulation results are given to verify the effectiveness of the Flat-top-DLF control method. In the simulation the following conditions were used. The voltage of the PV array is 400V, the voltage of the DC link without floating is 565V, the C_{PV} capacitance is 1000μF, the C_{B} booster capacitance is 100uF, the booster inductance is 5mH, the resistance of the booster inductance is 10mΩ, the switching frequency is 16,5kHz and the transferred power into the grid is constant 7kW.

In Fig. 8 the simulation results of the traditional Flat-top modulation can be seen for $d = 1/\sqrt{3}$.

In Fig. 8a i_{r}, i_{s}, i_{t} are the sinusoidal grid currents, in Fig. 8b *d_Booster* is the duty cycle of the booster transistor which is nearly constant, in Fig. 8c *iB_ref* is the reference for the booster current and *i_B_L* is the booster current, in Fig. 8d *udcreference* is the constant reference for the DC voltage controller and *u_B_out* is the DC link voltage and in Fig. 8e $d1$, $d2$ and $d3$ are the duty cycles of the inverter. From Fig. 8e it seems that Flat-top modulation is used on the inverter side.

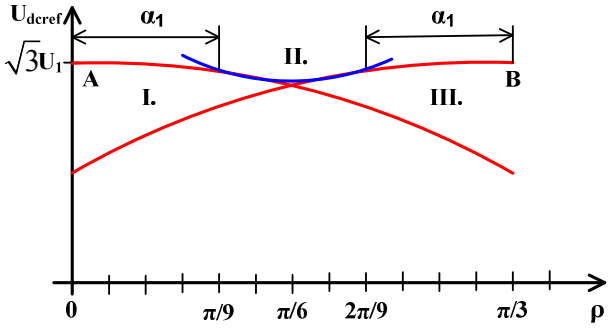

Fig. 7. DC voltage in the DLF subsections

It is seen that in case of Flat-top modulation the DC link voltage is constant and the IGBTs are not switched in that $\pi/3$ period where the grid current is almost maximal. In this simulation the standard control was used namely the inverter controls the DC link voltage to constant and the booster controls the MPP of the PV array.

In the next step instead of Flat-top modulation DLF-Flat-top hybrid modulation is used on the inverter side. The simulation results can be seen in Fig. 9.

In Fig. 9a i_{r}, i_{s}, i_{t} are the sinusoidal grid currents. In this case the DC link voltage is changing and assuming constant power the inverter current also has to be changed according to the voltage reference. In Fig. 8b *d_Booster* is the duty cycle of the booster transistor which is also changing according to the voltage reference. In Fig. 8c *iB_ref* is the reference for the booster current and *i_B_L* is the booster current. The booster current also changes according to the voltage reference. In Fig 8d *udcreference* is the reference for the DC voltage controller according to chapter 5 and *u_B_out* is the DC link voltage. Finally in Fig. 8e $d1$, $d2$ and $d3$ are the duty cycles of the inverter. From Fig. 9e it seems that DLF-Flat-top modulation is used on the inverter side.

The IGBT's non switching area is extended to about 100° of the grid period. In the non switching area the grid voltage and the grid current is almost maximal, so the switching losses were reduced to 25% compared to the traditional modulation.

7 Conclusion

With the newly developed DC link floating control we could make a high efficiency and reliable PV converter which satisfy the prescriptions and limitations of the standards. The DLF control was verified with some simulation and it worked correctly in the whole load range. Our future plan is to complete and verify the DFL method with the auxiliary DLF-3SC control with which we could further increase the efficiency.

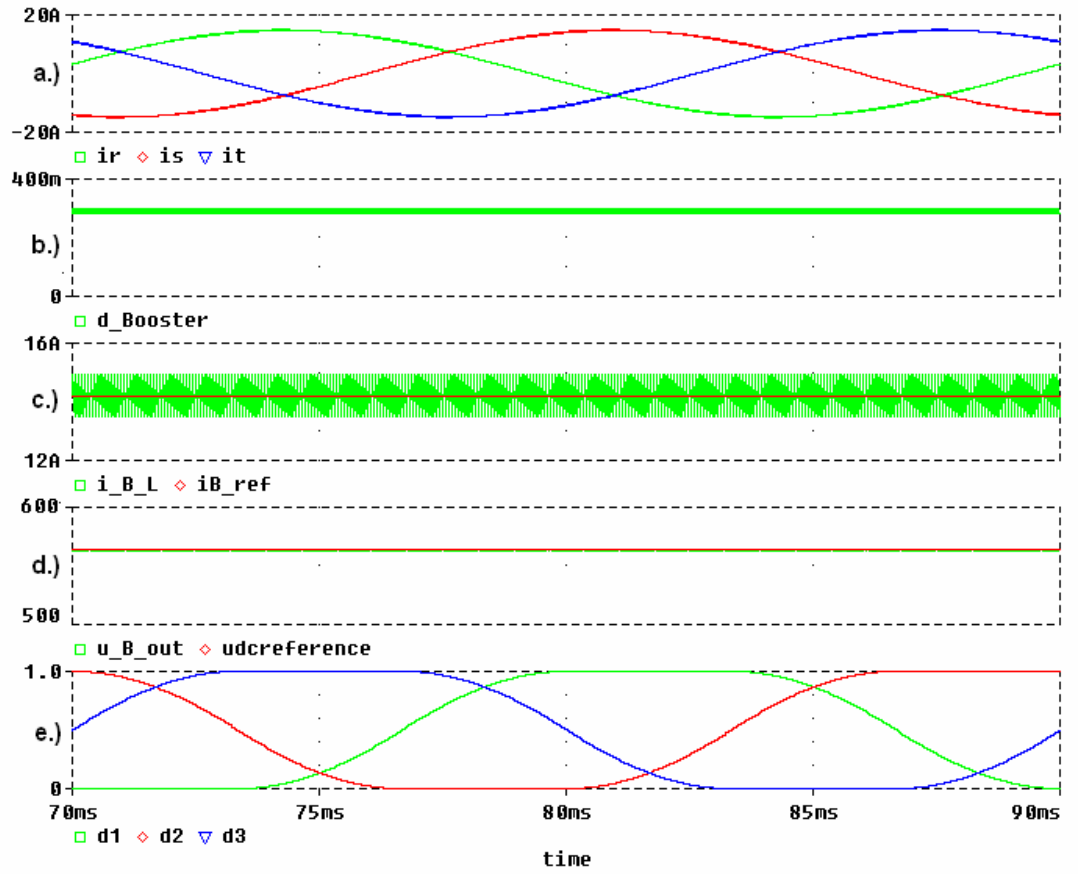

Fig. 8. Simulation results (Flat-top)

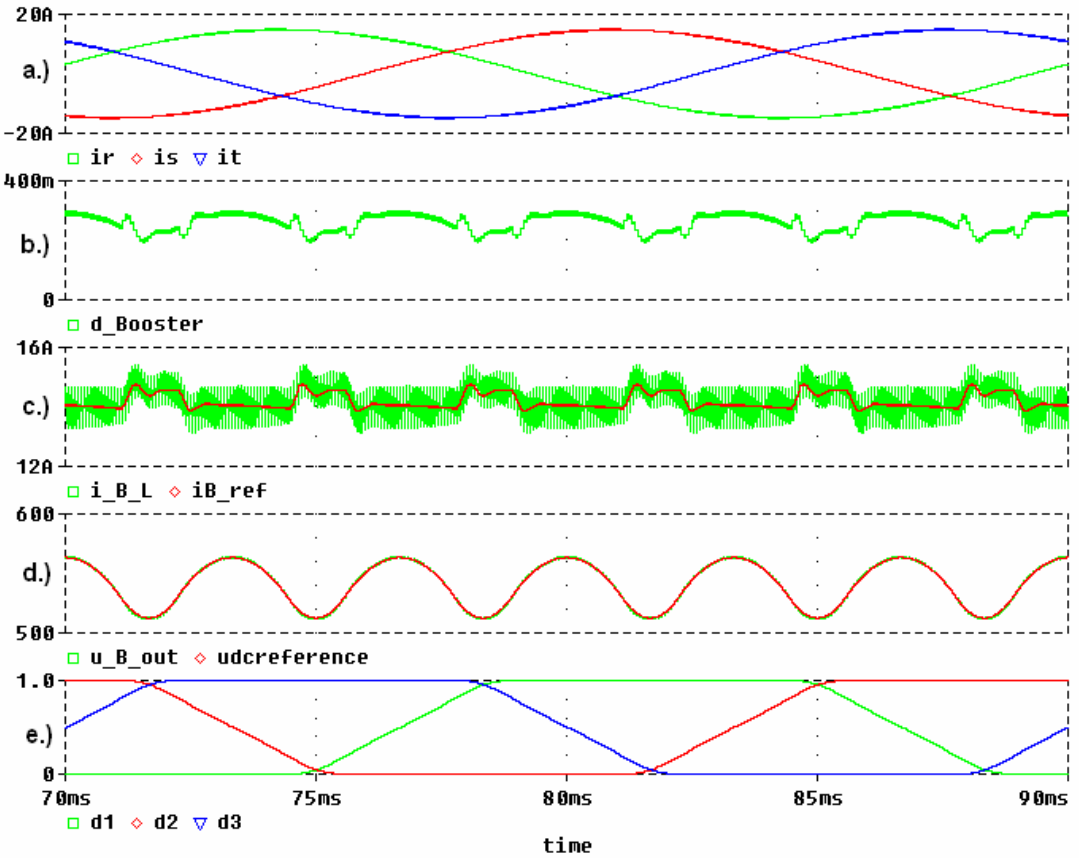

Fig. 9. Simulation results (DLF)

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