Periodica Polytechnica
Electrical Engineering
and Computer Science

61(3), pp. 264-271, 2017
https://doi.org/10.3311/PPee.10902

Design of HIL for Multi-Level Inverter Using Zynq-7000 Platform – Part 1

Balázs Farkas[1*], Károly Veszprémi[1]

RESEARCH ARTICLE

Received 18 April 2017; accepted after revision 25 May 2017

Abstract

Development of power electronic devices requires multi -disciplined engineering activities. These cover the thermal, electrical and software design. Due to this design complexity rapid prototyping methods and model-based design are becoming more and more important in the R&D projects in this field. In case of the multi-level inverter based drives the strict reliability requirements make the aforementioned new approaches more attractive. This article is the first part of the series which introduces the application of the model based design and Hardware-in-the-Loop (HIL) tools through the modeling of a Cellular H-Bridge inverter (CHB). This article focuses on the power electronic system modeling and verification. The model of the CHB is implemented and verified in Matlab.

Keywords

Multi-level inverter, Zynq-7000, Hardware in the loop, CHB

[1]Department of Electric Power Engineering,
Faculty of Electrical Engineering and Informatics,
Budapest University of Technology and Economics,
H-1111 Budapest, Egry J. utca 18, Hungary

*Corresponding author, e-mail: balazs.farkas86@gmail.com

1 Introduction

Nowadays the high extent of market competition and strict standard requirements imply that the power electronic products are continuously becoming more and more complex. The design of a competitive inverter has to simultaneously meet the time-to-market, economic, efficiency, reliability and the technical standards related requirements. Meeting this versatile set of requirements and constrains seems to be a challenge for the researchers and developers who are responsible for the product development [1].

High performance modeling tools [2] and model based design paradigm can help engineers to overcome the aforementioned product complexity [3]. Rapid prototype methods [4] can extend the performance of the model based design at high extent [5-7]. To demonstrate the performance of these tools, a HIL based model of a five-level CHB inverter is developed and tested in this article series. This demonstration project can be divided into 4 subprojects. The starting point is the modeling of power electronics. The second one is the implementation of the communication interface between the hardware and the host PC of developers. The third one is the development of DAQ and monitoring system, since the efficiency of the development highly depends on the observability of the system. The last one covers the creation of the tool chain, which makes model transformation easier.

The aim of this article is to introduce the model development, which makes hardware co-simulation possible. The accuracy of the model and the effect of the model transformation were verified by simulation. During the verification the behavior of a fixed point model was compared to the SimPower System based reference model.

The article consists of three main sections. The first section introduces the applied workflow and design procedure. In the next section the details of CHB model are analysed. In the last section the implemented fixed point model is simulated and verified in Simulink.

2 Workflow of the Model Based Development

This part of the article deal with the model based workflow. There are generally three critical aspects of the development projects. The first one is related to system decomposition, the second one is connected to the model behavior, transformation and verification. The last one covers any problem regarding the uncertainties during the development.

Fig. 1 describes the main design stages from the system decomposition point of view. This procedure is intended to handle the relevant consequences of the system complexity. It is practically based on the V-Model, which includes the development process of Simulink model and HW as well.

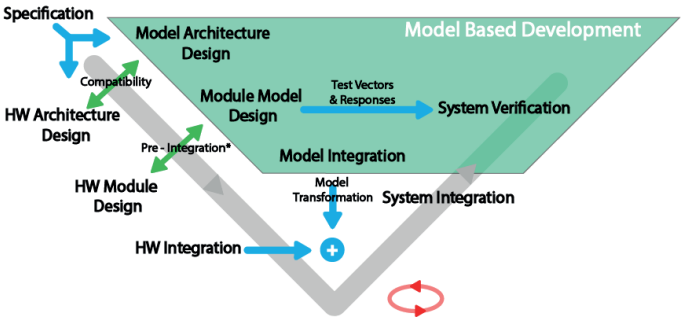

Fig. 1 Development process of the model and hardware in the V-model.

Apart from these phases it is important to see that the model evolution has got three maturity levels. They are the development of the reference model based on the Matlab SimPower System, floating point model and the fixed point model. The biggest advantage of the workflow is the automatic transformation not only of the model but also of the test data set. Due to this fact, the implementation activity in the fixed point model development is not theoretically required. As a result of this, the required amount of the developing works can be drastically reduced. In any maturity levels, three main development phases can be identified: design, implementation and verification, as it can be seen in Fig. 2.

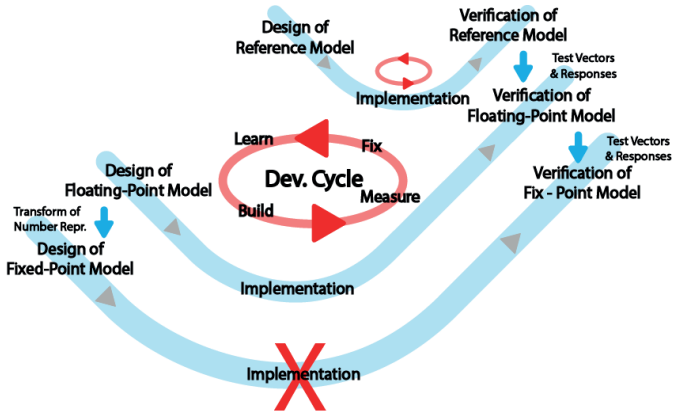

Fig. 2 Main stages of the Model based development in Matlab.

Aforementioned phases can be applicable from a module development up to system integration. During the design, the interfaces, architecture and model behavior are considered. In the implementation phase the model is created or improved. All activities in the last phase belong to the verification process. It covers not only the investigation of the system response but the test vector generation and improvement as well.

Since the developers are likely to face these unexpected events during their work, it is not worth trying to manage the development as if it could be deterministic. In case of Fig. 1, the red circle symbolizes the continuous integration concept, which means that the complexity of the system should be increased only by small increments. As a consequence of this, the V-Model developing path has to be followed by several times.

The second part of Fig. 2 with red color symbolizes the learning cycle regarding the model development. The four main stages in this cycle are building, measuring, fixing and learning. This concept is based on the hypothesis that the success of the development project strongly depends on the learning curve of the developers regarding system behavior and required technologies.

3 Modeling of CHB

CHB has got modular structure. As a consequence of this, its model has similar structure and hierarchy. Fig. 3 shows the schematic of the CHB inverter. The CHB inverter consists of two identical cells in each phase, which includes a three-phase rectifier and single-phase voltage source inverter. The control of the IGBTs in the cell is implemented by unipolar modulator, which is also part of the cells. Apart from the inverter, the motor and the transformer are the key elements of the model.

In the currently introduced model the transformer and motor are simplified. The model of transformer includes only a three-phase secondary voltage sources and leakage inductances. In addition, the phase-shifting of the transformer is not currently considered. Similarly, the motor model is also based on the leakage inductance and motor EMF.

The core elements of the model are the switching functions. These variables describe the states of semiconductors. Their values can be 1 if the semiconductor is in conduction state and 0 if it does not conduct.

3.1 Three-phase Diode-Front-End

The operation of the DFE is introduced in this section. DFE can model the behavior of the rectifier not only during normal operation but during overlap as well. The input of the rectifier is connected to the secondaries of the input transformer in CHB. Its output is connected to the DC link capacitor of the cell. From electrical point of view, the secondary stray inductances of the transformer realize current source supply. Thanks to the DC link capacitor, the output of the rectifier is coupled to a voltage source.

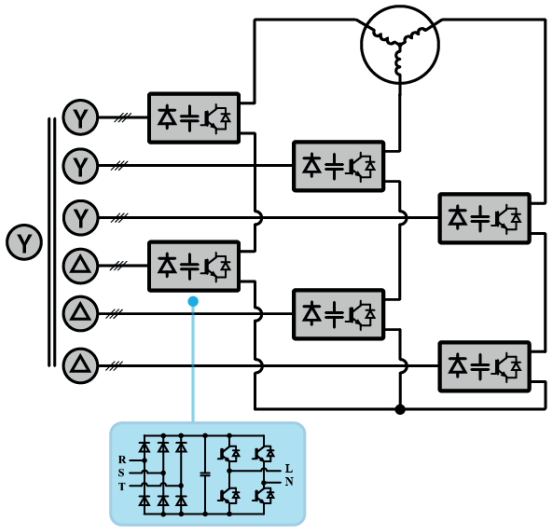

Fig. 3 Schematic of Cellular H – Bridge Inverter. There are 2 cells in each phases and the cells have three phase Diode-Front-End.

The schematic of DFE and the relevant signals are shown in Fig. 4. If there is no common mode current at grid side (1), the rectifier model has got only three state variables: the currents of the leakage inductances in R, S phases and the voltage of the DC link capacitor.

$$I_{LR} + I_{LS} + I_{LT} = 0 \tag{1}$$

For the sake of simple equation handling, circular naming terminology is used for the identification of the phase quantities. Instead of using traditional symbols like R, S, T, all equations use virtual positive order system: X, Y, Z. When any signals are intended to calculate, its equation has to be firstly derived by the following rule. The phase index of the considered variable should be substituted into X. The others should be substituted into Y and Z in the positive order.

Let's see an example: we would like to calculate any variable in S phase. In this case all X symbols in the equations should be changed to S, Y to T and Z to R.

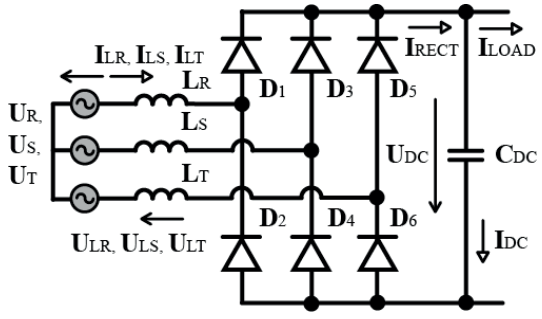

Fig. 4 Schematic of the three-phase Diode-Front-End and relevant electrical quantities with their positive direction.

The equation of the model in the form of the aforementioned virtual system is, where T_S symbolizes sample time:

$$I_{LX}[n+1] = \frac{U_{LX}[n]}{L_X} T_S + I_{LX}[n] \tag{2}$$

$$U_{DC}[n+1] = \frac{I_{DC}[n]}{C_{DC}} T_S + U_{DC}[n] \tag{3}$$

The operation of the model is introduced in Fig. 5. Depending on the active state and the input variables, the state machine calculates the value of the switching function in the n^{th} step, σ[n]. Based on the value of the switching functions, the voltages of the grid leakage inductances and the rectifier output current can be derived.

During the calculation of the switching functions the following rules are observed.

If no diode conducts, the condition for getting into the conduction state is:

- the relevant line voltage has to be maximal,
- the relevant line voltage has to be bigger than U_{DC}.
- If any diode pairs already conduct, they stay in the conduction state until:
- the phase current becomes zero or changes its sign.

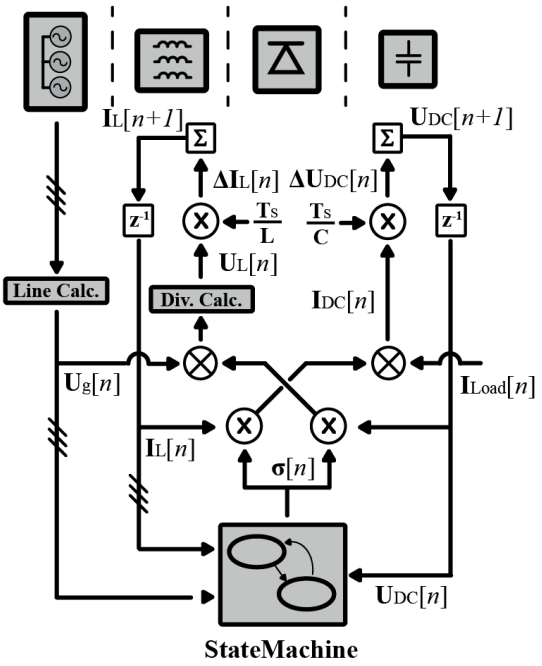

Fig. 5 Operation of the rectifier model.

In Fig. 6 the operation of the state machine is described for a subset of the states. The entry point is the OFF state. In this state none of the diodes conduct. The state machine exits from OFF state if the value of any line-line voltages become higher than the DC-link voltage. Later, OFF state can be active again if the phase currents become zero.

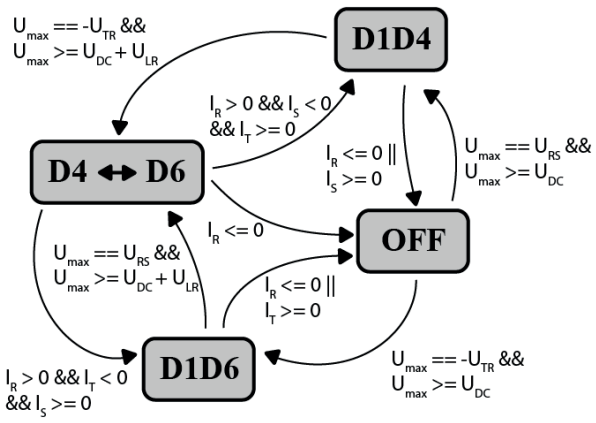

Fig. 6 Operation of the state machine in the rectifier model.

During overlap the three diodes are conducting. The commutation between diodes is initiated when the maximal line voltage is changed and the new line voltage value is higher than $U_{DC}[n]+U_{LX}[n]$. $U_{LX}[n]$ symbolizes the voltage of the stray inductance in the phase, in which the current was not zero before the commutation started. When none of the diodes is in conduction state in any phase the model forces the proper inductor current to zero. It can increase the robustness of the model. The state machine is implemented by Stateflow.

As a consequence of the fact that the interconnection between the leakage inductances is significantly changed, different equations have to be applied for normal operation and for the operation during overlap. In Fig. 7 and Fig. 8 the simplified schematics are introduced. The current of the DC-link capacitor can be calculated by the following equation:

$$I_{DC[n]} = I_{RECT}[n] - I_{LOAD}[n] \tag{4}$$

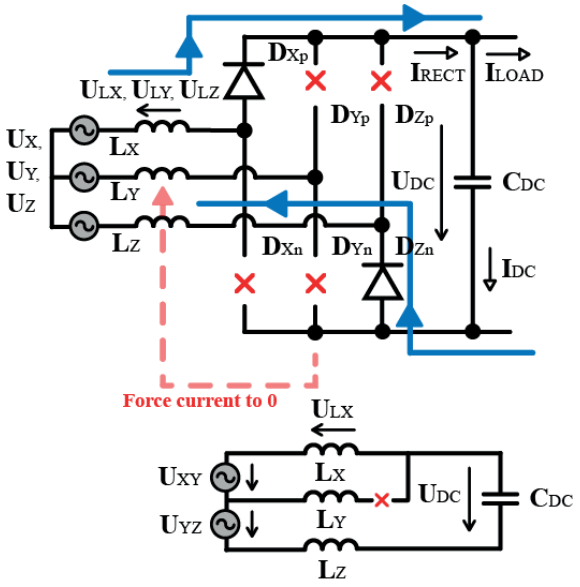

Fig. 7 Current path and simplified sch. in the normal operation mode.

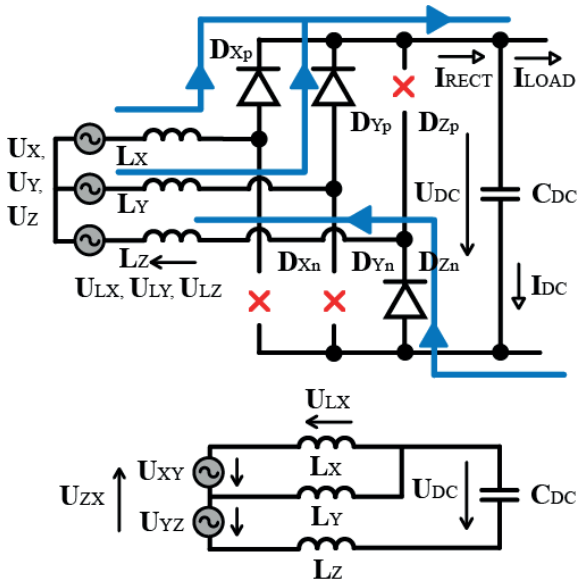

Fig. 8 Current path and simplified schematic during overlap.

If overlap is not observed the following equations define the value of $U_{LX}[n]$:

$$\xi_{DC-X1}[n] = \left[-\sigma_{Xp}\sigma_{Yn} + \sigma_{Xn}\sigma_{Yp}\right]\overline{\sigma_{Zp} + \sigma_{Zn}}\,\frac{L_X}{L_X + L_Y} \tag{5}$$

$$\xi_{DC-X2}[n] = \left[-\sigma_{Xp}\sigma_{Zn} + \sigma_{Xn}\sigma_{Zp}\right]\overline{\sigma_{Yp} + \sigma_{Yn}}\,\frac{L_X}{L_X + L_Z} \tag{6}$$

$$\xi_{XY-X}[n] = \left[\sigma_{Xp}\sigma_{Yn} + \sigma_{Xn}\sigma_{Yp}\right]\overline{\sigma_{Zp} + \sigma_{Zn}}\,\frac{L_X}{L_X + L_Y} \tag{7}$$

$$\xi_{YX-X}[n] = 0 \tag{8}$$

$$\xi_{ZX-X}[n] = -\left[\sigma_{Zp}\sigma_{Xn} + \sigma_{Zn}\sigma_{Xp}\right]\overline{\sigma_{Yp} + \sigma_{Yn}}\,\frac{L_X}{L_X + L_Z} \tag{9}$$

$$U_{LX}[n] = \left(\xi_{DC-X1} + \xi_{DC-X2}\right)U_{DC}[n] + \xi_{XY-X}\,U_{XY}[n] + \xi_{YX-X}\,U_{YX}[n] + \xi_{ZX-X}\,U_{ZX}[n] \tag{10}$$

During overlap the following equations can be used to calculate $U_{LX}[n]$:

$$\delta_{DC-X1}[n] = \left[-\sigma_{Xp}\sigma_{Yn}\sigma_{Zp} + \sigma_{Xn}\sigma_{Yp}\sigma_{Zn}\right]\frac{L_X x L_Z}{L_X x L_Z + L_Y} \tag{11}$$

$$\delta_{DC-X2}[n]=\left[-\sigma_{Xn}\sigma_{Yp}\sigma_{Zp}+\sigma_{Xp}\sigma_{Yn}\sigma_{Zn}\right]\frac{L_Y x L_Z}{L_Y x L_Z+L_X} \tag{12}$$

$$\delta_{XY-X}[n]=[\sigma_{Xp}\sigma_{Yp}\sigma_{Zn}+\sigma_{Xn}\sigma_{Yn}\sigma_{Zp}+\sigma_{Xp}\sigma_{Yn}\sigma_{Zp}+\sigma_{Xn}\sigma_{Yp}\sigma_{Zn}+\sigma_{Xn}\sigma_{Yp}\sigma_{Zp}+\sigma_{Xp}\sigma_{Yn}\sigma_{Zn}]\frac{L_X}{L_X+L_Y x L_Z} \tag{13}$$

$$\delta_{YX-X}[n]=[\sigma_{Xp}\sigma_{Yp}\sigma_{Zn}+\sigma_{Xn}\sigma_{Yn}\sigma_{Zp}+\sigma_{Xp}\sigma_{Yn}\sigma_{Zp}+\sigma_{Xn}\sigma_{Yp}\sigma_{Zn}+\sigma_{Xn}\sigma_{Yp}\sigma_{Zp}+\sigma_{Xp}\sigma_{Yn}\sigma_{Zn}]\frac{L_X x L_Y}{L_X x L_Y+L_Z} \tag{14}$$

$$\delta_{ZX-X}[n]=0 \tag{15}$$

$$U_{LX}[n]=\left(\delta_{DC-X1}+\delta_{DC-X2}\right)U_{DC}[n]+\delta_{XY-X}\,U_{XY}[n]+\delta_{YX-X}\,U_{YX}[n]+\delta_{ZX-X}\,U_{ZX}[n] \tag{16}$$

3.2 Single-Phase Inverter

Each cell includes a single-phase inverter at the motor side, Fig. 9. Because of motor leakage inductances, the inverter supply at the motor side can be considered as a current source. In case of the DC-link the supply behaves like a voltage source, as a consequence of the DC-link capacitor.

Similar to the rectifier, the core element of the single phase inverter model is also the state machine, Fig. 11. It can be decomposed into two parts. The first one controls the switching functions of the freewheeling diodes in the H-Bridge. Its behavior is determined by the motor voltage, DC link voltage and motor currents, Fig. 10. The second one can modify these switching functions based on the gate signals.

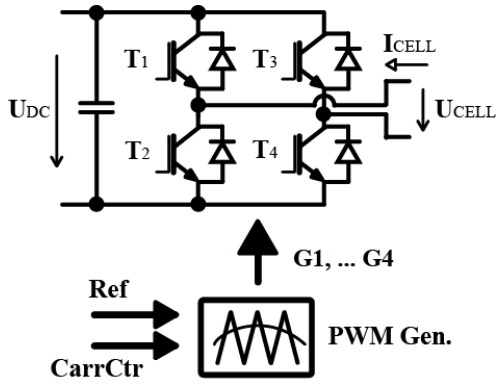

Fig. 9 Schematic of the single-phase inverter at cell output.

The switching functions of the freewheeling diodes can be calculated based on the following rules. In case of OFF state when no semiconductor is in conduction state, the condition for getting into the conduction state is:

- the motor voltage scaled to the cell level has to be higher than U_{DC}. If the motor voltage sign is positive, D_1D_4 diode pair starts to conduct, if it is negative, D_2D_3 diode pair starts conducting.
- if one of the diode pair is in conduction state, the commutation can be initiated by changing of the current sign or zero current.

After the diode conduction state is calculated, the gate signal is allowed to modify the switching functions with the following considerations:

- an IGBT can conduct only positive current
- if an IGBT is turning-on, its commutation diode pair is getting into off state, e.g. T_4 prohibits D_3.

The final values of the switching functions can be prevailed by first or second part of the state machine. This type of operation can potentially cause hazard during the current commutation between the IGBTs and freewheeling diodes. As a consequence of this fact, the turning-on of an IGBT has to simultaneously imply the activation of its freewheeling diode commutation pair. Therefore, the switching functions of the diodes are stably active, during the transient of the IGBT.

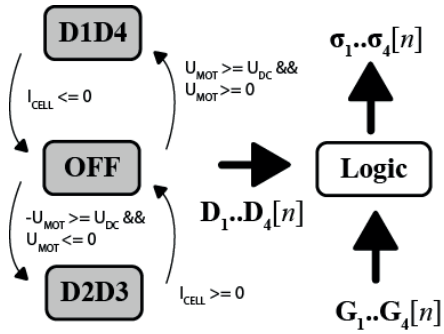

Fig. 10 Operation of the state machine in the inverter model.

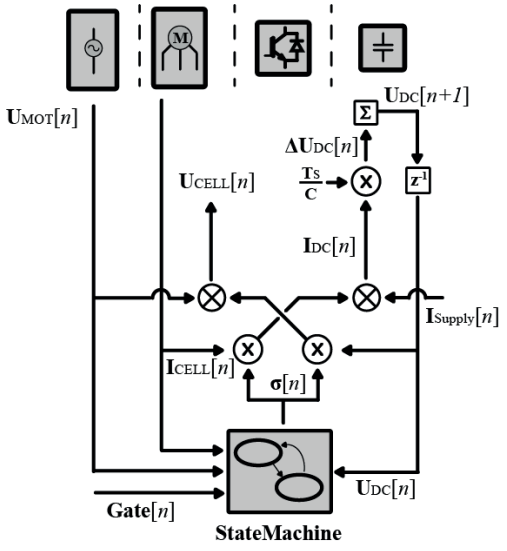

Fig. 11 Operation of the inverter model.

The gate signal of the IGBTs is generated by a modulator, Fig. 12. This modulator is the part of the cell. Thanks to the fact that the modulator is implemented in the FPGA, the resolution of the gate control does not depend on Matlab or communication speed. The modulator implements unipolar modulation, its reference signals are "refLegT1T2" and "refLegT1T2".

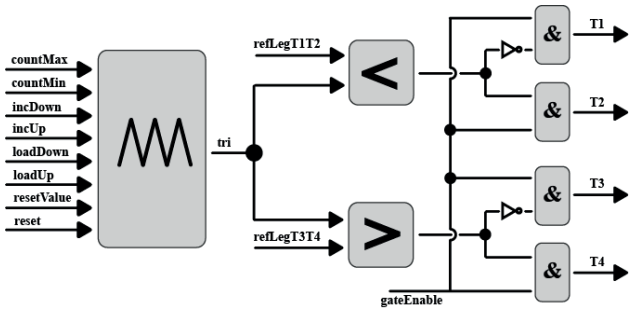

Fig. 12 Structure of the modulator in the cells.

The carrier generator has got several inputs to implement flexible design. The signal of "*countMax*" and "*countMin*" define the value of maximum and minimum of the generated triangle. The "*incDown*" and "*incUp*" define the increment and they have effect on the resolution of the generated PWM signals. The phase of the triangle can be set by "*resetValue*". It defines the value which has to be loaded into the counter during reset. The carrier generator is introduced in Fig. 13.

3.3 Cell and System

In this section the operation of two integrated models are introduced. The former is the model of the cell and the latter is the model of the drive system.

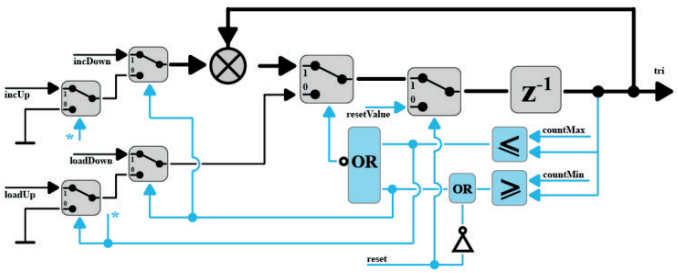

Fig. 13 Structure of the carrier generator.

In case of the cell, the model consists of rectifier, inverter and capacitor. Based on the DC-link voltage, grid currents and grid voltages, the rectifier model calculates the output current of the rectifier (I_{RECT}) in the n^{th} step. Meanwhile the inverter model determines its input current (I_{INV}). It uses the motor current, scaled motor voltage and gate signals. The current of the DC-link capacitor (I_{DC}) can be derived as the sum of the I_{RECT} and I_{INV}. By means of the equation (3) the value of the DC-link voltage can calculated for the $(n+1)^{th}$ step.

The model of the CHB firstly calculates the output voltages of the cells, by means of motor voltage, secondary voltages of the transformers, motor currents and cell reference voltages. Then the voltages at inductances of the motor should be derived (5-15) based on the cell output voltages and motor EMF. In the last stage, the currents of the motor are determined in the step of $(n+1)^{th}$ by using of the equation (2).

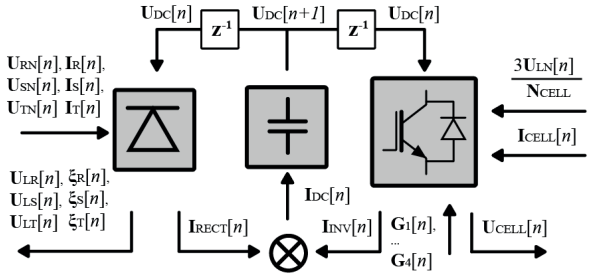

Fig. 14 Operation of the integrated cell model.

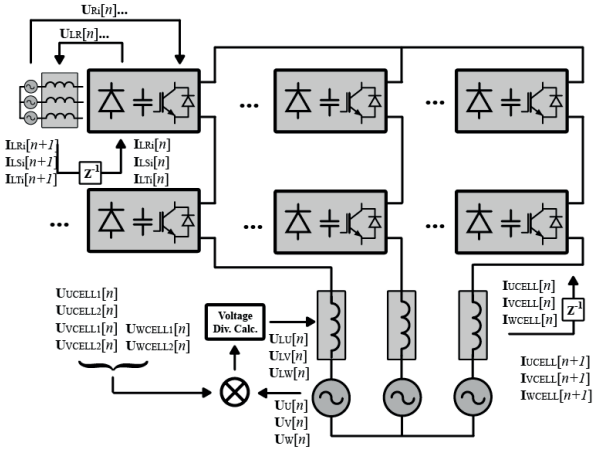

Fig. 15 Operation of the drive system.

4 Simulation Results

The accuracy and behavior of the implemented model are verified by means of the SimPower System reference model. The CHB control is open-loop, that is there is no current control loop. The cell reference signals are pre-calculated. Both models are simulated by the same parameter set in the Simulink. The configuration data is introduced in Table 1.

Table 1 Simulation Parameters

Parameter	Value
Motor Nominal Data	2.3 kV / 140 A
Grid Nominal Data (Sec.)	1.1 kV / 50 A
Motor Leakage Inductance	300 uH (1%)
Transformer Leakage Induct.	300 uH (~0.8%)
DC Link Capacitor	3 mF
Switching Frequency	3 kHz
Frequency of Motor EMF	50 Hz
Grid Frequency	50 Hz

Firstly, the relevant simulation results of the developed model are introduced. Then the signals of both models are compared. The input currents of the cell are shown in Fig. 16. The input current system is not symmetrical; it is mainly the consequence of the single phase load of the DC-link capacitors in the cells. This grid currents asymmetry is also the consequence of the fact that the frequency of the motor EMF is the same as the grid frequency.

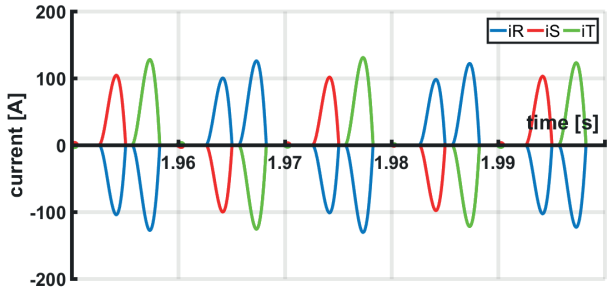

Fig. 16 Input currents of upper cell in U phase.

Fig. 17 and Fig. 18 show the motor currents. The motor leakage inductance was chosen to an unrealistic low value. Its aim was to increase the ripple of the motor current, which makes the model errors more observable.

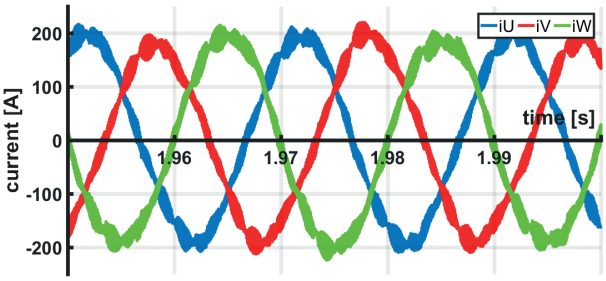

Fig. 17 Motor phase currents.

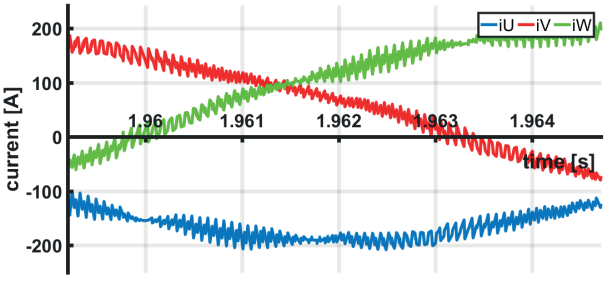

Fig. 18 Motor phase currents (enlarged)

The phase voltages of the CHB can be seen in Fig. 19. If there are N pieces of the two-level cell in each phase with symmetrical DC-link, the number of the voltage levels between the line and neutral has to be 2N + 1. The existence of five voltage levels can be observed in the figure.

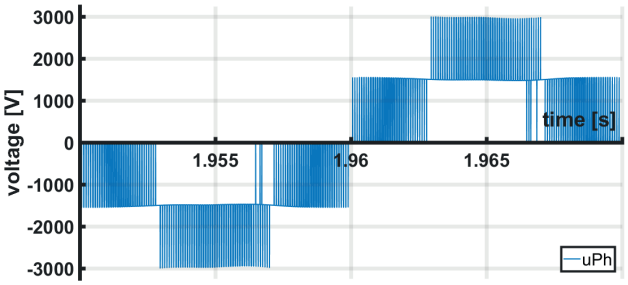

Fig. 19 U phase voltage at CHB output.

Fig. 20 describes the line voltage of the inverter. Since there are 2 cells in each phase the number of the voltage levels between line to line should be 4N + 1. It can be observed in the aforementioned figures.

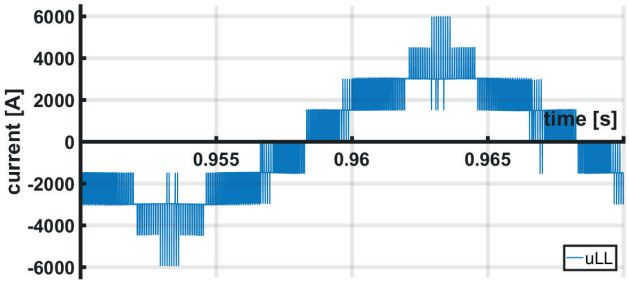

Fig. 20 U-V line voltage at CHB output.

Fig. 21 shows the DC link voltage of the cell in the U phase. The effects of the single phase load are the relative high voltage ripple and capacitor load in the DC link. The deviation between the results of the implemented and the reference model is minimal. Maximum deviation is around 10V if the average DC link voltage is roughly 1500V, it is around 0.7% error.

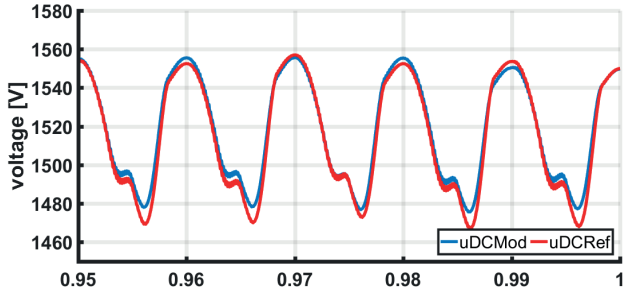

Fig. 21 DC link voltage of the upper cell in U phase.

The deviation between the developed model and the reference model is also shown in Fig. 22 and Fig. 23, or the input currents and the motor currents. In spite of the fact that the error of the DC-link voltage seems to be negligible, its effect on the motor current is significant. Its root causes are the small values of impedance.

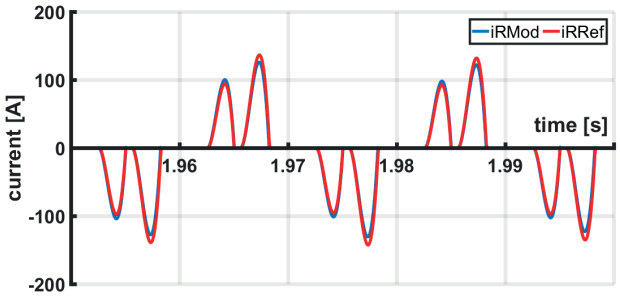

Fig. 22 Comparison of the implemented and reference model, in case of R phase Input current of the upper cell in U phase.

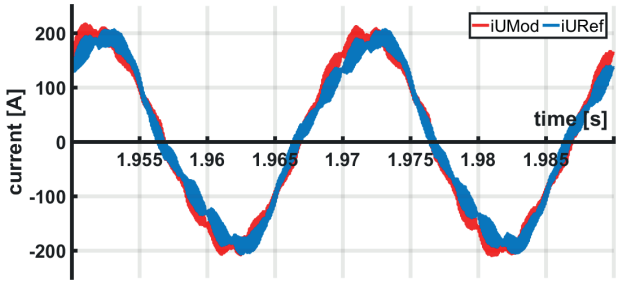

Fig. 23 Comparison of the implemented and reference model, in case of U phase motor current.

5 Conclusion

This two-part article series introduces power electronics model development and operation on the Zynq-7000 platform. The first part of the series (Part 1) focuses on the model based design workflow and development of the CHB model. The applied V-model and agile paradigm were conceptually introduced. Handling of the high risk and uncertainty from the early phase of the development is the key point of the followed workflow. In the second part, the details of the implemented model will be introduced. Each element of the model is sequentially investigated and their operation are explained. The accuracy of the model is verified by a reference model based on the SimPower System.

In the next part of this article series, the model transformation, the development of the hardware and the interfaces will be introduced. Finally, the operation of the Zynq-7000 based model will be also verified by the aforementioned reference model.

References

[1] Faruque, M. D. O., Strasser, T., Lauss, G. "Real-Time Simulation Technologies for Power Systems Design, Testing, and Analysis." *IEEE Power and Energy Technology Systems Journal*. 2(2), pp. 63-73. 2015. https://doi.org/10.1109/JPETS.2015.2427370

[2] Kökényesi, T., Varjasi, I. "Comparison of Real-Time Simulation Methods for Power Electronics Applications." In: 2013 4th International Youth Conference on Energy (IYCE), Siófok, Hungary, Jun. 6-8, 2013, pp. 1-5. https://doi.org/10.1109/IYCE.2013.6604137

[3] Matar, M. "An FPGA-Based Real-Time Simulator for the Analysis of Electromagnetic Transients in Electrical Power Systems." Phd Thesis, University of Toronto. 2009.

[4] Debreceni, T., Kökényesi, T., Sütő, Z., Varjasi, I. "FPGA-based real-time Hardware-In-the-Loop simulator of a mini solar power station." In: 2014 IEEE International Energy Conference (ENERGYCON), Cavtat, 2014, pp. 70-75. https://doi.org/10.1109/ENERGYCON.2014.6850408

[5] Li, W., Grégoire, L. A., Souvanlasy, S., Bélanger, J. "An FPGA-based real-time simulator for HIL testing of modular multilevel converter controller." In: 2014 IEEE Energy Conversion Congress and Exposition (ECCE), Pittsburgh, PA, 2014, pp. 2088-2094. https://doi.org/10.1109/ECCE.2014.6953678

[6] Matar, M., Iravani, R. "FPGA Implementation of the Power Electronic Converter Model for Real-Time Simulation of Electromagnetic Transients." *IEEE Transactions on Power Delivery*. 25(2), pp. 852–860. 2010. https://doi.org/10.1109/TPWRD.2009.2033603

[7] Ould-Bachir, T., Merdassi, A., Cense, S., Blanchette, H. F., Bélanger, J. "FPGA-based Real-Time Simulation of a PSIM Model: An Indirect Matrix Converter Case Study." In: IECON 2015 - 41st Annual Conference of the IEEE Industrial Electronics Society, Yokohama, 2015, pp. 003336-003340. https://doi.org/10.1109/IECON.2015.7392614