

Modeling of Short P-Channel Symmetric Double-Gate MOSFET for Low Power Circuit Simulation

Rekib Uddin Ahmed¹, Prabir Saha^{1*}

¹ Department of Electronics and Communication Engineering, National Institute of Technology Meghalaya, Shillong-793003, India

* Corresponding author, e-mail: sahaprabir1@gmail.com

Received: 27 April 2019, Accepted: 09 October 2019, Published online: 17 December 2019

Abstract

In the present era, down scaling of complementary metal-oxide-semiconductor (CMOS) technology has lead the metal-oxide-semiconductor field-effect-transistor's (MOSFET) sizes to nanometer regime which in turn experiencing difficulties due to the effect of physical and technological perspective. Double-gate (DG) MOSFET is considered as a promising device to reduce the shortcoming and shrink down towards nanometer domain. This paper proposes electrostatic potential distribution and drain current models for the lightly doped symmetrical p-channel DG MOSFET. The analytic solution of potential distribution is derived by solving the 2D Poisson's equation incorporated with hole density through the superposition method. The drain current model has been explored by incorporating physical effects like threshold-voltage roll-off, channel length modulation and surface roughness scattering. Functionality of the models has been calculated in MATLAB and the obtained results are verified and compared with state of the art literature.

Keywords

channel length modulation, cross-over point, drain-current, potential distribution, p-channel, subthreshold slope, threshold voltage

1 Introduction

The continued downscaling of complementary metal-oxide semiconductor (CMOS) technology is approaching its limit due to the short-channel effects (SCE) like threshold voltage roll-off, mobility degradation and degradation of subthreshold slope [1]. New MOSFET architectures: multi-gate MOSFETs which employ the use of multiple gates to prevent the deleterious SCEs in scaled transistors and hold promise to extend the scalability of CMOS technology [2]. Double-gate (DG) MOSFET is one of the multi-gate devices which can be successfully scaled down to 30 nm gate length [3]. Moreover, the device has better control over SCEs [4] which allows the silicon body to be lightly doped compared to conventional bulk MOSFETs. The dual gates and the lightly doped ultra-thin body of the device result in elimination of dopant fluctuation and mobility degradation effects [5]. The combination of light body doping and ultra-thin body also helps in steeper subthreshold swing and lower junction and body capacitance [6]. Because of these benefits, DG MOSFETs shows better logic delays than the bulk devices [7].

The primary challenge for DG-CMOS technology is to explore two gate materials having proper work functions

for the desired threshold voltages of n- and p-channel DG MOSFETs respectively [5]. Either it can be accomplished by constructing both n- and p-channel DG MOSFETs side by side on the same substrate, connected in series between the supply terminals. In order to design circuits based on DG-CMOS technology, calculations and simulations are performed to optimize the various parameters, for which mathematical models depicting the electrical characteristics of n- and p-channel DG MOSFETs are required. Pre-requisites to use a device in the simulators are electrostatic potential distribution (φ), threshold voltage (V_{th}), and drain current (I_{ds}) models. The φ model is the key for the transistor electrical compact model, as it is needed for the calculation of I_{ds} and charge distribution [7, 8]. Several such models have been reported for the n-channel DG MOSFETs [9-15], whereas there are few [16-18] papers on modeling of p-channel DG MOSFETs which are inadequate for the short-channel lightly-doped silicon body. Cheralathan et al. [19] have reported a paper, where p-channel DG-MOSFET parameters were evaluated through sign-changing of the existing models [20] for the n-channel DG MOSFET. Since the mobility and physical effects

in p-channel devices are different than that of n-channel [17], thus, modeling of p-channel DG MOSFET is utmost necessary for the simulation of DG-CMOS circuits.

In this paper, analytical ϕ and I_{ds} models for the lightly doped symmetrical p-channel DG MOSFET are proposed in nanoscale regime (30 nm). However, the quantum mechanical effects are not highlighted in the proposed models, because it starts functioning to the devices when silicon body thickness (t_{si}) is less than 5 nm [13, 17]. The 2D Poisson's equation along-with the mobile charge density (holes) is solved through superposition method [9] to obtain the ϕ model. The proposed ϕ model is able to show the variation of channel potential with respect to gate-to-source voltage (V_{gs}) from weak to strong inversion region. The proposed ϕ model is also verified with the industry standard professional device simulator (Silvaco – ATLAS). Addition to this, the I_{ds} model is proposed from the existing models for symmetrical n-channel DG MOSFET [21–24] considering drift-diffusion approach. The reported I_{ds} model is improved by incorporating physical effects like threshold voltage roll-off, channel length modulation and surface roughness scattering.

2 Proposed potential distribution model

Fig. 1 shows the cross-sectional view of a p-channel symmetric DG MOSFET where the p-type source and drain are heavily doped and the silicon body is of lightly doped n-type ($\sim 10^{15} \text{ cm}^{-3}$). Table 1 lists all the parameters considered in this paper along with their symbols and values. In short p-channel DG MOSFET, the electrostatics potential $\phi(x, y)$ is determined by 2D Poisson's equation incorporated with hole density:

$$\frac{\partial^2 \phi(x, y)}{\partial x^2} + \frac{\partial^2 \phi(x, y)}{\partial y^2} = -\frac{q}{\epsilon_{si}} \frac{n_i^2}{N_{si}} e^{-\frac{[\phi(x, y) - V]}{V_T}}. \quad (1)$$

To derive the analytical solution for the ϕ model, the superposition method is applied, where $\phi(x, y)$ is split into two parts [25]: long channel component $\phi_0(y)$, which is the solution of 1D Poisson's equation, and short

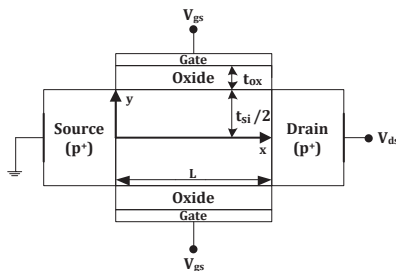


Fig. 1 Cross-sectional view of a symmetrical p-channel DG MOSFET.

Table 1 Symbol of the parameters and their values used in this paper.

Symbol	Parameter	Value considered
L	Channel length	30 nm
t_{si}	Silicon body thickness	12 nm for ϕ model and 10 nm for I_{ds} model
t_{ox}	Gate oxide thickness	1 nm
W	Channel width	50 nm
q	Elementary charge,	$1.6 \times 10^{-19} \text{ C}$
ϵ_0	Permittivity of free space	$8.85 \times 10^{-12} \text{ Fm}^{-1}$
ϵ_{ox}	Dielectric permittivity of gate oxide	3.9
ϵ_{si}	Dielectric permittivity of silicon	11.8
k_B	Boltzmann constant	$1.38 \times 10^{-23} \text{ JK}^{-1}$
n_i	Intrinsic charge density	$1.45 \times 10^{10} \text{ cm}^{-3}$
N_{si}	Body doping density	10^{15} cm^{-3}
N_{sd}	Source/drain doping density	10^{20} cm^{-3}
V_T	Thermal voltage	0.0259 V
V_{fbp}	Flat band voltage	$-\left(\chi + \frac{E_g}{2} - V_T \ln \frac{N_{si}}{n_i}\right)$ for I_{ds} model
V_{bip}	Built-in voltage	-0.58 V
χ	Electron affinity of silicon	4.17 eV
ϕ_m	Work function of metal gates	4.71 eV for ϕ model and 4.74 eV for I_{ds} model.
V	Quasi-fermi potential of holes	0 V at $x < L$ V_{ds} at $x = L$
E_g	Bandgap of silicon	1.08 eV
μ_{ac}	Mobility limited by acoustic phonons	
μ_{sr}	Mobility limited by surface roughness scattering	As given by the model in [30]
μ_b	Hole mobility in the silicon body	

channel component $\phi_1(x, y)$, which is the solution of 2D Laplace equation. The $\phi(x, y)$ for the short p-channel DG MOSFET can be expressed as:

$$\phi(x, y) = \phi_0(y) + \phi_1(x, y). \quad (2)$$

The 1D Poisson's equation across the thickness (along y) of p-channel device is given by [26]:

$$\frac{d^2 \phi_0(y)}{dy^2} = -\frac{q}{\epsilon_{si}} \frac{n_i^2}{N_{si}} e^{-\frac{[\phi_0(y) - V]}{V_T}} \quad (3)$$

with boundary condition at the silicon-oxide (Si – SiO₂) interface:

$$\left. \frac{d\varphi_0(y)}{dy} \right|_{y=\frac{t_{si}}{2}} = \frac{\varepsilon_{ox}}{\varepsilon_{si}} \frac{V_{gs} - V_{fb_p} - \varphi_0\left(\frac{t_{si}}{2}\right)}{t_{ox}}, \quad (4)$$

where V_{fb_p} is the flat band voltage. Equation (3) is integrated twice in order to obtain the solution [5].

$$\varphi_0(y) = V + V_T \ln \left[\left(\frac{qn_i^2}{2\varepsilon_{si}V_T N_{si}} \right) \left(\frac{t_{si}}{2\beta} \right)^2 \cos^2 \left(\frac{2\beta}{t_{si}} y \right) \right] \quad (5)$$

Substituting Eq. (5) in Eq. (4) yields an implicit expression for β :

$$\ln(\beta) - \ln(\cos \beta) + 2r\beta \tan \beta + \frac{V_{gs} - V_{fb_p} - V}{2V_T} + \ln \left[\left(\frac{2}{t_{si}} \right) \sqrt{\frac{2\varepsilon_{si}V_T N_{si}}{qn_i^2}} \right] = 0, \quad (6)$$

where $r = \frac{\varepsilon_{si}t_{ox}}{\varepsilon_{ox}t_{si}}$. Equation (6) has to be solved numerically in order to calculate the values of β . The expression for β is [27]:

$$\beta = \frac{t_{si}}{2} \sqrt{\frac{qn_i^2}{2\varepsilon_{si}V_T N_{si}}} e^{-\frac{[\varphi_0(y=0)-V]}{V_T}}, \quad (7)$$

where $\varphi_0(y=0)$ is the long channel component of $\varphi(x,y)$ describing the potential at the center of the silicon body. From Eq. (7), it is observed that the parameter β is a function of $\varphi_0(y=0)$ whose value is unknown. Since it is a transcendental equation, the β has to be solved numerically [6]. Yu et al. [22] proposed a computation method (algorithm) to explicitly obtain the values of β . The short channel component $\varphi_1(x,y)$ is the solution of 2D Laplace equation:

$$\frac{\partial^2 \varphi_1(x,y)}{\partial x^2} + \frac{\partial^2 \varphi_1(x,y)}{\partial y^2} = 0 \quad (8)$$

with boundary conditions:

$$\varphi_1(x,y) \Big|_{x=0} = V_{bi_p} - \varphi_0(y) \quad (9)$$

$$\varphi_1(x,y) \Big|_{x=L} = V_{bi_p} + V_{ds} - \varphi_0(y) \quad (10)$$

$$\left. \frac{\partial \varphi_1(x,y)}{\partial y} \right|_{y=\frac{t_{si}}{2}} = -\frac{\varepsilon_{ox}}{\varepsilon_{si}} \frac{\varphi_1(x, t_{si}/2)}{t_{ox}} \quad (11)$$

$$\left. \frac{\partial \varphi_1(x,y)}{\partial y} \right|_{y=0} = 0. \quad (12)$$

The solution of Eq. (8) has been solved in the reported paper [28].

$$\varphi_1(x,y) = \sum_{n=1}^3 \left[A_n e^{-\frac{2\lambda_n x}{t_{si}}} + B_n e^{\frac{2\lambda_n x}{t_{si}}} \right] \cos \left(\frac{2\lambda_n y}{t_{si}} \right) \quad (13)$$

The expressions of A_n and B_n are obtained through applying the boundary conditions (Eqs. (9) and (10)).

$$A_n = \frac{2 \sin(\lambda_n)}{[2\lambda_n + \sin(2\lambda_n)] \sinh \left(\frac{2\lambda_n L}{t_{si}} \right)} \left[V_{bi_p} + V_{ds} - V_{bi_p} e^{-\frac{2\lambda_n L}{t_{si}}} \right] + \frac{2\lambda_n \cos \left(\frac{\lambda_n}{2} \right) \varphi_0 \left(\frac{t_{si}}{2} \right)}{[2\lambda_n + \sin(2\lambda_n)] \sinh \left(\frac{2\lambda_n L}{t_{si}} \right)} \left[e^{-\frac{2\lambda_n L}{t_{si}}} - 1 \right] \quad (14)$$

$$B_n = \frac{2\lambda_n \cos \left(\frac{\lambda_n}{2} \right) \varphi_0 \left(\frac{t_{si}}{2} \right)}{[2\lambda_n + \sin(2\lambda_n)] \sinh \left(\frac{2\lambda_n L}{t_{si}} \right)} \left[1 - e^{-\frac{2\lambda_n L}{t_{si}}} \right] - \frac{2 \sin(\lambda_n)}{[2\lambda_n + \sin(2\lambda_n)] \sinh \left(\frac{2\lambda_n L}{t_{si}} \right)} \left[V_{bi_p} + V_{ds} - V_{bi_p} e^{-\frac{2\lambda_n L}{t_{si}}} \right] \quad (15)$$

The value of λ_n can be calculated numerically from the expression obtained through applying boundary conditions (Eqs. (11) and (12)):

$$\lambda_n \sin(\lambda_n) - \left(\frac{1}{2r} \right) \cos(\lambda_n) = 0. \quad (16)$$

Equation (2) can be used to calculate subthreshold current ($I_{ds,SUB}$). Assuming drift-diffusion approach, the $I_{ds,SUB}$ is expressed as:

$$I_{ds,SUB} = \frac{\mu_p q W \frac{n_i^2}{N_{si}} V_T \left[1 - e^{-\frac{V_{ds}}{V_T}} \right]}{\int_0^L \int_{-t_{si}/2}^{t_{si}/2} e^{-\frac{\varphi(x,y)}{V_T}} dx dy}, \quad (17)$$

where μ_p is the mobility of holes. The expression Eq. (17) is a semi-analytical model where the integrals are solved by using numerical method (Simpson's one-third rule) [29].

3 Proposed drain current model

The hole current density considering both drift and diffusion current density is expressed as:

$$J_p(x,y) = -q\mu_p \frac{n_i^2}{N_{si}} e^{-\frac{[\varphi_0(y)-V]}{V_T}} \frac{dV}{dx}. \quad (18)$$

Substituting Eq. (5) in Eq. (18) and integrating with respect to (w.r.t) x the expression for I_{ds} is obtained as:

$$I_{ds} = \mu_p \frac{2W}{L} \frac{4\epsilon_{si} V_T}{t_{si}} \int_0^{V_{ds}} \beta \tan \beta dV. \quad (19)$$

Replacing the term $\beta \tan \beta$ by q_i [23] and the derivative of V is obtained through differentiating Eq. (6) w.r.t. q_i .

$$dV = 2V_T \left[2r + \frac{1}{q_i} \right] dq_i, \quad (20)$$

where q_i is the normalized charge density. Substituting Eq. (20) in Eq. (19):

$$I_{ds} = \mu_p \frac{2W}{L} \frac{4\epsilon_{si} V_T}{t_{si}} \int_{q_{is}}^{q_{id}} q_i 2V_T \left[2r + \frac{1}{q_i} \right] dq_i, \quad (21)$$

where q_{is} and q_{id} are normalized charge density at the source and drain ends. On solving Eq. (21), the I_{ds} model for a long p-channel DG MOSFET is obtained.

$$I_{ds, long} = \mu_p \left(\frac{2W}{L} \right) \left(\frac{8\epsilon_{si}}{t_{si}} \right) V_T^2 \left[(q_{id} - q_{is}) + r(q_{id}^2 - q_{is}^2) \right] \quad (22)$$

Threshold voltage roll-off effect (ΔV_{th}) modifies the V_{gs} by the effective gate voltage (V_{ge}):

$$V_{ge} = V_{gs} - \Delta V_{th}.$$

The analytical expression of V_{th} for a short p-channel DG MOSFET is [27]:

$$V_{th} = V_{fbp} + k_1 V_T \ln Q + k_2 [V_{bi} + V_T \ln Q]^{\frac{1}{2}} [V_{bi} + V_{ds} + V_T \ln Q]^{\frac{1}{2}} + k_3 (2V_{bi} + V_{ds}) \quad (23)$$

$$\text{with } Q = \frac{Q_{th} N_{si}}{n_i^2 t_{si}}, \quad k_1 = -\frac{e^{\frac{4L}{\lambda}} - 2e^{\frac{2L}{\lambda}} + 1}{\left(e^{\frac{L}{\lambda}} - 1 \right)^4},$$

$$k_2 = \frac{2e^{\frac{L}{2\lambda}} \left(1 + e^{\frac{L}{\lambda}} \right)}{\left(e^{\frac{L}{\lambda}} - 1 \right)^2}, \quad k_3 = -\frac{2e^{\frac{3L}{\lambda}} - 4e^{\frac{2L}{\lambda}} + 2e^{\frac{L}{\lambda}}}{\left(e^{\frac{L}{\lambda}} - 1 \right)^4}.$$

The V_{th} of a long p-channel DG MOSFET is expressed as:

$$V_{th, long} = V_{fbp} + k_1 V_T \ln Q. \quad (24)$$

The expression of ΔV_{th} is given by:

$$\Delta V_{th} = V_{th, long} - V_{th}. \quad (25)$$

Q_{th} is the inversion charge sheet density at threshold condition. To compute the V_{th} , small value of $V_{ds} = 20$ mV

is considered so that the device does not reach saturation region of operation. The channel length modulation effect is considered by multiplying the core model $I_{ds, long}$ with the factor F_{CLM} [23]:

$$F_{CLM} = 1 + \left(\frac{\lambda}{L} \right)^A \left(\frac{V_{deff}}{V_{geff} - V_{th}} \right) \quad (26)$$

$$\text{with } A = 1 + \sqrt{\frac{\lambda}{L}},$$

$$V_{geff} = 2V_{th} + (V_{ge} - 2V_{th}) \tanh \left(\frac{V_{ge}}{V_{th}} \right)^2,$$

$$V_{deff} = V_{ds} \tanh \left(\frac{1.5V_{ds}}{V_{geff}} \right)^2,$$

where $\lambda = \sqrt{\frac{\epsilon_{si} \epsilon_{ox} t_{ox} + \epsilon_{ox} \frac{t_{si}^2}{4} - \epsilon_{ox} \frac{t_{si}^2}{16}}{2\epsilon_{ox}}}$ is the natural channel

length [13]. In order to smoothen the $I_{ds, long}$ model Eq. (22) in the transition from subthreshold to linear region of operation, a flag called $isSI$ [24] has been used.

$$isSI = \frac{1}{2} - \frac{\tanh \left[5(V_{ge} - V_{th}) \right]}{2} \quad (27)$$

$$q_i = \left(\frac{1}{2r} \right) \text{Lambert } W$$

$$\left[\frac{qt_{ox}}{\epsilon_{ox}} \sqrt{\frac{n_i^2 \epsilon_{si}}{2k_B T N_{si}}} e^{-\left(\frac{V_{ge} - V_{fbp} - V}{2V_T} \right)} e^{-\left(\frac{V_{ge} - V_{th} - V}{2\eta V_T} \right)} \right] \left[A + e^{-\left(\frac{V_{ge} - V_{th} - V}{2\eta V_T} \right)} \right] \quad (28)$$

The expression of q_i (Eq. (28)) is incorporated with various parameters [13, 24] such as:

$$\eta = \frac{SS}{V_T} \ln 10, \quad \eta' = \frac{\eta}{2 - \eta},$$

$$SS = V_T \ln 10 \left[\frac{e^{\frac{4L}{2\lambda}} - 1}{e^{\frac{4L}{2\lambda}} - 2e^{\frac{3L}{2\lambda}} + 2e^{\frac{L}{2\lambda}}} \right], \quad (29)$$

$$A = \frac{4}{e^{0.8}} e^{-(V_{th} + V_{fbp})}.$$

Consideration of surface roughness scattering effect substitutes the μ_p with the function [30]:

$$\frac{1}{\mu} = \frac{1}{\mu_{ac}} + \frac{1}{\mu_{sr}} + \frac{1}{\mu_b}. \quad (30)$$

The complete I_{ds} model incorporated with ΔV_{th} , channel-length modulation, and surface roughness scattering effects is expressed as:

$$I_{ds} = \mu \left(\frac{2W}{L} \right) \left(\frac{8\epsilon_{si}}{t_{si}} \right) V_T^2 \left[(q_{id} - q_{is}) + isSI \times r (q_{id}^2 - q_{is}^2) \right] F_{CLM}. \quad (31)$$

4 Results and discussion

The φ model Eq. (2) is validated by performing simulation in Silvaco – ATLAS and to validate the I_{ds} model Eq. (31), comparison has been made with the simulation results in [19].

4.1 Potential distribution

The φ model Eq. (2) is calculated in MATLAB by considering the values: $V = 0$, $V_{bi_p} = -0.58$ V, and $V_{fb_p} = -0.02$ V (Table 1). The potential distribution at the surface (φ_s) shown in Fig. 2 (a), (b), are plotted for different bias conditions. The potential distribution at the center of the silicon body (φ_{cent}), and at the effective conductive path ($\varphi_{t_{si}/4}$) are found in good agreement with the simulation data as shown in Fig. 2 (c), (d). Table 2 presents the absolute error analysis of the potential distribution along the channel at different positions (y) across the depth of silicon body. The maximum error ($\approx 17.67\%$) is observed at $y = 4.0$ nm and minimum error ($\approx 2.95\%$) is observed at $y = 0.0$ nm (at the center of the silicon body). The average error at $y = 6.0$ nm (at the surface)

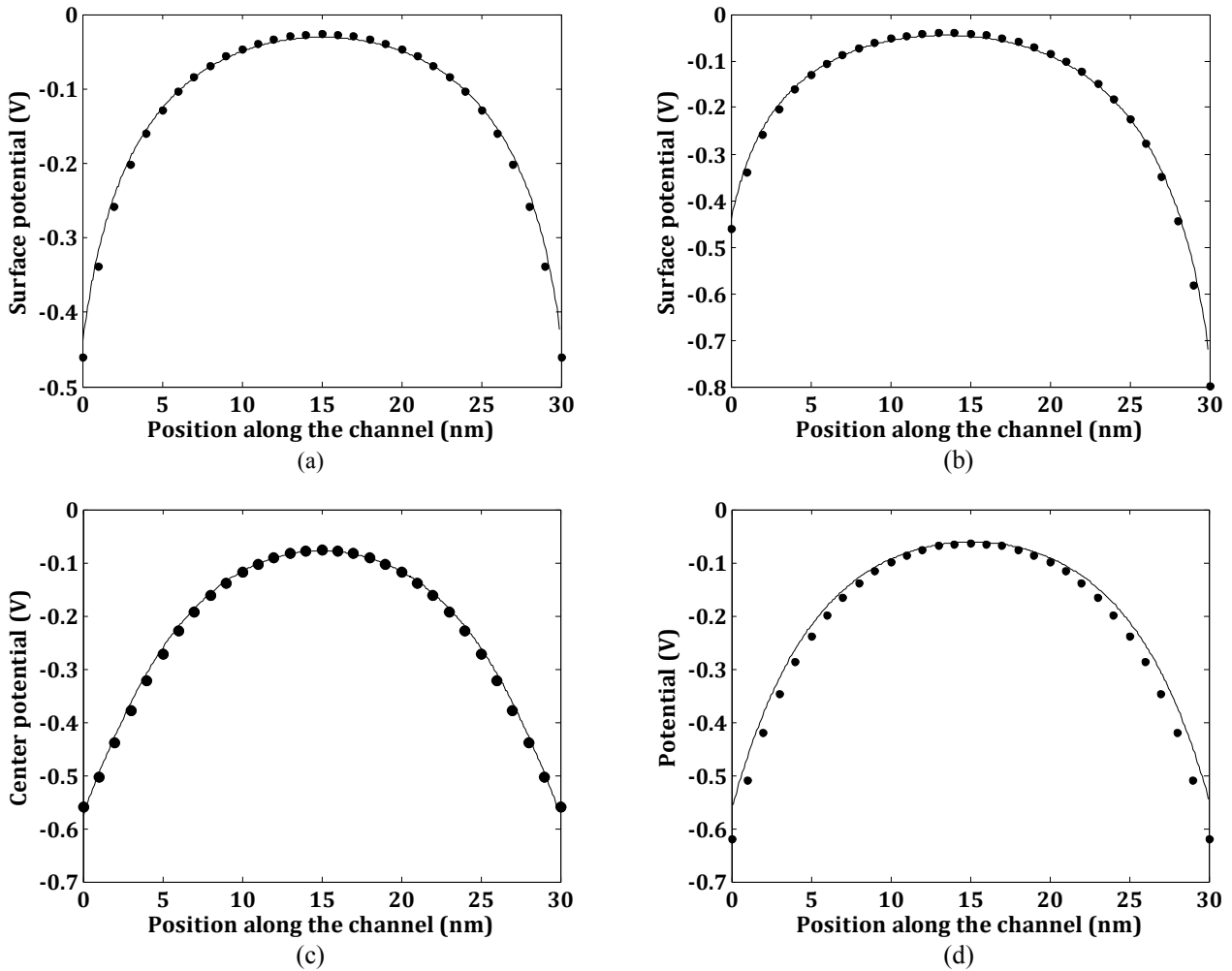


Fig. 2 Model results (symbols) of the symmetrical p-channel DG MOSFET with dimensions: $L = 30$ nm, $t_{ox} = 1$ nm and $t_{si} = 12$ nm, being compared with the simulation results obtained from Silvaco-ATLAS (solid lines) (a) surface potential along the channel at bias conditions $V_{gs} = 0$ V, $V_{ds} = 0$ V, (b) surface potential along the channel at bias conditions $V_{gs} = 0$ V, $V_{ds} = -0.4$ V, (c) center potential along the channel at bias conditions $V_{gs} = 0$ V, $V_{ds} = 0$ V, (d) potential distribution along the effective conductive path $\left(y = \frac{t_{si}}{4} \right)$ at bias condition $V_{gs} = 0$ V, $V_{ds} = 0$ V.

Table 2 Absolute error analysis of the ϕ model at different positions (y) across the depth of silicon body.

y (nm)	Maximum error (V)	Average error (V)	Maximum error (%)
0	0.0170	0.0060	2.9553
0.5	0.0244	0.0083	6.5815
1.0	0.0272	0.0097	7.1886
1.5	0.0244	0.0103	6.1094
2.0	0.0317	0.0139	6.9771
2.5	0.0443	0.0163	8.1720
3.0	0.0749	0.0207	13.7677
3.5	0.0810	0.0216	15.1330
4.0	0.0940	0.0228	17.6772
4.5	0.0797	0.0111	14.9787
5.0	0.0651	0.0102	13.0798
5.5	0.0488	0.0088	10.1411
6.0	0.0277	0.0064	7.5106

and $y = 0.0$ nm are found as 0.0064 V and 0.0060 V respectively. On the other hand, the same for $y = 3.0$ nm (at the effective conductive path [13]) is found as 0.0207. The proposed ϕ model works well in describing the potential distribution at the surface and center of the silicon body rather than any other point. This is why the model results shown in Fig. 2 (a)-(c) are in good agreement with the simulation results, and deviation from the simulated data is observed in the potential distribution shown in Fig. 2 (d). The variation of ϕ_s , ϕ_{cent} , and $\phi_{t_{si}/4}$ w.r.t. V_{gs} considered at $x = L/2$ are shown in Fig. 3. It is observed that ϕ_s , ϕ_{cent} , and $\phi_{t_{si}/4}$ pass through a common point for a particular value of V_{gs} which is termed as crossover point [14, 31]. The presented ϕ model works well in the subthreshold region of operation mainly for V_{gs} lower than -0.4 V.

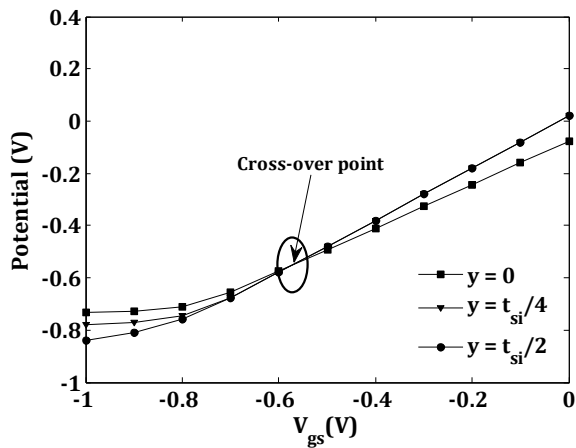


Fig. 3 The ϕ model results showing ϕ_s , ϕ_{cent} , and $\phi_{t_{si}/4}$ at $x = L/2$. (Only model results).

4.2 Drain current model

The I_{ds} model Eq. (30) results (Fig. 4) are calculated considering parameter values given in Table 1 for the device dimension: $L = 30$ nm, $W = 50$ nm, $t_{si} = 10$ nm, $t_{ox} = 1$ nm. To compute the V_{th} , $Q_{th} = 5 \times 10^{12}$ cm⁻² [23] is considered. The V_{fbp} is calculated using the relation: $V_{fbp} = \phi_m - \left(\chi + \frac{E_g}{2} - V_T \ln \frac{N_{si}}{n_i} \right)$. In Fig. 4, the I_{ds} model results are computed by considering constant hole

mobility (μ_p) of 470.5 cm²/Vs [30], ignoring the effects of surface-roughness scattering [23]. Fig. 4 (a), (b) shows the transfer characteristics for different values of V_{ds} from where the extracted subthreshold slope (SS) has been calculated as 64.2 mV/decade (Fig. 4 (b)). The output characteristics for the same DG MOSFET structure are shown in Fig. 4 (c). In order to validate the proposed I_{ds} model, a comparison has been made with the simulation results published in [19]. Fig. 4 (d) shows the transfer characteristics in comparison with simulation results of [19]. From the comparison, maximum absolute error = 0.0880 mA has been found in case of $V_{ds} = -0.1$ V and the same for $V_{ds} = -1.0$ V has been found as 0.0360 mA. Disagreement in the characteristics observed is due to the consideration of only mobile-charges in Poisson's equation and difference in physical effects considered in the presented analyses in this paper. Table 3 presents the differences in the physical effects and parameter's values considered in [19] and this presented work.

5 Conclusion

The analytic potential distribution model for lightly doped symmetrical p-channel DG MOSFET is deduced by solving 2D Poisson's equation incorporated with hole density. The Poisson's equation is solved using superposition method due to which the potential distribution model is valid from weak to strong inversion regions. Good agreement has been observed while comparing the analytical model results with the simulation results of an industry standard professional device simulator Silvaco-ATLAS. Moreover, the drain current model for lightly-doped p-channel DG MOSFET has also been introduced. Physical effects like threshold voltage roll-off, channel length modulation and surface roughness scattering are considered in this analysis. The equations have been implemented in MATLAB and verified with its counterparts.

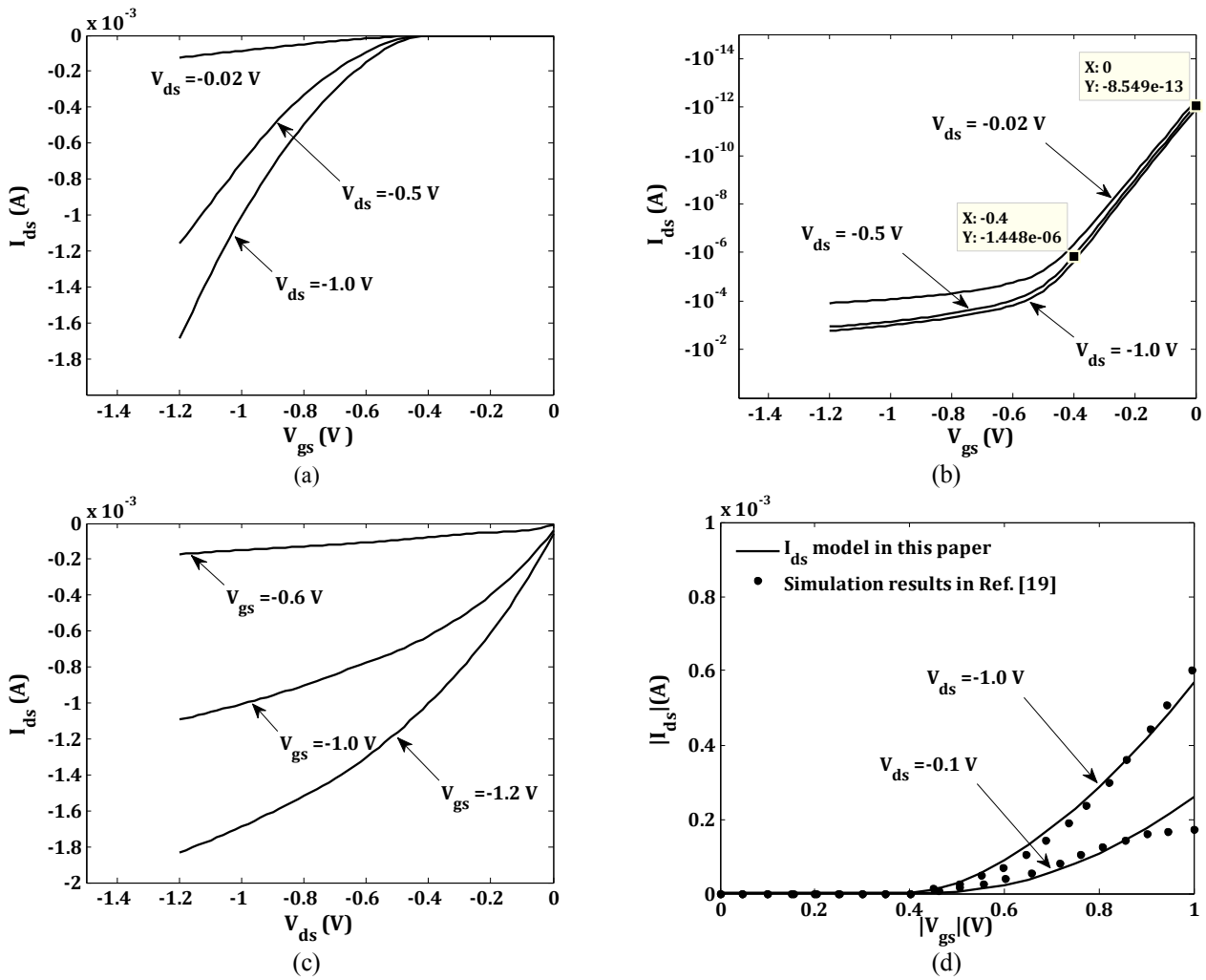


Fig. 4 Model results of the symmetrical p-channel DG MOSFET with dimensions $W = 50$ nm, $L = 30$ nm, $t_{si} = 10$ nm, and $t_{ox} = 1$ nm in (a) transfer characteristics in linear scale, (b) transfer characteristics in semi-logarithmic scale, (c) output characteristics, (d) transfer characteristics in comparison with the simulation results of [19] considering the drift-diffusion approach with device dimensions $L = 22$ nm, $W = 100$ nm, $t_{ox} = 0.7$ nm, effective oxide thickness of high- K dielectric layer = 1.1 nm.

Table 3 Parameters used by Cheralathan et al. [19] and in this presented model.

Physical parameters	Cheralathan et al. [19]	Presented model
Poisson's equation	Mobile charge and depletion charge.	Only mobile charge.
Physical effects	Threshold voltage roll-off, DIBL, subthreshold slope degradation, velocity saturation.	Threshold voltage roll-off, channel length modulation.
Parameter values	Constant hole mobility, $(\mu_p) = 95$ cm ² /Vs.	Constant hole mobility, $(\mu_p) = 95$ cm ² /Vs.
	Carrier velocity saturation, $(v_{sat}) = 1.01$ cm/s ⁻¹ .	Work function of metal gates, $(\phi_m) = 4.74$ eV [23].
	Mobility degradation parameters [32], $\theta_1 = 0.4$ V ⁻¹ and $\theta_2 = 3.9$ V ⁻² .	Flat band voltage, $(V_{fb}) = 0.2983$ V Body doping density, $(N_{si}) = 10^{15}$ cm ⁻³ .

Acknowledgement

This work was supported by Ministry of Electronics and Information Technology, Government of India, under Visvesvaraya PhD Scheme. The authors would like to thank Dr. Shubankar Majumdar, Assistant professor, Department of Electronics and Communication Engineering, National Institute of Technology Meghalaya, India formerly associated with National Institute of Technology Raipur, India for his help and useful suggestions.

References

- [1] Razavi, B. "Design of Analog CMOS Integrated Circuits", 2nd ed., McGraw-Hill, New York, USA, 2001.
- [2] Wong, H. S. P. "Beyond the conventional transistor", IBM Journal of Research and Development, 46(2.3), pp. 133–168, 2002.
<https://doi.org/10.1147/rd.462.0133>
- [3] Frank, D. J., Laux, S. E., Fischetti, M. V. "Monte Carlo simulation of a 30 nm dual-gate MOSFET: How short can Si go?", In: International Technical Digest on Electron Devices Meeting, San Francisco, USA, 1992, pp. 553–556.
<https://doi.org/10.1109/IEDM.1992.307422>
- [4] Balestra, F., Cristoloveanu, S., Benachir, M., Brini, J., Elewa, T. "Double-gate silicon-on-insulator transistor with volume inversion: A new device with greatly enhanced performance", IEEE Electron Device Letters, 8(9), pp. 410–412, 1987.
<https://doi.org/10.1109/EDL.1987.26677>
- [5] Taur, Y. "An analytical solution to a double-gate MOSFET with undoped body", IEEE Electron Device Letters, 21(5), pp. 245–247, 2000.
<https://doi.org/10.1109/55.841310>
- [6] Lu, H. "Compact Modeling of Double-Gate MOSFETs", PhD Dissertation, University of California, 2006.
- [7] Dunga, M. V. "Nanoscale CMOS Modeling", PhD Dissertation, University of California, 2008.
- [8] Deng, W., Ma, X., Huang, J. "Surface potential calculation and drain current model for junctionless double-gate polysilicon TFTs", AIP Advances, 4(8), Article number: 087107, 2014.
<https://doi.org/10.1063/1.4892609>
- [9] Oh, S. H., Monroe, D., Hergenother, J. M. "Analytic description of short-channel effects in fully depleted double-gate and cylindrical surrounding-gate MOSFETs", IEEE Electron Device Letters, 21(9), pp. 445–447, 2000.
<https://doi.org/10.1109/55.863106>
- [10] Chen, Q., Agrawal, B., Meindl, J. D. "A comprehensive analytical subthreshold swing (S) model for double-gate MOSFETs", IEEE Transactions on Electron Devices, 49(6), pp. 1086–1090, 2002.
<https://doi.org/10.1109/TED.2002.1003757>
- [11] Liang, X., Taur, Y. "A 2-D analytical solution for SCEs in DG MOSFETs", IEEE Transactions on Electron Devices, 51(9), pp. 1385–1391, 2004.
<https://doi.org/10.1109/TED.2004.832707>
- [12] El Hamid, H. A., Guitart, J. R., Iniguez, B. "Two-Dimensional Analytical Threshold Voltage and Subthreshold Swing Models of Undoped Symmetric Double-Gate MOSFETs", IEEE Transactions on Electron Devices, 54(6), pp. 1402–1408, 2007.
<https://doi.org/10.1109/TED.2007.895856>
- [13] Tsormpatzoglou, A., Dimitriadis, C. A., Clerc, R., Rafhay, Q., Pananakakis, G., Ghibaudo, G. "Semi-Analytical Modeling of Short Channel Effects in Si and Ge Symmetrical Double-Gate MOSFETs", IEEE Transactions on Electron Devices, 54(8), pp. 1943–1952, 2007.
<https://doi.org/10.1109/TED.2007.901075>
- [14] Ray, B., Mahapatre, S. "Modeling of Channel Potential and Subthreshold Slope of Symmetric Double-Gate Transistor", IEEE Transactions on Electron Devices, 56(2), pp. 260–266, 2009.
<https://doi.org/10.1109/TED.2008.2010577>
- [15] Monga, U., Fjedly, T. A. "Compact subthreshold current modeling of short-channel nanoscale double-gate MOSFET", IEEE Transactions on Electron Devices, 56(7), pp. 1533–1537, 2009.
<https://doi.org/10.1109/TED.2009.2021714>
- [16] Moers, J., Trelenkamp, S., Hart, A. V. D., Goryll, M., Mantl, S., Kordos, P., Luth, H. "Vertical p-channel double-gate MOSFETs", In: ESSDERC '03. 33rd Conference on European Solid-State Development Research, Estoril, Portugal, 2003, pp. 143–146.
<https://doi.org/10.1109/ESSDERC.2003.1256831>
- [17] Song, J., Yuan, Y., Yu, B., Xiong, W., Taur, Y. "Compact Modeling of Experimental n- and p-Channel FinFETs", IEEE Electron Device Letters, 57(6), pp. 1369–1374, 2010.
<https://doi.org/10.1109/TED.2010.2047067>
- [18] Kumari, V., Illango, A., Saxena, M., Gupta, M. "Charge-based modeling of channel material-engineered P-type double-gate MOSFET", In: 2014 IEEE 2nd International Conference on Emerging Electronics (ICEE), Bangalore, India, 2014, pp. 1–4.
<https://doi.org/10.1109/ICEmElec.2014.7151141>
- [19] Cheralathan, M., Contreras, E., Alvarado, J., Cerdeira, A., Iannaccone, G., Sangiorgi, E., Iniguez, B. "Implementation of nanoscale double-gate CMOS circuits using compact advanced transport models", Microelectronics Journal, 44(2), pp. 80–85, 2013.
<https://doi.org/10.1016/j.mejo.2012.11.006>
- [20] Alvarado, J., Iniguez, B., Estrada, M., Flandre, D., Cerdeira, A. "Implementation of the symmetric double-gate MOSFET model in Verilog-A for circuit simulation", International Journal of Numerical Modelling, Electronic Networks, Devices and Fields, 23(2), pp. 88–106, 2010.
<https://doi.org/10.1002/jnm.725>
- [21] Taur, Y., Liang, X., Wang, W., Lu, H. "A continuous, analytic drain-current model for DG-MOSFETs", IEEE Electron Device Letters, 25(2), pp. 107–109, 2004.
<https://doi.org/10.1109/LED.2003.822661>
- [22] Yu, B., Lu, H., Liu, M., Taur, Y. "Explicit Continuous Models for Double-Gate and Surrounding-Gate MOSFETs", IEEE Transactions on Electron Devices, 54(10), pp. 2715–2722, 2007.
<https://doi.org/10.1109/TED.2007.904410>
- [23] Tsormpatzoglou, A., Tassis, D. H., Dimitriadis, C. A., Ghibaudo, G., Pananakakis, G., Collaert, N. "Analytical modelling for the current-voltage characteristics of undoped or lightly-doped symmetric double-gate MOSFETs", Microelectronic Engineering, 87(9), pp. 1764–1768, 2010.
<https://doi.org/10.1016/j.mee.2009.10.015>
- [24] Papathanasiou, K., Theodorou, C. G., Tsormpatzoglou, A., Tassis, D. H., Dimitriadis, C. A., Bucher, M., Ghibaudo, G. "Symmetrical unified compact model of short-channel double-gate MOSFETs", Solid-State Electronics, 69, pp. 55–61, 2012.
<https://doi.org/10.1016/j.sse.2011.10.002>
- [25] Chen, Q., Harrell, E. M., Meindl, J. D. "A physical short-channel threshold voltage model for undoped symmetric double-gate MOSFETs", IEEE Transactions on Electron Devices, 50(7), pp. 1631–1637, 2003.
<https://doi.org/10.1109/TED.2003.813906>

- [26] Song, J. "Compact Modeling of Experimental n- and p-channel Fin-FETs", PhD Dissertation, University of California, 2010.
- [27] Ahmed, R. U., Saha, P. "Modeling of Threshold Voltage and Subthreshold Current for P-Channel Symmetric Double-Gate MOSFET in Nanoscale Regime", In: 2017 IEEE International Symposium on Nanoelectronic and Information Systems (iNIS), Bhopal, India, 2017, pp. 179–183.
<https://doi.org/10.1109/iNIS.2017.44>
- [28] Shankar, R., Kaushal, G., Maheshwaram, S., Dasgupta, S., Manhas, S. K. "A Degradation Model of Double Gate and Gate-All-Around MOSFETs With Interface Trapped Charges Including Effects of Channel Mobile Charge Carriers", IEEE Transactions on Device Materials Reliability, 14(2), pp. 689–697, 2014.
<https://doi.org/10.1109/TDMR.2014.2310292>
- [29] Grewal, B. S. "Higher Engineering Mathematics", Khanna Publishers, New Delhi, India, 2012.
- [30] Lombardi, C., Manzini, S., Saporito, A., Vanzi, M. "A physically based mobility model for numerical simulation of nonplanar devices", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 7(11), pp. 1164–1171, 1988.
<https://doi.org/10.1109/43.9186>
- [31] Baruah, R. K., Mahapatre, S. "Justifying threshold voltage definition for undoped body transistors through "crossover point" concept", Physica B: Condensed Matter, 404(8-11), pp. 1029–1032, 2009.
<https://doi.org/10.1016/j.physb.2008.11.005>
- [32] Cheralathan, M., Sampedro, C., Roldán, J. B., Gámiz, F., Iannaccone, G., Sangiorgi, E., Iñiguez, B. "Compact drain-current model for reproducing advanced transport models in nanoscale double-gate MOSFETs", Semiconductor Science and Technology, 26(9), Article number: 095015, 2011.
<https://doi.org/10.1088/0268-1242/26/9/095015>

Appendix

By separation of variables, the short channel potential component $\varphi_1(x, y)$ can be expressed as:

$$\varphi_1(x, y) = X(x)Y(y), \quad (32)$$

substituting Eq. (32) in Laplace equation:

$$Y(y) \frac{\partial^2 X(x)}{\partial x^2} + X(x) \frac{\partial^2 Y(y)}{\partial y^2} = 0$$

$$\Rightarrow \frac{1}{Y(y)} \frac{\partial^2 Y(y)}{\partial y^2} = -\frac{1}{X(x)} \frac{\partial^2 X(x)}{\partial x^2} = k.$$

The boundary value problem reduces to two ordinary differential equations in x and y .

$$\frac{d^2 X(x)}{dx^2} + kX(x) = 0 \quad \text{and} \quad \frac{d^2 Y(y)}{dy^2} - kY(y) = 0.$$

If $k \geq 0$, then $\frac{d^2 Y(y)}{dy^2} - kY(y) = 0$ will have trivial solution. So assuming $k = -\lambda^2 < 0$ then, $\frac{d^2 Y(y)}{dy^2} + \lambda^2 Y(y) = 0$ has the general solution:

$$Y(y) = A \cos(\lambda y) + B \sin(\lambda y), \quad (33)$$

differentiating Eq. (33) with respect to y :

$$\frac{dY(y)}{dy} = -A\lambda \sin(\lambda y) + B\lambda \cos(\lambda y), \quad (34)$$

applying the boundary condition (Eq. (12)):

$$\Rightarrow X(x) \frac{dY(y)}{dy} \Big|_{y=0} = 0,$$

$$\text{since } X(x) \neq 0, \text{ so } \frac{dY(y)}{dy} \Big|_{y=0} = 0$$

$$\Rightarrow -A\lambda \sin(\lambda 0) + B\lambda \cos(\lambda 0) = 0$$

$$\Rightarrow B = 0$$

$$\therefore Y(y) = A \cos(\lambda y),$$

applying the boundary condition (Eq. (11)):

$$\Rightarrow X(x) \frac{dY(y)}{dy} \Big|_{y=\frac{t_{si}}{2}} = -\frac{\epsilon_{ox}}{\epsilon_{si}} \frac{\varphi_1(x, t_{si}/2)}{t_{ox}}$$

$$\Rightarrow X(x) \left[-A\lambda \sin\left(\frac{\lambda t_{si}}{2}\right) \right] = -\frac{\epsilon_{ox}}{\epsilon_{si}} \frac{X(x)Y\left(\frac{t_{si}}{2}\right)}{t_{ox}}$$

$$\Rightarrow A\lambda \sin\left(\frac{\lambda t_{si}}{2}\right) = \frac{\epsilon_{ox}}{\epsilon_{si}} \frac{A \cos\left(\frac{\lambda t_{si}}{2}\right)}{t_{ox}}$$

$$\Rightarrow \frac{\lambda t_{si}}{2} \sin\left(\frac{\lambda t_{si}}{2}\right) - \frac{\epsilon_{ox} t_{si}}{2\epsilon_{si} t_{ox}} \cos\left(\frac{\lambda t_{si}}{2}\right) = 0. \quad (35)$$

Equation (35) has infinitely many solutions and can be generalized as:

$$\Rightarrow \lambda_n \sin(\lambda_n) - \left(\frac{1}{2r}\right) \cos(\lambda_n) = 0, \quad (36)$$

where $\lambda_n = \frac{\lambda t_{si}}{2}$.