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# Integrated Thermal Management in System-on-Package Devices

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**Abstract**

Thanks to the System-on-Package technology (SoP) the integration of different elements into a single package was enabled. However, from the thermal point of view the heat removal path in modern packaging technologies (FCBGA) goes through several layers of thermal interface material (TIM) that together with the package material create a relatively high thermal resistance which may lead to elevated chip temperature which causes functional error or other malfunctions. In our concept, we overcome this problem by creating integrated microfluidic channel based heat sink structures that can be used for cooling the high heat dissipation semiconductor devices (e.g.: processors, high power transistor or concentrated solar cells). These microchannel cooling assemblies can be integrated into the backside of the substrate of the semiconductor devices or into the system assemblies in SoP technology. In addition to the realization of the novel CMOS compatible microscale cooling device we have developed precise and valid measurement methodology, simulation cases studies and a unique compact model that can be added to numerical simulators as an external node. In this paper the achievements of a larger research are summarized as it required the cooperation of several experts in their fields to fulfil the goal of creating a state-of-the-art demonstrator.

**Keywords**

microscale cooling, thermal management, thermal characterization, thermo-hydrodynamic modeling

## 1 Introduction

Due to the more-than-Moore integration, the continuously evolving 3D packaging technologies and the ongoing scaling, even the constant dissipation of integrated circuits will result in elevated die(s) temperature [1-3]. Since the maximum temperature is needed to be limited, several cooling concepts have been developed. As macro-scale conventional air-cooling solutions are at their limits, new concepts are investigated in order to deal with the increased heat flux and to prevent the die temperatures from reaching critical values. One promising solution is the application of microscale cooling structures formed in the backside of the semiconductor substrate either by wet- or physical-etching (e.g.: deep reactive-ion etching).

In case of integrated microscale cooling structures, the thermal resistance between the junction and the coolant depends on several fluid dynamic properties - e.g.: the flow rate, the exact geometry and the topology of the channels (dimensions, 3D layout etc.). In addition, it is also mandatory to determine the thermal resistance at different flow-rates in order to validate the analytical calculation and/or simulation results and validate the cooling structure itself.

At first, these microscale structures were only used for cooling purpose, but in several cases, they were applied in integrated thermal management solutions (e.g.: temperature homogenization along the die or among different dies in a system-in-package structure). In special cases, this kind of management is indispensable, because one of the sources of functional errors in integrated digital circuits is the temperature inhomogeneity, whereas the delay of standard digital cells is varied by the temperature change [4-8]. For example, in case of clock distribution networks (CDN) of processors [9, 10] the dynamic clock skew minimization requires small temperature changes. In addition, if this skew is investigated in stacked die or 3D packaging this problem would be even more serious.

In the beginning of the research work, we aimed to create appropriate compact models, where the heat transfer rate through the microchannel walls is accurately

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modelled at different points of the channel(s) and could be used as possible inputs for thermal simulators or logical simulator environments [11-20]. We intended to develop a new method to extend in-house electro-thermal simulator tool with the developed compact models to make it eligible to accurately simulate the modelled hydrodynamics behavior in a short time.

In another approach, logi-thermal simulation is a relatively new simulation paradigm which connects gate level or even higher abstraction level simulation of digital circuits to thermal simulation, providing a consistent calculation of the switching event distribution and the corresponding evolving dissipation distribution, timing integrity and temperature distribution. The basics principles of logi-thermal simulation have been described in numerous conference and journal papers [4-8].

In a previous paper [8] we have shown with the help of logi-thermal simulation that placement of through-silicon vias (TSVs) affects the temperature distribution of 3D ICs. In contrast to prior publications dealing with this topic where CFD analysis of the microchannels was performed assuming different power maps, in the frame of this research project we aimed to include the newly developed compact models of microscale channel structures into our logi-thermal simulation environment [4-7].

Other aim was to develop a CMOS compatible process technology to realize microscale channel structures in the silicon substrate of integrated circuits. Another aim was to realize channels with the dimensions of 100 micrometers with either rectangle or trapezoidal cross shape. It would be better if the newly developed process steps can be applied in mass production, so couple of wafers can be manufactured at once (batch processing).

To validate the effectiveness and the accuracy of the evolved compact models we needed a reliable, repeatable characterization technique based on standard measuring methods. It enabled the precise determination of the partial thermal resistance of the microscale heat-sink structure at different flow rates.

Based on this planned goals our work was divided into four larger areas which represented different branches of the research work:

1. processing and manufacturing;
2. simulation and modelling;
3. characterization, measurements;
4. possible applications.

## 2 Manufacturing technologies, sample processing and preparation

As mentioned the processing of a CMOS compatible integrated microscale heatsink structures was needed to be developed. The technology setup was elaborated and several experimental setups were carried out. It was followed by the realization of different channel patterns and the development of process steps for integrating microscale heat sink structure into semiconductor devices. Finally, some prototypes were developed. It must be mentioned that close interactions had to be maintained between each segment of the whole research since for example the results of the simulations influenced the layout of the channels in the microscale heatsink structures. Also, the built-up of the support structure applied during the measurements determined the geometric dimensions and set-up of the investigated structures.

The key contribution of this segment to the whole research was the elaboration of the CMOS compatible integrated manufacturing technology since the microscale heatsink are aimed to be used on the back side of high yield, high performance devices so the applicability must be demonstrated [21-23].

By applying CMOS compatible wet chemical etching process realizing integrated microscale channel structures several sample devices were created. In the first phase, microcooler devices with radial channel patterns were created and covered using anodic bonding procedure. The layout of the devices were similar to a formerly realized microscale cooler structure which was manufactured using LIGA process. This way the two results were comparable.

Based on our simulations, analytical modelling and calculation (Sections 3 and 4) new channel architecture and layout were developed and the necessary chrome mask sets were designed and manufactured. The new integrated microscale heatsink structures with the new channel patterns were realized on (100) orientation silicon wafers which resulted in steeper channel walls and higher Nusselt number and heat exchange ratio. This will be proved by measurements in the following year.

At this point, it must be emphasized that since the System-on-Package integration is not a straightforward task, many fabrication steps have to be fully developed before a successful chip-level cooling system is ready to be used. That is why a refined manufacturing technology had to be developed and presented which gives the possibility

to create the microscale heatsink structures integrated together with the electronic devices. With the refined manufacturing technology, several channel patterns were created and tested with the enhanced thermal characterization method (which is presented in Section 4). Some of the new channel patterns were designed not to achieve the highest heat removal capability but for the fine tuning and validating of the modelling and characterization technique.

All devices were manufactured by using double side polished n-type (100) orientation Cz-Si wafers with bulk resistivity between 5-10 Ω·cm and thickness of 250 ±25 µm. After a standard RCA cleaning procedure, the first 200 nm $SiO_2$ masking layer was grown by thermal oxidation. After patterning the masking layer, n-type spin-on dopant source was spun on the wafer for 20 seconds at 3000 rpm, followed by a 20-minute pre-deposition in a mixture of $N_2$ and $O_2$ gas at 1000 °C. During 35-minutes drive-in process in $O_2$ ambient a $SiO_2$ layer was formed on the wafers, which was further used as masking layer in the second p-type diffusion step. The boron diffusion using planar diffusion sources in the center position of the chips was formed after patterning the masking oxide layer and 990 °C pre-deposition step for 30 minutes was executed in $N_2$ gas, followed by 45-minutes drive-in step at 1100 °C.

Masking layer needed for the microchannel etching process was grown during the drive-in step performed in high purity $O_2$ ambient gas. The commercially available 25 wt.% (percentage by weight) TMAH solution was diluted with deionized (DI) water to 5 wt.% and the microchannel etching process was performed on the opposite side of the wafers at elevated temperature (92 °C). In order to reach higher silicon etching rates 2 g/l ammonium peroxydisulfate (AP) was added to the etchant every hour to increase the etching rate uniformity and stabilize the etching rate over the entire process time.

After the etching was finished and the desired microchannel depth was reached, the remaining silicon dioxide thickness on both sides of the wafer was enough for patterning and masking during metallization processes. 280 nm thick contact layer deposition was performed by Al thermal evaporation with a source of 99.99 Al wire on hot filament. The aluminum layer was selectively removed from the surface by Al etching in $H_3PO_4$:$HNO_3$ solution and the final metallization layer was obtained after thermal annealing at 450 °C in $N_2$ atmosphere. Using the same anisotropic etching setup and parameters on additional silicon wafers through-silicon holes with proper positioning above the microchannels were fabricated for gas inlet and channel sealing purposes. Using wafer dicing 15 × 15 $mm^2$ chips were obtained and wafer bonding was employed in order to have the final samples suitable for thermal transient measurements. In Fig. 1 the detailed layout design of the device can be seen.

The chips were bonded together by using thermocompression bonding technique. First, the diced chips were preconditioned. This included: ultrasonic cleaning in DI water, a standard $HNO_3$ cleaning cycle, $O_2$ plasma treatment for surface activation and surface hydration in DI water. The bonding procedure was carried out at $10^{-3}$ mbar chamber pressure, 3000 mbar bonding pressure and 500 °C bonding temperature for 2 hours. The relaxation time of the samples before measurement was one week.

The new structures (Fig. 2) can be applicable for liquid and gas fluid as well, so the applicability and integrability of this structure into a System-on-Package device will be ensured.

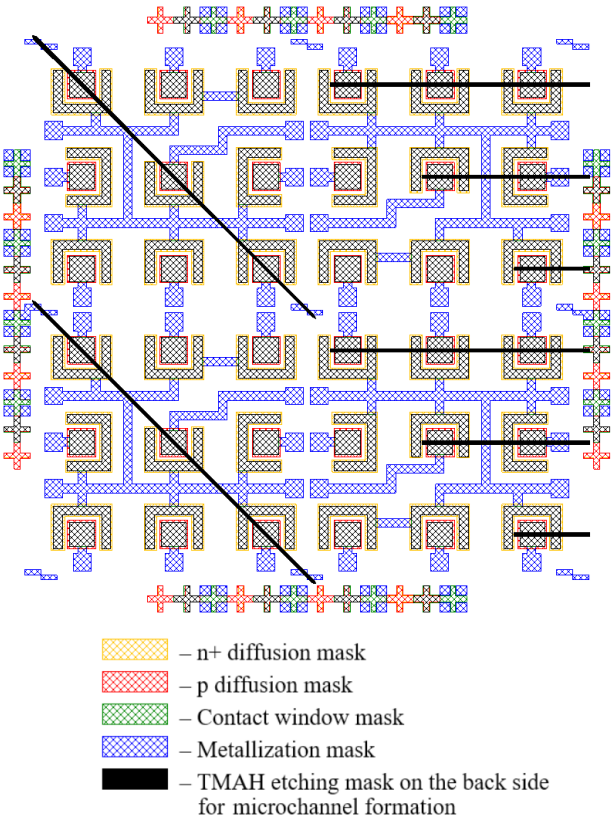


**Fig. 1** Compact drawing showing all lithographic masks superimposed - the heat dissipating devices over the diagonal channels (top-left and bottom-left chips), 3 simple channels with different lengths (top-right and bottom-right chips)

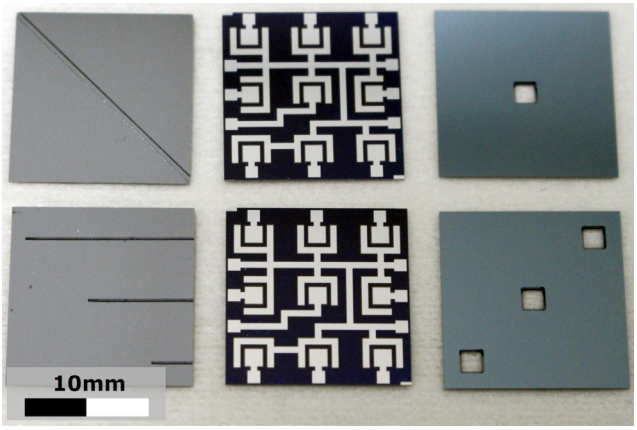


**Fig. 2** Finished devices from left to right: the front sides of the integrated devices containing the microscale channels; dissipating diodes (that can also be used for thermal testing); sealing parts with gas inlet for different channel patterns.

## 3 Numerical analysis and modelling

In Section 3 the investigation of the thermal behavior of the microscale heatsink structure by multi-domain simulation and modelling is presented. Some CFD simulations of different channel patterns were carried out and certain ones were selected and recommended for fabrication. The main aim of this segment of the development was to elaborate a compact model of the integrated microscale heatsink structure which can be used in the future in thermal / electro-thermal simulation tools. Another important issue was to acquire a behavior model which is useful for system-level analysis, virtual prototyping etc. It is also evident that the outcome of the compact modelling and the electro-thermal simulations was compared with the results of the characterization as well.

During the modelling and compact model generation tasks, the main aim was to create a ladder-type analytical thermal model for microscale channel based heatsink structures to determine the local heat transfer(s) and the temperature distribution along the channel(s) depending on the channel geometries, the thermal properties of the fluid and the wall temperature(s). However, the main difference between other solutions and our model is the fact that it deals with the hydrodynamic entry phenomenon and only includes analytical derivations.

During the model creation phase several consideration had to be made, since the resulting model have to be "simple" or compact enough to be used even in conventional electrical circuit simulator programs. However, the heat transfer and the temperature distribution along the channel cannot be described with one stage, preferably RC model. In addition, several non-linearities and multiphysical coupling effects are to be considered as well.

An essential step to gain a model was the division of the channel into several segments and for each segment a T-equivalent circuit is created. The ladder-type thermal model obtained by applying the T-equivalent subcircuit as a building block can be used as a compact model of microscale channel structures [17, 18, 24].

Several analytical or semi-empirical equations can be found in [25] to determine the average Nusselt number, which depends on the cross sectional geometry and the length of the channel These equations also deal with the hydrodynamic entry phenomenon, which describes the Nusselt number near the inlet, thus the heat transfer coefficient will be higher than the average Nusselt number of the whole channel.

If the $L$ long channel is divided into $n$ segments, then the length of one segment is $L_{segment} = L_{channel} / n$. The Nusselt number for each segment can be determined based on the following equation:

$$\mathrm{Nu}_{seg} = 5.14 + \frac{0.065 \cdot \left(D_H / L_{segment}\right) \cdot \mathrm{Re} \cdot \mathrm{Pr}}{1 + 0.04 \cdot \left[\left(D_H / L_{segment}\right) \cdot \mathrm{Re} \cdot \mathrm{Pr}\right]^{\frac{2}{3}}}, \tag{1}$$

where $D_H$ is the hydraulic diameter, Re and Pr are the Reynolds and the Prandtl number respectively.

The local Nusselt number calculation is mandatory to determine the $h$ heat transfer coefficient between the wall of the channel and the fluid. It can be calculated as presented in [25]:

$$h = \frac{k_f \cdot \mathrm{Nu}}{D_H}. \tag{2}$$

The constant number 5.14 in Eq. (1) represents the Nusselt number for the fully developed laminar flow, far from the hydrodynamic entry region (the mathematical limit of the function). Increasing the aspect ratio results in higher Nusselt number for the fully developed region, but the area reservation of one channel due to the increasing width results in less channel per unit area.

The $D_H$ hydraulic diameter can be determined for a square-based column as follows:

$$D_H = \frac{2 \cdot a \cdot b}{a + b}. \tag{3}$$

The Reynolds and Prandtl number can be calculated as:

$$\mathrm{Re} = \frac{D_H \cdot \frac{dm}{dt} \Big/ A}{\mu} = \frac{D_H \cdot \rho \cdot \frac{dV}{dt} \Big/ A}{\nu} = \frac{D_H \cdot \rho \cdot v}{\nu} \tag{4}$$

$$\mathrm{Pr} = \frac{C_p \cdot \nu}{k_f}, \tag{5}$$

where $v$ is the dynamic and the $\mu$ is the kinematic viscosity of the fluid, $\rho$ is the density of the fluid, $L$ is the length and $v$ is the mean velocity of the fluid.

If the channel is divided into parts with infinitesimal length, then the heat energy ($Q$) flows through one part ($dA$) per unit time will be:

$$dQ = h \cdot \left(T_w - T_f\right) \cdot dA = h \cdot \left(T_w - T_f\right) \cdot p \cdot dx, \tag{6}$$

where $dx$ means the infinitesimal length in the channel, $p$ is the perimeter, $T_w$ and $T_f$ are the temperature of the substrate and the actual average temperature of the fluid in the channel at the point of investigation respectively and $h$ is the local heat transfer coefficient.

Based on the conservation of energy the heat leaving the substrate will warm up the fluid as shown:

$$h \cdot \left(T_w - T_f\right) \cdot p \cdot dx = \frac{dm}{dt} \cdot C_p \cdot dT_f. \tag{7}$$

The rearrangement of Eq. (10) results:

$$\frac{1}{\left(T_w - T_f\right)} \cdot dT_f = \frac{h \cdot p}{\frac{dm}{dt} \cdot C_p} dx. \tag{8}$$

Based on the solution method of linear differential equations (variable separation) and performing the integration between $[0 \ldots L]$ where $L$ is the total length of the channel and between $[T_i \ldots T_e]$ where $T_i$ is the temperature of the fluid when it enters the specified region and $T_e$ is the mean temperature of the fluid when it leaves the $dx$ width part results:

$$\ln \frac{T_w - T_e}{T_w - T_i} = -\frac{h \cdot p \cdot L}{\frac{dm}{dt} \cdot C_p}, \tag{9}$$

where $p \cdot L$ is the total area of the channel walls where the heat transfer occurs.

The mean temperature of the fluid at the exit of the $k^{\text{th}}$ segment can be derived as:

$$T_{e_k} = T_{w_k} - \left(T_{w_k} - T_{i_k}\right) \cdot \exp\left(-\frac{h_k \cdot p_k \cdot L_k}{\frac{dm}{dt} \cdot C_p}\right). \tag{10}$$

The actual heat exchange per unit time within the $k^{\text{th}}$ segment can be determined:

$$dQ_k = \frac{\left(T_{w_k} - T_{i_k}\right)}{R_{th_cross_k}} = \frac{dm}{dt} \cdot c_p \cdot \left(T_{e_k} - T_{i_k}\right). \tag{11}$$

The temperature difference can be calculated between the inlet and the outlet of the $k^{\text{th}}$ segment based on Eq. (10).

$$T_{e_k} - T_{i_k} = \left(T_{w_k} - T_{i_k}\right)\left(1 - \exp\left(-\frac{h_k \cdot p_k \cdot L_k}{\frac{dm}{dt} \cdot C_p}\right)\right) \tag{12}$$

The $R_{th_cross_k}$ can be derived from Eqs. (11) and (12):

$$R_{th_cross_k} = \frac{1}{\frac{dm}{dt} \cdot c_p \cdot \left(1 - \exp\left(-\frac{h_k \cdot p_k \cdot L_k}{\frac{dm}{dt} \cdot C_p}\right)\right)}. \tag{13}$$

If constant Nusselt number is applied (e.g.: derived from the average Nusselt number of the whole length or determined at one selected point of the channel by numerical simulation) the $R_{th_cross_k}$ remains constant. If the hydrodynamic entry phenomenon is taken into account, the Nusselt number (thus also the heat transfer coefficient) is changing from segment to segment, hence the $R_{th_cross_k}$ value is changing as well.

Based on Eq. (12) the temperature difference calculation can be simplified and results in a *heat flow controlled temperature source*.

$$T_{e_k} - T_{i_k} = \frac{1}{\frac{dm}{dt} \cdot c_p} \cdot \frac{\left(T_{w_k} - T_{i_k}\right)}{R_{th_cross_k}} = \frac{1}{\frac{dm}{dt} \cdot c_p} \cdot \frac{dQ_k}{dt} \tag{14}$$

By applying Eqs. (11), (13), and (14) an equivalent circuit model can be created (Fig. 3) based on the analogy between the thermal and electrical systems. Kirchhoff's law clearly defines the connections of each element in thermal domain as well, even if the microscale channel is cut down into $k$ segments. The temperatures and the heat flow rates can be corresponded to the voltage and electrical current values respectively.

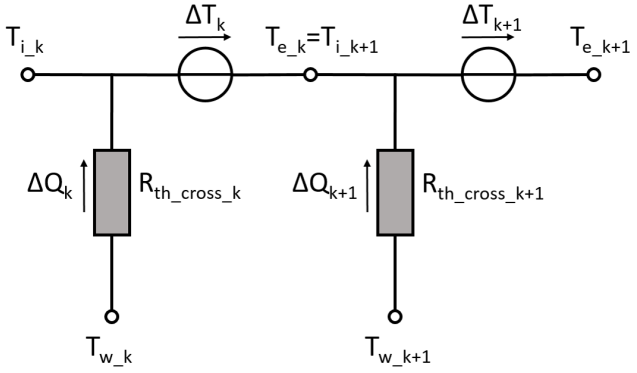


**Fig. 3** The proposed T-equivalent analytical thermal model of one channel (two neighbouring segments are depicted)

In each segment the $R_{th_cross_k}$ thermal resistance(s) can be calculated by utilizing Eqs. (13) and (14).

This model was implemented in a conventional thermal field solver (CTFS) simulation tool to augment the capability of simulating the thermal impact of integrated heat sink structures even with radial channel pattern (Fig. 4). The implementation steps and the results (Fig. 5) are compared to the analytically calculated, CFD modelled and to the measured values. This augmented CTFS engine gives the opportunity to investigate the operation of system-on-package (SoP) devices.

Our novel analytical fluid dynamics compact models can be used in logi- or electro-thermal simulation tools to determine the flow, pattern, fluid properties, etc. dependent local heat flux and the temperature distribution on the surface of the chip even in case of stacked-die structures. The new compact model can take the variable Nusselt-number (and the heat transfer coefficient) values along each channel into consideration. This number is very important in the proper, thermal aware placement of the dissipating elements (e.g.: high-power transistors, amplifier circuits, VCOs, CACHE, ALU components). A thermal simulator tool was extended with the presented compact models (Fig. 4) to make it eligible to accurately simulate the hydrodynamics phenomenon in a short time. This extended thermal simulator engine was connected to the logic simulator engine creating logi-thermal simulation capabilities. Nonetheless, this environment can provide insights to the temperature-dependent behavior of the circuit it can give additional details about dynamic thermal characteristics of the digital circuit.

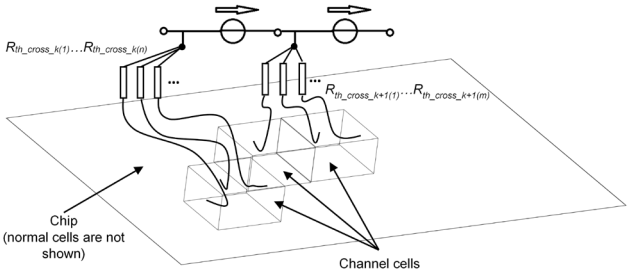


**Fig. 4** Channel model implemented as boundary condition for the SUNRED model

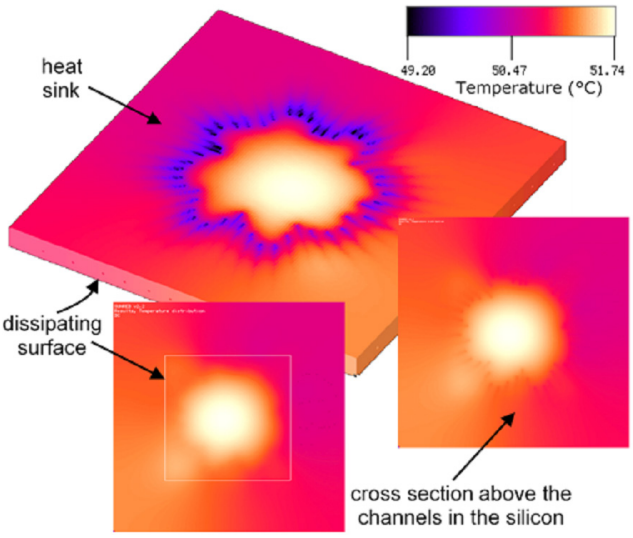


**Fig. 5** Temperature distributions from SUNRED simulation of the realized structure, volumetric flow rate = 120 l/h

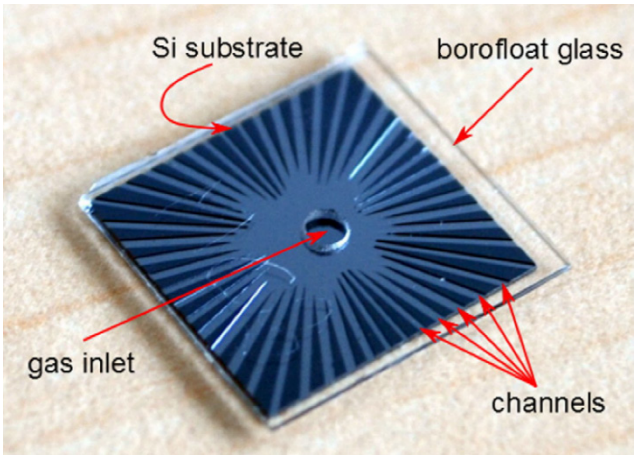


**Fig. 6** The first prototype of the microscale heat exchanger with radial channel pattern

## 4 Measurements and characterization

The 3rd large research activity focused on the characterization and verification of microchannel cooling structures. In the first phase, the development of a new measurement setup and support structure for thermal transient testing was done. The main goals were to measure the partial thermal impedance of the microchannel cooling structures with different build-ups and patterns and compare these results to the results of the simulation and modelling work presented in Section 3. In this way, a new multi-domain characterization method of different microfluidic channel based heat exchanger structure was created.

The first set of samples were manufactured with the microscale channels only, which means that no active device was realized on the top side of the wafer (Fig. 6). As a consequence, the thermal characterization of the foreseen cooling solution at this stage required the application of an external active device.

The thermal resistance was measured by attaching a high-power transistor acting as a heater and simultaneously a temperature sensor to one side of the structure,

and a cold-plate to the opposite side providing the proper thermal ground (Fig. 7). An advantage of thermal measurements on cold plate is that such a setup usually provides the shortest possible heat removal path and allows the quickest possible required characterization times. After powering up the transistor, its temperature rise has to be measured till thermal equilibrium and by knowing the applied power step and the temperature of cold plate, we can obtain the junction to ambient thermal resistance.

The junction temperature rise of the transistor can be measured using the principles published in [19]. The forward voltage of the emitter-base junction is a temperature sensitive parameter (TSP). Its sensitivity (or K-factor) has to be identified previously by a calibration process, using a relatively small sensor current (e.g. 1 mA). The $\Delta T_j$ junction temperature change must be measured between two steady-states.

The problem with this solution is that this overall thermal resistance also includes the heat loss paths. The method of obtaining the partial thermal resistance of the microchannel heat sink is identified with the help of the structure functions [17].

In order to obtain the structure function, thermal transient measurement has been carried out. The recorded thermal transient contains all available information about the 1D heat-conduction path. In our case this path starts at the junction of the power transistor and ends at the thermal ground (cold plate, micro-channel cooler).

The concept of extracting information from the thermal transient was already introduced several years ago and was described in a number of publications and standards [26-28].

The cumulative structure function is a direct map of the cumulative thermal capacitance vs. cumulative thermal resistance from the junction of the transistor to the cold plate [29]. Thus, the origin of the curve always corresponds to the junction of the transistor, and the function always ends with a singularity indicating the infinite thermal capacitance of the ambient. By applying the former measurement system, which eliminates numerous previously revealed measurement errors, the flow rate dependent partial thermal resistance ($R_{TH_MC}$) of the devices can be determined.

The flow rate of the cooling fluid was controlled by a digital mass flow control unit. As a result of the measurements we managed to determine the thermal resistances at different flow rates. These results are in good agreement with the analytical calculations and the CFD simulations.

In the following part of the research activity several additional, previously unexplored measurement error sources were identified and resolved. The main error source was caused by the outflowing of the heated-up fluid. Since the speed of the outlet gas was significant, it induced pressure difference in the surroundings which moved the air in the vicinity of the measurement structure. As a consequence, the moving air near the structure created a parallel heat flow, which generated a flow rate dependent convective heat exchange (Fig. 8) and tampered the measurement results.

Based on these, new results the measurement setup was refined (Fig. 9) and new measurements were carried out. The measured results were compared to the CFD simulation results and gave a very good correspondence, better then in case of the former results.

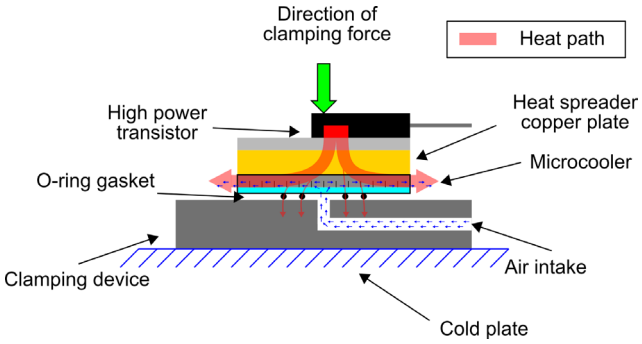


**Fig. 7** Cross-sectional view of the improved sample holder of the measurement setup

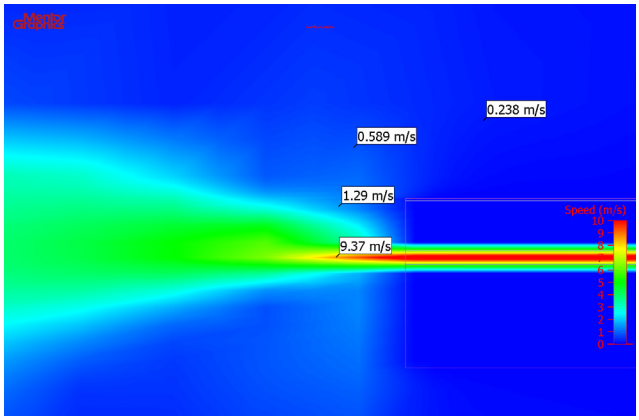


**Fig. 8** Air velocity map around the outlet of the sample holder

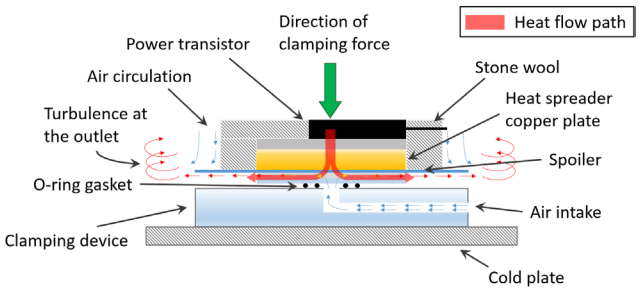


**Fig. 9** Cross-sectional view of the enhanced sample holder of the measurement setup

With the new measurement system, (Fig. 10) numerous measurement errors have been eliminated.

With this new measurement setup, the hydrodynamic and the thermal characterization for the new samples were carried out by using liquid and gas coolant, as well.

The determined partial thermal resistance values could have been compared with the results of the simulations and analytical calculations. The highest deviation was 8 % at 30 liters per hour but with increasing flowrates the measurement errors become lower, that is quite an outstanding in case of microscale thermo-hydrodynamic characterization.

In case of liquid coolant, an additional support structure is needed to ensure the liquid reaches the inlet of the channels, flows through the channel and is conducted towards the drain or heat exchanger.

In conclusion, it can be said that the elaborated enhanced characterization method is suitable to reduce parasitic physical effects which were not accounted for during the previous measurements. Furthermore, the validation of the setup with a CFD model became possible and the identified partial thermal resistance of the microchannel cooling devices can be defined accurately. This value is a good general overall thermal metric which can be used to compare different cooling solutions as well as it can be used as a compact model in system level thermal simulations.

## 5 Characterization of concentrated photovoltaic cells (CPV) and other applications

In the beginning of the research the applicability of cooling structures with integrated microscale channels in SoP structures were investigated. It was evident that first of all we concentrated much effort to advise integration possibilities since the successful integration would be a real breakthrough. It was found out that companies like IBM are also having difficulties with this step.

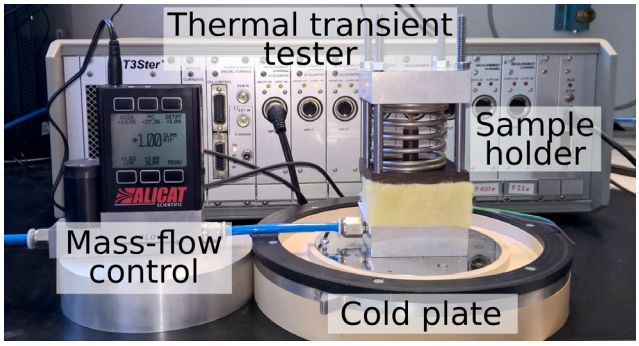


**Fig. 10** The enhanced measurement setup

The main problem with SoP structures is that different dies are stacked on each other forming a real 3D structure. Between the dies, high resistivity layers are formed to ensure electrical insulation. These layers also have high thermal resistivity and therefore the temperature elevation is higher beside the same dissipation.

One way to decrease the thermal resistance is to bring the cooling structures closer to the junction that is why it has to be realized inside the package. Some approaches include applications of integrated micro-refrigerators attached close to the hot-spot locations. Some papers present the method and the results of forming microscale channel structure inside the insulation layers [3]. In our approach, the microscale channel structure is realized inside the die itself which results lower thermal resistance between the active area and the case/ambient. Despite certain efforts the packaging technology is still under development, but several possibilities are envisioned.

It can be imagined that the elaborated characterization method, simulation engine and the manufacturing have numerous applicability. As it was described, we envision its usage in System-on-Package devices, stacked-die structures to decrease the thermal resistance of the primary heat flow path. Despite the fact that the first demonstrator SoP device which utilizes microscale heatsink structures is still in development, we have looked towards other areas to demonstrate the expedience of our method.

So as a consequence, during the last phase of the project the applicability and the realization possibilities of the integration of microscale channel based heat sink structures to the concentrated photovoltaic cells for integrated thermostating purpose were investigated (Fig. 11) [30].

Based on the results of Section 3, the maximum heat flux could have been estimated in case of different channel patterns and different types of coolant before the fabrication. The geometries (height, length of the channel, etc.) were optimized regarding to thermal and fabrication

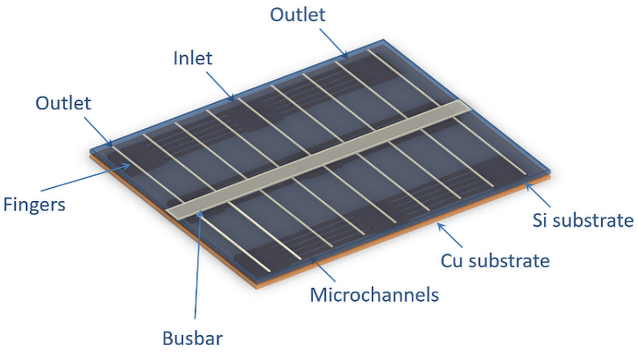


**Fig. 11** Visualization of the CPV cell

aspects. By applying water as a liquid coolant beside applying 1 bar pumping power the maximum achievable heat flux is calculated and simulated to be up to 300 W from a 5 cm × 5 cm area. The process steps were developed and the demonstrational sample was fabricated (Fig. 12).

In our concept, the microscale channels can be integrated into the back surface metallization. The microscale channels can be formed by electroplating copper around a photoresist channel pattern. This approach has the advantage that it has no restrictions regarding the solar cell material and technology. Our research team developed a detailed description on the process technology, performed mechanical simulations for the feasibility of our approach, optimized the channel geometry for a 20 × 20 mm concentrator solar cell and estimated the cooling performance of the microscale channel structure at different operating conditions. We found that the proposed cooling solution can be applicable. The characterization and the measurement of the samples are in progress.

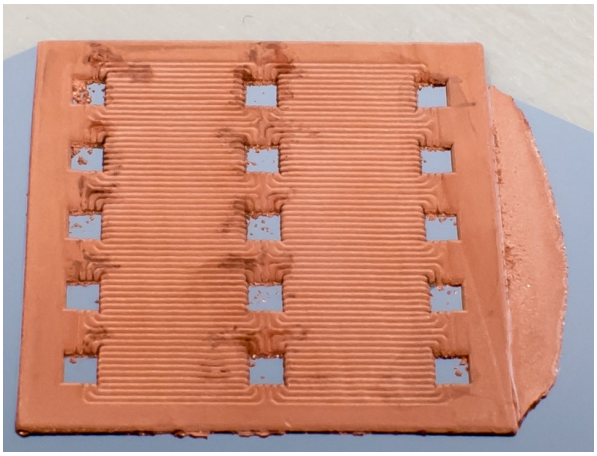

**Fig. 12** First CPV prototype

## 6 Conclusions

The main aim of our paper was to present the development of an integrated thermal management system to cool/thermostat semiconductor devices. Through forced convection and by realizing integrated microscale channel structures on the backside of the substrate of semiconductor devices, the cooling of active electronic devices was realized. The fabrication process technology to apply anisotropic etching steps was successfully set up and several structures were formed with different channel geometries and dimensions, realizing single, parallel and radial arrangement of them. The initial characterization steps based on thermal transient measuring at different working fluid flow rates were elaborated and carried out and the overall measuring system was fine-tuned to realize a valid, repeatable characterization method by eliminating several secondary error sources. In order to validate the measurement results CFD modelling and simulation was accomplished and based on these results an analytical based modelling methodology was developed and a complete modelling tool was created to determine hydrodynamic and thermal properties of the channels. A new analytical formula was founded to determine the exact heat resistance value between the wall of the channels and the ambient. In the last phase of the research, we focused on the cooling of concentrated PV cells by realizing channel structures within the backside metallization. The technology has been elaborated and the thermal models were created.

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