343

A Low Quantum Cost Implementation of Reversible Binary-Coded-Decimal Adder

Sheba Diamond Thabah[1], Prabir Saha[1*]

[1] Department of Electronics and Communication Engineering, National Institute of Technology Meghalaya, Bijni Complex, Laitumkhrah, Shillong, 793003 Meghalaya, Upland Road, India
[*] Corresponding author, e-mail: prabir.saha@nitm.ac.in

Abstract

The prediction and forthcoming of a quantum computer into the real-world is the much gained research area over the last decades, which initiated the usefulness and profit of reversible computation because of its potentiality to reduce power consumption in designing arithmetic circuits. In this paper, two design approaches are proposed for the design of a reversible Binary-Coded-Decimal adder. The first approach is implemented and realized from reversible gates proposed by researchers in the technical literature capable of breaking down into primitive quantum gates, whereas the second approach is realized from the existing synthesizable reversible gates only. Parallel implementations of such circuits have been carried out through the proper selection and arrangements of the gates to improve the reversible performance parameters. The proposed design approaches offer a low quantum cost along-with lower delay and hardware complexity for any *n*-digit addition. Analysis results of proposed design 1 show appreciable improvements over gate count, quantum cost, and delay by at least 9 %, 17 %, and 26 % respectively, whereas, the proposed design 2 show that the results significantly improve the parameters (gate count, quantum cost, and delay) by at least 45 %, 33 %, and 50 % respectively compared to existing counterparts found in the literature.

Keywords

Binary-Coded-Decimal (BCD), delay, quantum cost, primitive quantum gates, hardware complexity

1 Introduction

Decimal arithmetic circuits have a wide application in commercial, financial, and internet-based systems, and the design of such circuits with low power consumption is a challenging task for researchers. Over the last decades, designers realize the circuits that are capable of reducing the power loss with the help of the advanced level of integration or new fabrication methodologies. Long back, Landauer [1] stated that logic computation through classical gates has information loss, i.e., for each bit loss, at least *KTln2* joules of energy or heat loss occurs during the transition, where *K* is known as Boltzmann's constant and *T* is the absolute temperature. For larger circuits, the energy loss is proportional to the number of Gate Count (GC), i.e., number of bits/digits. However, Bennett [2] proved that removal of such energy loss is possible with the help of the reversible mechanism, which leads to the use of reversible logic gates. The inherent properties of such reversible circuits are the same number of input and output vectors along-with unique mapping styles between them, and

input vectors must be able to obtain uniquely from the output vectors [3, 4]. Besides that, fan-out and feedback are the limitations in reversible logic computation. However, a Feynman reversible gate is the solution for the fan-out problem (used as copying circuits).

On the other hand, the hardware implementation of the decimal arithmetic circuits has some limitations like precisions [5], delay and power, from its counterpart. Thereby, low power and high-speed hardware realization of such decimal arithmetic circuits have a significant impact on the present time.

Numerous approaches [6–12] have been proposed for the design of reversible Binary-Coded-Decimal (BCD) adder, where, synthesizable reversible gates (such as Feynman Gate (FG) [13], Toffoli Gate (TG) [14], Peres Gate (PG) [15], and Fredkin Gate (FRG) [16]) and non-synthesizable reversible gates (such as New Gate (NG), TSG gate, HNG gate, HNFG gate, Peres Full-Adder Gate (PFAG), TR gate, Negative Controlled Toffoli (NCT)

gate, and BJN gate) are utilized in realizing the designs. The previous approaches listed in this paper for the reversible implementation of BCD adder realized and designed with higher GC and Quantum Cost (QC) values, where it indirectly leads to higher delay. So, the main motive in this paper is to realize the same with lower GC and QC values, which further reduce the delay in the circuit.

Therefore, in this paper, two novel approaches for the reversible implementation of BCD adder are proposed. The first approach has implemented through existing synthesizable reversible gates combined together with some non-synthesizable reversible gates that researchers have proposed capable of breaking down into Primitive-Quantum-Gates (PQGs). The second approach has implemented through the existing synthesizable reversible gates only. Also, the proposed approaches generalized for the n-digit addition. The proposed approaches offer the critical path delay reductions of at least ~26 % simultaneously with lower hardware complexity. Moreover, the QC and GC exhibit improvement of at least ~17 % and ~9 %, respectively, compared to the state-of-art designs found in the literature.

2 Binary-Coded-Decimal adder

BCD adder is one of the computer arithmetic circuits that perform the addition of two BCD numbers. There are mainly three parts in the BCD adder circuit, as shown in Fig. 1, i.e.:

- the first adder,
- the Six-Correction-Logic (SCL), and
- the second adder.

The first adder (4-bit binary adder) executes the addition of the two BCD numbers in binary format, and the result of the addition is then checked by the SCL using Eq. (1). If the result is higher than "1001" or there is a carry generated, then the result is wrong (i.e., when $Y = 1$) and has to be corrected. The correction is carried out by the

second 4-bit binary adder, where the addition of "0110" adds up the result of the first adder. However, if the result is correct (i.e., when $Y = 0$), then no addition is performed in the second adder. The BCD adder in Fig. 1 is realizable for any n-digit addition by only cascading it into n-blocks.

$$Y = C_4 + S_3 (S_1 + S_2) \qquad (1)$$

3 Proposed design approaches for reversible Binary-Coded-Decimal adder
3.1 Design 1
In this approach, the reversible Full-Adder (FA) is realized using one HNG, as shown in Fig. 2, where the three inputs of the FA (i.e., A, B, and Cin) supplied to the first three inputs of the HNG with the fourth input supplied with a constant 0. The outputs (Cout and Sum) of FA positioned in the third and fourth output of HNG with two garbage outputs (GOs) G1 and G2. Reversible implementation of an n-bit parallel adder is achievable using a reversible FA (shown in Fig. 2) by cascading into n blocks. Therefore, a reversible 4-bit binary adder is realized using four reversible full-adders (FAs)/four HNG gates (holding four constant inputs (CIs) and eight GOs), as shown in Fig. 3. For the SCL implementation, two reversible gates, namely, BJN and TG, are applied (with only one constant input (CI) and four GOs), as shown in Fig. 4. The complete circuit realization of the reversible BCD adder shown in Fig. 5, where the circuit has GC, CI, and garbage output (GO) of 10 (8 HNG + 1 BJN + 1 TG), 11 and 16, respectively.

3.2 Design 2
The reversible realization of FA utilized two PG with one CI and two GOs, as shown in Fig. 6, where, A, B, and Cin are the inputs, whereas Sum and Cout are the outputs. Also, this reversible FA (in Fig. 6) is possible to realize an n-bit reversible parallel adder. Now, since a 4-bit binary
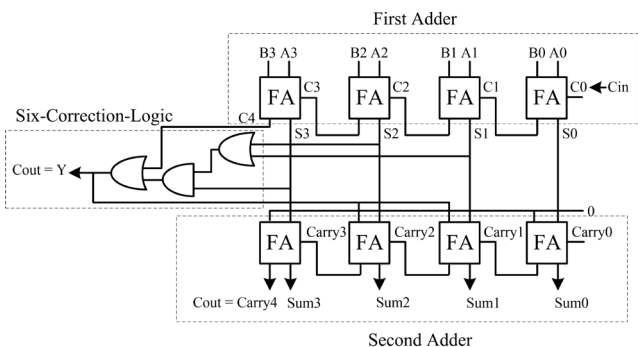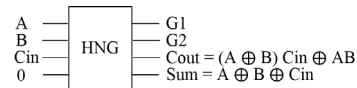

Fig. 2 Reversible full-adder using HNG
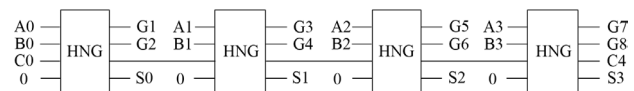
Fig. 3 Reversible 4-bit binary adder using HNG
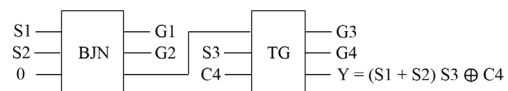
Fig. 4 Reversible Six-Correction-Logic using BJN and TG

Fig. 1 Binary-Coded-Decimal adder (for 1-digit)
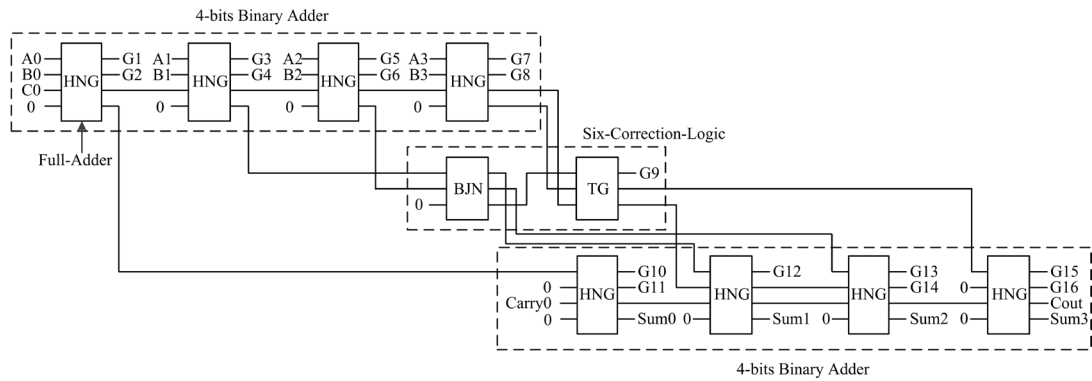
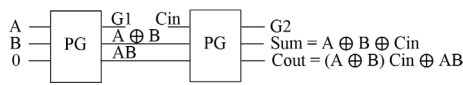**Fig. 5** Reversible BCD adder implementation of proposed design 1

Fig. 6 Reversible full-adder using PG

adder implemented from four FA; therefore, eight PG gates are required for the same as shown in Fig. 7 (with four CIs and eight GOs). For the reversible SCL (Fig. 8), two reversible gates, namely, FRG and TG, are used for the implementation of the function (holding one CI and four GOs). The complete realization of the reversible BCD adder is shown in Fig. 9, where the CI and GO are 12 and 17, respectively. With one extra gate of FG for copying purposes, the total GC required for the complete realization is 19 (16 PG + 1 FG + 1 FRG + 1 TG).

Furthermore, the implementation for any *n*-digit addition is possible using both (design 1 and design 2) designs by cascading it into *n* blocks.

4 Results, performance analysis, and discussions
Table 1 gives the calculation values of the QC, TLC, depth, and delay together with the Equivalent-Quantum-Circuit (EQC) of the reversible gates used in our designs and the previous designs [6–12]. Both the proposed
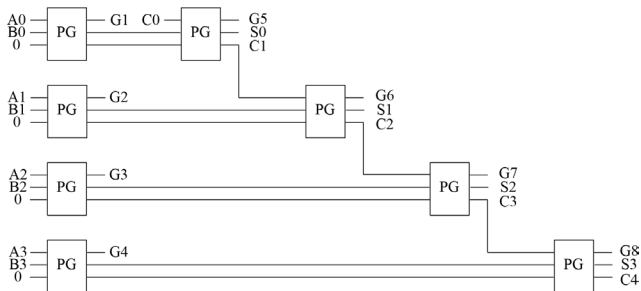

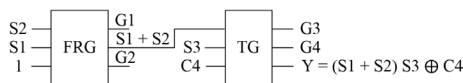**Fig. 7** Reversible 4-bit binary adder using PG

Fig. 8 Reversible Six-Correction-Logic using FRG and TG

approaches of the reversible BCD adder are verified using the RCViewer+ tool and the performance parameters such as GC, CI, GO, QC, delay, and TLC summarized in Table 2. The performance of the proposed designs compared with the existing designs found in the literature shown in Table 3. The existing designs in [6–11] utilized synthesizable reversible gates together with other reversible gates (not yet synthesizable) available in the literature and are compared with the proposed design 1. In contrast, the existing design in [12] employed only synthesizable reversible gates and is compared with proposed design 2. The GC, CI, GO, QC, delay, and TLC metrics among the compared designs analyzed in Sub-sections 4.1 to 4.6.

4.1 Gate count
From Table 3, the GC of the existing designs [6–11] is 23, 11, 23, 14, 36, and 14, respectively, and the proposed design 1 reduced the GC to 10 only. Again in [12], the design has a GC of 35, whereas the proposed design 2 significantly reduces the GC to 19. Comparing with the existing designs [6–11], the proposed design 1 has a reduction of at least 9.09 %, whereas, when compared with design [12], the proposed design 2 shows a significant reduction of 45.71 %.

4.2 Constant input
The numbers of CIs incorporated by the set of existing designs [6–9, 11] are 17, 12, 13, and 19, respectively. The design in [10] includes only one CI for the reversible implementation of BCD adder but making use of 36 gates, which is enormous compared to the other existing designs. Also, with the increasing of digits, the number of gates employed becomes additionally huge, as shown in Table 3. The design approach in [12] involves 13 number of CI, where, the proposed design 2 lessens the number of CI by 1 unit. As seen in Table 3, the proposed designs show a slight reduction of CI over the existing designs [6–9, 11, 12] found in the literature.
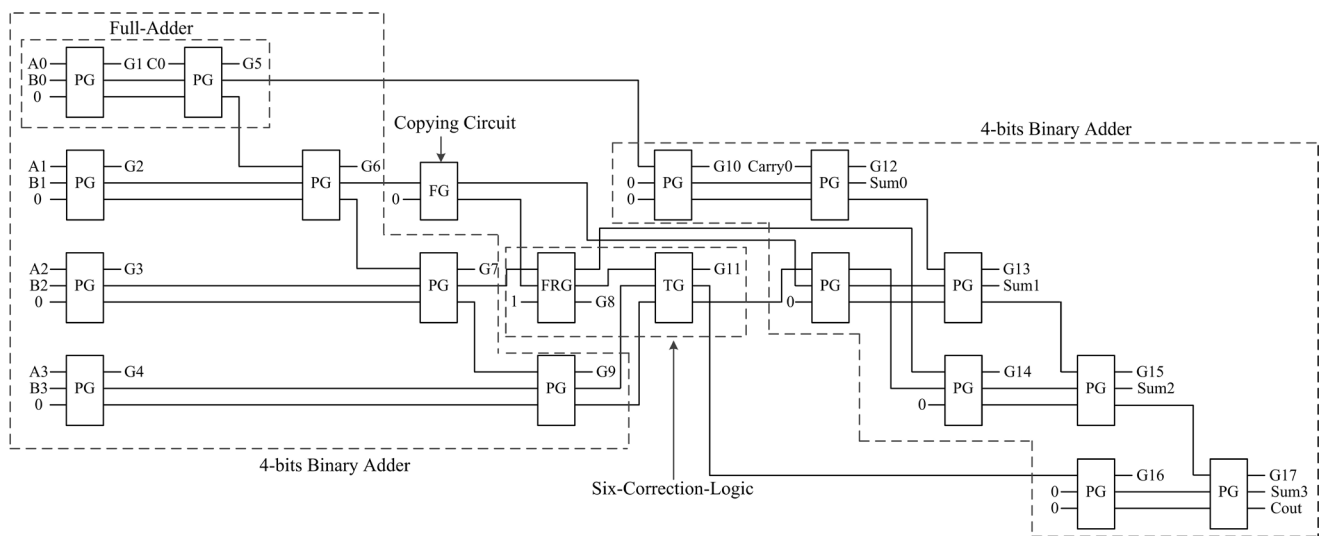
Fig. 9 Reversible BCD adder implementation of proposed design 2

4.3 Garbage output

The set of existing designs [6–9, 11, 12] gives rise to 22 and 24 numbers of GOs. The design in [10] generates only 5 GOs but compromising other performance parameters like GC of 36, which is significantly large when compared to the existing designs. The proposed design 1 and design 2 produce GO values of 16 and 17, respectively. As seen in Table 3, the proposed designs show appreciable improvements in reducing the GO when compared to the existing designs found in the literature, excluding design in [10].

4.4 Quantum cost

The QC of a reversible circuit is quantified by the total number of the PQGs (which includes NOT, CNOT, V, and $V^\dagger$ gates [17, 18]) used in realizing a circuit, and each is realized to be 1. However, when there is a successive combination of a CNOT gate with a $V/V^\dagger$/CNOT gate in the same line of operation, these two PQGs are considered as one gate only and have a unit QC and also a unit delay. In Table 1, the dotted rectangular box represents the combination of a CNOT gate with a $V/V^\dagger$/CNOT gate. For example, in the case of FRG (in Table 1), two dotted rectangular boxes are present, which constitute a total of five quantum gates. Thus, the QC of FRG is 5. Similarly, the other reversible gates listed in Table 1 computed in the same means with the help of EQC.

From Table 3, the evaluated QC values of the existing designs [6–11] are found to be 157, 137, 140, 81, 70, and 88, respectively. The first proposal makes use of 58 PQGs, which display a reduction of 63.06 %, 57.66 %, 58.57 %, 28.39 %, 17.14 %, and 34.09 %, respectively when compared with the existing designs [6–11] found in the literature.

Also, the design in [12] holds a QC value of 113, whereas the proposed design 2 narrowed the QC value to 75 with a substantial reduction of 33.63 %.

4.5 Delay

Mohammadi and Eshghi [18] proposed that delay of a reversible circuit is analyzed from the logical depth and the Critical-Delay-Path (CDP) of the circuit when implemented from the PQGs, and each PQGs are known to have a unit delay, called Δ. However, the target input (second input) of a $V^\dagger$ gate has a delay of 2Δ. The logical depth of a reversible gate is the total number of the PQGs involved in building it. With the concept of logical depth, the CDP of the reversible circuit further analyzed. The calculated CDP is the maximum delay in the input-to-output lines of operation in the reversible gates. For example, in the case of PG (from Table 1), there are three lines of operation where the logical depth of the first, second, and third lines is 2, 3, and 3, respectively. Now, the CDP/delay is calculated using the knowledge of the logical depth. In the first line and second line of operation (of PG gate from Table 1), each of the quantum gates has a unit delay results in 2Δ and 3Δ delay, respectively. However, in the third line of operation, the first and second V gate has each of a unit delay, whereas, the third target input of a $V^\dagger$ gate has a delay of 2Δ, which summed up to a total delay of 4Δ. Therefore, the delay of PG is 4Δ (maximum delay from the input-to-output of the gate). The rest of the reversible gates delays are calculated in the same course of action and reported, as shown in Table 1.

From Fig. 5, the proposed design 1 goes through eight gate levels to complete the required function of the circuit. In the first to third level, an HNG gate is present, each

Table 1 Reversible gates with QC, TLC, depth, and delay calculations

Reversible gates	Parameters	Equivalent-Quantum-Circuit
1. FG $P = A$ $Q = A \oplus B$	QC = 1 TLC = 1α Depth = 1 Delay = 1Δ	
2. TG $P = A$ $Q = B$ $R = AB \oplus C$	QC = 5 TLC = $1\alpha + 1\beta$ Depth = 5 Delay = 4Δ	
3. PG $P = A$ $Q = A \oplus B$ $R = AB \oplus C$	QC = 4 TLC = $2\alpha + 1\beta$ Depth = 4 Delay = 4Δ	
4. FRG $P = A$ $Q = \bar{A}B \oplus AC$ $R = AB \oplus \bar{A}C$	QC = 5 TLC = $2\alpha + 4\beta + 1\delta$ Depth = 5 Delay = 4Δ	
5. NG $P = A$ $Q = AB \oplus C$ $R = \bar{A}C \oplus \bar{B}$	QC = 11 TLC = $2\alpha + 2\beta + 3\delta$ Depth = 11 Delay = 9Δ	
6. TSG $P = A$ $Q = \bar{A}\bar{C} \oplus \bar{B}$ $R = (\bar{A}\bar{C} \oplus \bar{B}) \oplus D$ $S = (\bar{A}\bar{C} \oplus \bar{B})D \oplus AB \oplus C$	QC = 13 TLC = $4\alpha + 3\beta + 3\delta$ Depth = 13 Delay = 8Δ	
7. HNG $P = A$ $Q = B$ $R = A \oplus B \oplus C$ $S = (A \oplus B)C \oplus AB \oplus D$	QC = 6 TLC = $4\alpha + 2\beta$ Depth = 6 Delay = 5Δ	
8. HNFG $P = A$ $Q = A \oplus C$ $R = B$ $S = B \oplus D$	QC = 4 TLC = 2α Depth = 4 Delay = 3Δ	
9. PFAG $P = A$ $Q = A \oplus B$ $R = A \oplus B \oplus C$ $S = (A \oplus B)C \oplus AB \oplus D$	QC = 8 TLC = $4\alpha + 2\beta$ Depth = 8 Delay = 8Δ	
10. TR $P = A$ $Q = A \oplus B$ $R = A\bar{B} \oplus C$	QC = 4 TLC = $2\alpha + 1\beta + 1\delta$ Depth = 4 Delay = 4Δ	
11. NCT $P = A$ $Q = B$ $R = \bar{A}\bar{B} \oplus C$	QC = 5 TLC = $1\alpha + 1\beta + 2\delta$ Depth = 5 Delay = 5Δ	
12. BJN $P = A$ $Q = B$ $R = (A + B) \oplus C$	QC = 5 TLC = 2α Depth = 5 Delay = 4Δ	

Note: α = A two-input EXOR gate calculation, β = A two-input AND gate calculation, δ = A NOT gate calculation, and Δ = A unit delay.

Table 2 Analysis results of the proposed design approaches of reversible BCD adder

Designs	Parameters	First Adder (a)	Six-Correction-Logic (SCL) (b)	Second Adder (c)	Copying Circuit (d)	Total = (a + b + c + d)
Proposed design 1 (for 1-digit addition)	GC	4(4HNG)	2(1BJN, 1TG)	4(4HNG)		10
	CI	4	1	6		11
	GO	8	1	7		16
	QC	24	10	24	-	58
	Delay	20Δ	9Δ	20Δ		40Δ
	TLC	$16\alpha + 8\beta$	$3\alpha + 1\beta$	$16\alpha + 8\beta$		$35\alpha + 17\beta$
Proposed design 2 (for 1-digit addition)	GC	8(8PG)	2(1FRG, 1TG)	8(8PG)	1(1FG)	19
	CI	4	1	6	1	12
	GO	8	2	7	0	17
	QC	32	10	32	1	75
	Delay	20Δ	8Δ	20Δ	1Δ	40Δ
	TLC	$16\alpha + 8\beta$	$3\alpha + 5\beta + 1\delta$	$16\alpha + 8\beta$	1α	$36\alpha + 21\beta + 1\delta$

Table 3 Comparison analysis of reversible BCD adder (for 1-digit addition)

Designs		GC	CI	GO	QC	Delay	TLC
[6]		23	17	22	157	64Δ	$42\alpha + 30\beta + 33\delta = 105$
[7]		11	12	22	137	83Δ	$38\alpha + 30\beta + 33\delta = 101$
[8]		23	13	22	140	63Δ	$39\alpha + 27\beta + 24\delta = 90$
[9]		14	17	22	81	54Δ	$41\alpha + 21\beta + 6\delta = 68$
[10]		36	1	5	70	57Δ	$36\alpha + 10\beta + 9\delta = 55$
[11]	Design 1	15	19	24	88	70Δ	$46\alpha + 21\beta = 67$
	Design 2	14	19	24	90	70Δ	$46\alpha + 21\beta = 67$
Proposed	Design 1	10	11	16	58	40Δ	$35\alpha + 17\beta = 52$
[12]		35	13	24	113	80Δ	$35\alpha + 19\beta + 4\delta = 58$
Proposed	Design 2	19	12	17	75	40Δ	$36\alpha + 21\beta + 1\delta = 58$

having a delay of 5Δ. In the fourth level, two gates (HNG and BJN) are in parallel with a maximum delay of 5Δ (considering the maximum delay of the two gates, which is of HNG gate). Also, in the fifth level, two gates (TG and HNG) are concurrent with a maximum delay of 5Δ. The last three (that is, sixth, seventh, and eighth) levels possessed each of an HNG gate, with each having delays of 5Δ. In total, the proposed design 1 has a delay of 40Δ. With the same conception, the delay of the proposed design 2 is calculated and found to be 40Δ. Also, the CDP of the existing designs is computed and recorded, as shown in Table 3. The proposed design 1 shows an appreciable reduction of 37.50 %, 51.80 %, 36.50 %, 25.92 %, 29.82 %, and 42.85 % over the delay variable when differentiating with existing counterparts [6–11]. However, the proposed design 2 exhibits a total reduction of half the delay times when contrasting with existing design [12] found in the technical literature.

4.6 Total Logical Calculation
The hardware complexity is calculated by the Total Logical Calculation (TLC), where, it is the total number of the classical gates to realize a given reversible circuits.

From Table 3 it is noticed that the total TLC values of the existing designs [6–12] happens to be 105, 101, 90, 68, 55, and 67 respectively, whereas, the proposed design 1 acquired only 52 classical gates to achieve the determined circuit, which reveals a slight reduction of TLC limit by only 5 % when compared with design [10]. In contrast, it shows an appreciable reduction of 50.47 %, 48.51 %, 42.22 %, 23.53 %, and 22.38 %, respectively, when compared with the other counterparts [6–9, 11] found in the literature. However, the proposed design 2 used an equivalent number of classical gates when compared with the existing design [12].

Also, using the RCViewer+ tool, the proposed designs are mapped into EQC, as shown in Fig. 10 (for design 1) and Fig. 11 (for design 2), respectively. In Fig. 10, the outputs of the reversible BCD adder displayed as Cout = Carry0, Sum3 = Z11, Sum2 = Z9, Sum1 = Z8, Sum0 = Z7, and in Fig. 11 displayed as Cout = Z12, Sum3 = Z11, Sum2 = Z4, Sum1 = B1, Sum0 = Z7, respectively. For any n-digit, the improvements are consistent since the production of the performance results straightforwardly multiplied by n times.
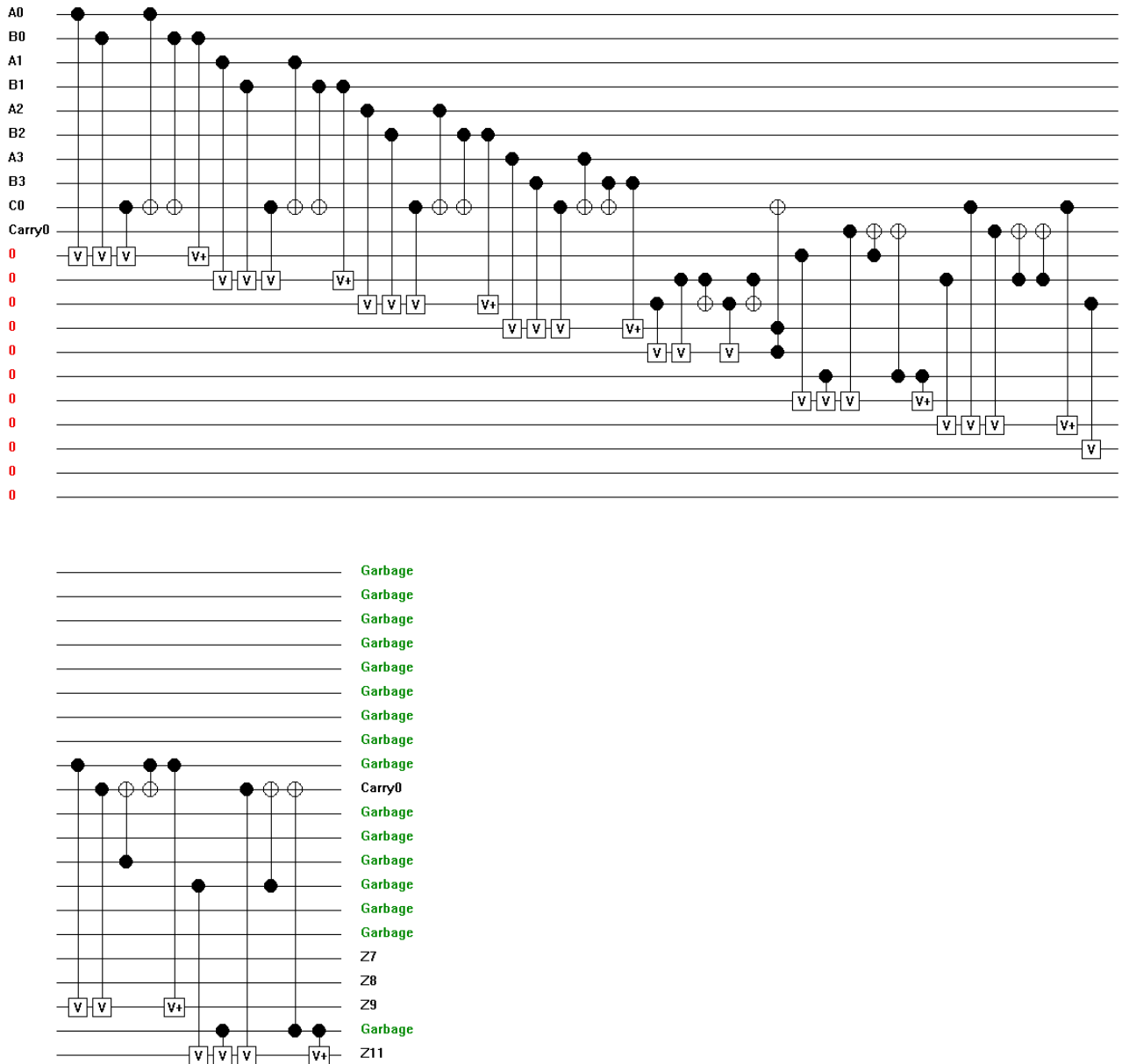
Fig. 10 Equivalent-Quantum-Circuit of proposed design 1

5 Conclusion

In this paper, two design approaches of reversible BCD adder are proposed where it disclosed improvements over GC, QC, delay, and TLC. Also, the proposed designs offer less hardware complexity with lower delay and QC compared to the existing designs found in the literature.

With the actuality of quantum computers to be constructed and build from reversible components and circuits, the reversible BCD adders are the encouraging and welcoming step towards the realization and implementation of larger reversible systems.
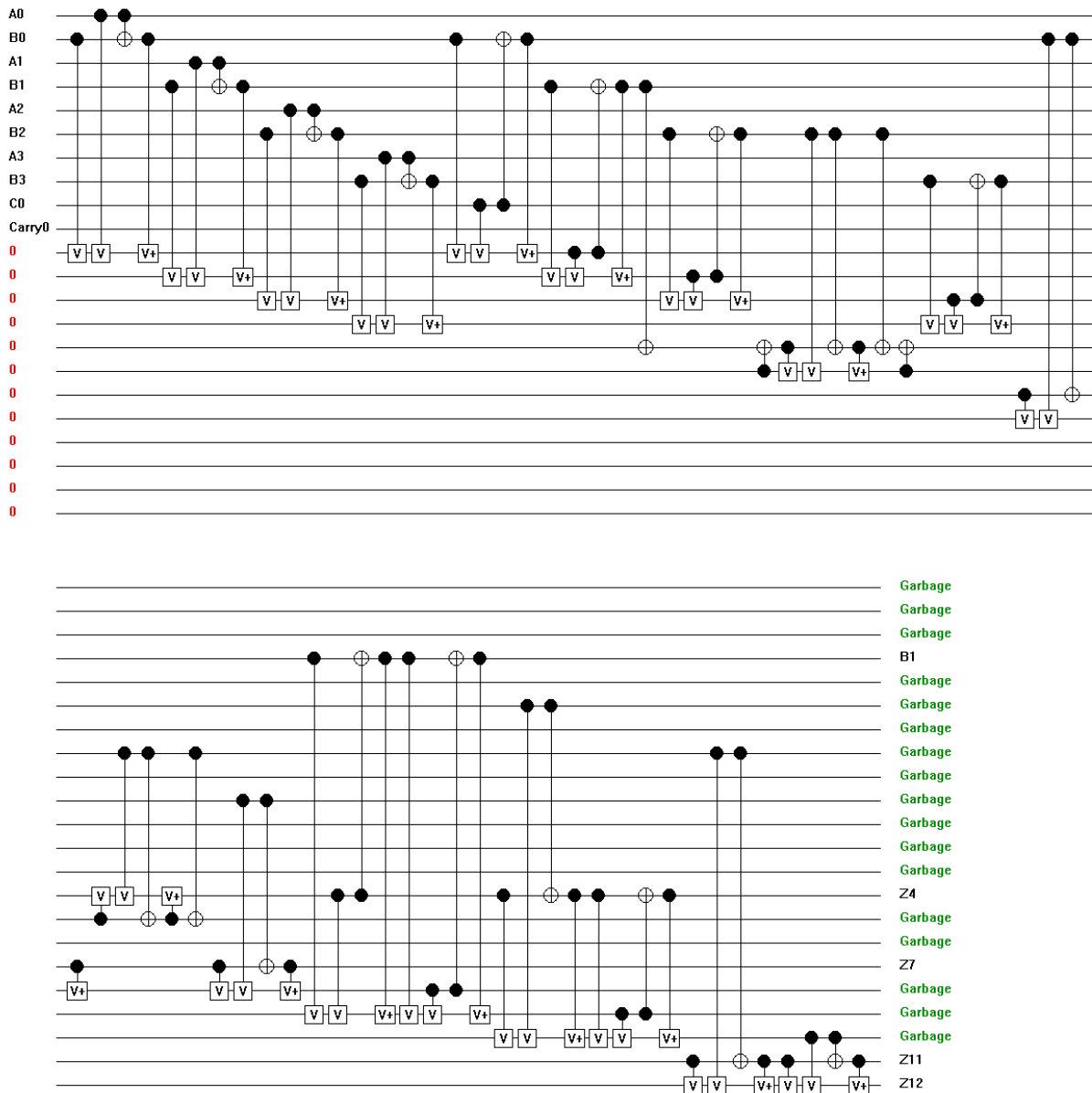
Fig. 11 Equivalent-Quantum-Circuit of proposed design 2

References

[1] Landauer, R. "Irreversibility and Heat Generation in the Computing Process", IBM Journal of Research and Development, 5(3), pp. 183–191, 1961.
https://doi.org/10.1147/rd.53.0183

[2] Bennett, C. H. "Logical Reversibility of Computation", IBM Journal of Research and Development, 17(6), pp. 525–532, 1973.
https://doi.org/10.1147/rd.176.0525

[3] Perkowski, M., Jozwiak, L., Kerntopf, P., Mishchenko, A., Al-Rabadi, A., Coppola, A., Buller, A., Song, X., Khan, M. H. A., Yanushkevich, S. N., Shmerko, V. P., Chrzanowska-Jeske, M. "A General Decomposition for Reversible Logic", In: Proceedings Reed-Muller Workshop, Starkville, MS, USA, 2001. [online] Available at: https://pdxscholar.library.pdx.edu/cgi/viewcontent.cgi?article=1198&context=ece_fac [Accessed: 16 November 2018]

[4] Thapliyal, H., Srinivas, M. B. "A Novel Reversible TSG Gate and Its Application for Designing Reversible Carry Look-Ahead Adder and Other Adder Architectures", In: Srikanthan, T., Xue, J., Chang, C.-H. (eds.) Advances in Computer Systems Architecture (ACSAC 2005), Lecture Notes in Computer Science, Springer, Berlin, Heidelberg, Germany, 2005, pp. 805–817.
https://doi.org/10.1007/11572961_66

[5] Hayes, J. P. "Computer Architecture and Organization", In: McGraw-Hill, New York, NY, USA, 1998.

[6] Babu, H. M. H., Chowdhury, A. R. "Design of a reversible binary coded decimal adder by using reversible 4-bit parallel adder", In: 18th International Conference on VLSI Design, Kolkata, India, 2005, pp. 255–260.
https://doi.org/10.1109/ICVD.2005.74

[7] Thapliyal, H., Kotiyal, S., Srinivas, M. B. "Novel BCD adders and their reversible logic implementation for IEEE 754r format", In: 19th International Conference on VLSI Design held jointly with 5th International Conference on Embedded Systems Design (VLSID'06), Hyderabad, India, 2006.
https://doi.org/10.1109/VLSID.2006.122

[8] Babu, H. M. H., Chowdhury, A. R. "Design of a compact reversible binary coded decimal adder circuit", Journal of Systems Architecture, 52(5), pp. 272–282, 2006.
https://doi.org/10.1016/j.sysarc.2005.05.005

[9] Haghparast, M., Navi, K. "A Novel Reversible BCD Adder For Nanotechnology-Based Systems", American Journal of Applied Sciences, 5(3), pp. 282–288, 2008.
https://doi.org/10.3844/ajassp.2008.282.288

[10] Thapliyal, H., Ranganathan, N. "A new reversible design of BCD adder", In: 2011 Design, Automation & Test in Europe, Grenoble, France, 2011, pp. 1–4.
https://doi.org/10.1109/DATE.2011.5763308

[11] Islam, M. S., Hafiz, M. Z., Begum, Z. "Quantum Cost Efficient Reversible BCD Adder for Nanotechnology-Based Systems", International Journal of Computer and Electrical Engineering (IJCEE), 4(1), pp. 10–13, 2012.
https://doi.org/10.7763/IJCEE.2012.V4.443

[12] Nagamani, A. N., Ashwin, S., Agrawal, V. K. "Design of optimized reversible Binary and BCD adders", In: 2015 International Conference on VLSI Systems, Architecture, Technology, and Applications (VLSI-SATA), Bangalore, India, 2015, pp. 1–5.
https://doi.org/10.1109/VLSI-SATA.2015.7050488

[13] Feynman, R. "Quantum mechanical computers", Foundations of Physics, 16(6), pp. 507–531, 1986.
https://doi.org/10.1007/BF01886518

[14] Toffoli, T. "Reversible Computing", Laboratory for Computer Science, Massachusetts Institute of Technology (MIT), Cambridge, MA, USA, Rep. MIT/LCS/TM-151, 1980.
https://doi.org/10.21236/ADA082021

[15] Peres, A. "Reversible logic and quantum computers", Physical Review A, 32(6), pp. 3266–3276, 1985.
https://doi.org/10.1103/PhysRevA.32.3266

[16] Fredkin, E., Toffoli, T. "Conservative logic", International Journal of Theoretical Physics, 21(3), pp. 219–253, 1982.
https://doi.org/10.1007/BF01857727

[17] Nielsen, M. A., Chuang, I. L. "Quantum Computation and Quantum Information", Cambridge University Press, New York, NY, USA, 2010.

[18] Mohammadi, M., Eshghi, M. "On figures of merit in reversible and quantum logic designs", Quantum Information Processing, 8(4), pp. 297–318, 2009.
https://doi.org/10.1007/s11128-009-0106-0