Periodica Polytechnica Electrical Engineering and Computer Science, 64(4), pp. 382–391, 2020

FOPID Controller Design and Implementation for High Gain Quadratic Boost Switched Capacitor Converter

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Received: 20 February 2020, Accepted: 17 May 2020, Published online: 08 October 2020

Abstract

In Solar panel and UPS, high gain DC-DC converters are commonly used. In grid connected inverter specifications, the batteries and solar panel voltage level are low. The use of multiple series related DC batteries and PV panels directly connected to the inverter, it simplifies the process, but the expense is high, and efficiency is low. A high-gain Quadratic Boost Switched Capacitor Converter is proposed in this paper. The high step up voltage gain is achieved by adding the voltage multiplier topology in the conventional quadratic boost converter with the correct duty ratio. The fractional order controller is implemented, and it's tuned by genetic algorithm optimization method for improving the performance of the proposed converter. Its characteristics are low energy processing, robustness and balanced voltage of cells. The performed that include the proposal and existing solutions, the theoretical results are verified from MATLAB/SIMULINK toolbox.

Keywords

Quadratic Boost Switched Capacitor Converter (QBSCC), fractional order PID controller, high gain, transient analysis, steady state analysis, genetic algorithm

1 Introduction

In recent years, PV systems, fuel cell, wind energy and more energy applications are developed to address the global energy shortage issues [1, 2]. Fuel cell generating system provides electric power normally in the range of 6 V to 48 V, which is not appropriate for high voltage applications. Some high gain DC-DC converters are used to boost up the voltage in the range of 200/400 V DC, further it is converter to AC voltage by DC-AC inverter for grid connected applications shown in Fig. 1.

The isolated DC–DC converter provides high gain DC voltage by adjusting the turn's ratio of transformer and regenerating technique are employed by clamping the voltage [3–5]. Non-isolated DC-DC converters are attracted



Fig. 1 Fuel cell power generation system

by low and medium power applications because of its advantage like simplicity, low cost and improved efficiency than isolated converter. A 15 V input, 200 V output, 100 W DC-DC boost converter for micro grid application is presented in [6], however high gain is achieved through the coupled inductor. Due to the leakage inductance of transformer voltage spike are produced across the switches, mostly in high gain converter two or more switches are used, it leads to switching stress. To improve the reliability, safe, economics of the commercial fuel cell EV hybrid systems are developed by Energy Storage Devices (ESDs) optimization [7, 8], battery charger [9], local renewable energy for electric vehicle and charging management are explained [9, 10].

Power converter plays an important role to boost up the voltage from 100 V to 400 V through a DC bus link, super capacitor system with a low input current ripple [11, 12]. Recently high gain quadratic boost converter is coupled with Cuk converter to overcome the need of high voltage gain and reduced input current ripple. Quadratic DC-DC Boost-Cuk HQBC converter type I and type II

Cite this article as: Desingu, S., Mouttou, A. "FOPID Controller Design and Implementation for High Gain Quadratic Boost Switched Capacitor Converter", Periodica Polytechnica Electrical Engineering and Computer Science, 64(4), pp. 382–391, 2020. https://doi.org/10.3311/PPee.15783

are examined in detail [13]. From the study, the controller implementation of the modified high gain converter is very minimum and very few control techniques are adopted only for the quadratic boost converter. Controller is very essential to improve the dynamic and static performance for the static load and dynamic load. Non minimum phase behavior of the quadratic boost converter modeling, analysis and some control technique like average current-mode controller, two loop integer order controllers, sliding mode controller have been widely discussed in the literature [14–20].

This paper concentrates on improving the output voltage gain by designing of hybrid DC-DC converter (i.e., combination of quadratic boost converter and voltage multiplier) named as Quadratic Boost Switched Capacitor Converter (QBSCC). It has numerous advantages like high voltage gain with single active switch and having provision to vary the level of output voltage by using switched capacitor circuit with self-balancing form. QBSCC also having the properties of non-minimum phase, so non-linear controller is adopted for improving the performance of the system. PID controller technique is broadly adopted for converter because it is simple, very effective and user friendly. It has solely three tuning parameters and it is lack of robustness.

Due to the non-linearity constraint of input and output variables several nonlinear control methods are developed. Recently nonlinear system design issues and analysis of uncertainties nonlinear problems are addressed by sliding mode approach where uncertainties are grouped in to unknown but bounded functions. It gives better performance in internal parameter variation, external disturbance and provides good results in fast transient response. To increase the stability of system and controller performance PID controller is replaced by fractional order PID controller. Fractional PID controller has the advantage of additional tuning parameter (i.e., fractional integral and derivative parameter) [21, 22]. Genetic algorithm optimization method is used to tune the parameters of non- integer order and integer order controller. The performance results are analyzed and compared with integer order PID controller for Quadratic Boost Switched Capacitor Converter using the simulation platform of MATLAB/SIMULINK.

The rest of the paper is organized as follows. In Section 2 discussed about the operating principle, modes of operation, full order and reduce order model for QBSCC. Fractional order controller implementation for QBSCC is described in the Section 3. Performance comparison of QBSCC with integer order and non–integer order controller presented in Section 4. Finally, concluding remarks are drawn in Section 5.

2 Quadratic Boost Switched Capacitor Converter 2.1 Operating principle

The non-isolated quadratic boost converter switched capacitor converter operates is continuous conduction mode and produce output voltage in form of self-balancing. In QBSCC output voltage can be increased by adding the pair of switched capacitor (see Fig. 2). The proposed QBSCC has four different modes of operation with the time interval of t_0 , t_1 , t_2 and t_3 respectively.

Mode I: (t_0-t_1) : During this ON state of switch SW, the diode D_1 is in reverse biased condition and diode D_2 is in forward biased condition. In this period the inductor L_1 stores energy from input voltage E and the inductor L_2 stores the energy from voltage in capacitor C_1 is shown in Fig. 3 (a). Hence the capacitor energy C_1 discharges slowly through the inductor L_2 .

Mode II: (t_1-t_2) : During this period, the switch SW remains in turn ON state, the diode D_1 , D_2 position remain same as reverse biased and forward biased respectively. However, diode D_4 starts conducting, due to C_4 's voltage is smaller than C_2 's voltage then C_2 clamps C_4 's voltage through D_4 depicts in Fig. 3 (b) and Fig. 4.

Mode III: (t_2-t_3) : Fig. 3 (c) shows the switch SW in OFF state, here the diode D_1 and D_3 are forward biased and diode D_2 , D_4 , D_5 are operated in reverse biased condition. Hence the energy stored in both the inductors L_1 and L_2 got discharged. Meanwhile, the voltage across capacitor C_1 start charging through D_1 and the capacitor C_2 is charged through inductor L_2 by the conduction of the diode D_5 . Similarly, C_2 and C_3 are also charged by conduction of diode D_3 .

Mode IV: (t_3-t_4) : The position of switch remains same as previous mode (OFF state). When D_3 closes, capacitor C_4 and the input voltage E plus the inductor's voltage clamp the voltage across C_2 and C_3 through D_5 (see Fig. 3 (d)). The continuous conduction mode state of operation is presented in Fig. 4. Based on the four modes of QBSCC operation, dynamic behavior of the system is derived with two LTI models (i.e., ON state and OFF state).



Fig. 2 Quadratic Boost Switched Capacitor Converter



Fig. 3 Modes of operation of the QBSCC

2.2 Modelling of Quadratic Boost Switched Capacitor Converter

To obtain the transfer function of the proposed converter, the full order state space model is derived. Since the proposed converter has single switch, two different model is derived. During switch ON state one model is obtained and during switch OFF state another model is obtained. The input voltage for the converter is *E*. The state variables in the circuit are voltage across capacitor C_1 denoted as V_{C1} , current through the inductors L_1 and L_2 denoted as i_{L1} , and i_{L2} , voltage across capacitor C_1 , C_2 , C_3 , C_4 denoted as V_{C1} , V_1 , V_2 and V_3 respectively.



Fig. 4 Key waveform of CCM of QBSCC

The parameters are R, L_1 , L_2 , C_1 , C_2 , C_3 , and C_4 . Where R represents the load and the load voltage is denoted as V_0 . The state space model can be derived by writing the voltage loop equations. The ON state dynamic equations can be written using the Fig. 3 (b) and are given in Eq. (1). The OFF state dynamic equations can be derived using the model given in Fig. 3 (d) and are given in Eq. (2):

$$\frac{di_{L1}}{dt} = \frac{E}{L_{1}}$$

$$\frac{di_{L2}}{dt} = \frac{V_{C1}}{L_{2}}$$

$$\frac{dV_{C1}}{dt} = -\frac{i_{L2}}{C_{1}}$$

$$\frac{dV_{1}}{dt} = -\frac{V_{1}}{(C_{2} + C_{4})R} - \frac{V_{2}}{(C_{2} + C_{4})R}$$

$$\frac{dV_{2}}{dt} = -\frac{V_{1}}{C_{3}R} - \frac{V_{2}}{C_{3}R}$$

$$\frac{dV_{3}}{dt} = -\frac{V_{1}}{(C_{2} + C_{4})R} - \frac{V_{2}}{(C_{2} + C_{4})R}$$
(1)

$$\frac{di_{L1}}{dt} = \frac{E}{L_1} - \frac{V_{C1}}{L_1}$$

$$\frac{di_{L2}}{dt} = \frac{V_{C1}}{L_2} - \frac{V_{C2}}{L_2}$$

$$\frac{dV_{C1}}{dt} = \frac{i_{L1}}{C_1} - \frac{i_{L2}}{C_1}$$

$$\frac{dV_1}{dt} = \frac{i_{L2}}{C_2} - \frac{V_1}{C_2R} - \frac{V_2}{C_3R}$$

$$\frac{dV_2}{dt} = \frac{V_1}{(C_2 + C_3)R} - \frac{V_2}{(C_2 + C_3)R}$$

$$\frac{dV_3}{dt} = \frac{V_1}{(C_3 + C_4)R} - \frac{V_2}{(C_3 + C_4)R}$$

2.3 Reduced order model of Quadratic Boost Switched Capacitor Converter

(2)

The voltage balancing feature of the Quadratic Boost Switched Capacitor Converter is obtaining a reduced order model. The derived reduced order model exhibits an approximate dynamics for the two levels QBSCC. This feature provides several advantages for the control design and implementations. In order to increase the gain of the converter, a diode-capacitor pair is added at the output. The reduced order model is convenient for simplification and this approach will focus only on output voltage across the load rather than to find voltage across every capacitor at the output. The reason to go for reduced order model because of its simplicity and robustness.

The dynamic behavior of the reduced order model is approximately equal to the full order model. The balancing form of voltage is present in capacitor which is connected across the load. Hence the value of capacitor and the value of voltage remain same. When increasing the number of voltage level in output, then the capacitor can be treated as series and parallel combination. In Fig. 5 (a), describes the reduced order ON state. Here capacitors C_2 and C_4 are in parallel, then the equivalent capacitor is taken as C_{eql} . Similarly, the Fig. 5 (b) explains the reduced order model of the circuit in switch OFF mode. Here the C_3 and C_4 are in series, C_2 is taken as C_{eq2} . Here it is assumed that $C \approx C_2 \approx C_3 \approx C_4$ and $V_1 \approx V_2 \approx V_3 \approx \ldots \approx V_N \approx \frac{V}{N}$. *V* is the

output voltage. The state equations are obtained using Kirchoff voltage law and Kirchoff current law. The dynamic nonlinear state equations of reduced order switch ON state and switch OFF state are given in Eq. (3) and Eq. (4):



Fig. 5 Reduced order model of QBSCC

$$\frac{di_{L1}}{dt} = \frac{E}{L_{1}} \\
\frac{di_{L2}}{dt} = \frac{V_{C1}}{L_{2}} \\
\frac{dV_{c1}}{dt} = -\frac{i_{L2}}{C_{1}} \\
\frac{dV}{dt} = -\frac{NV}{RC_{eq1}} \\
, (3)$$

$$\frac{di_{L1}}{dt} = \frac{E}{L_{1}} - \frac{V_{c1}}{L_{1}} \\
\frac{di_{L2}}{dt} = \frac{V_{C1}}{L_{2}} - \frac{V}{L_{2}} \\
\frac{dV_{c1}}{dt} = \frac{i_{L1}}{C_{1}} - \frac{i_{L2}}{C_{1}} \\
\frac{dV}{dt} = \frac{i_{L2}}{C_{eq2}} - \frac{NV}{RC_{eq2}} \\
. (4)$$

In the transient state analysis, the large signal model is evaluated for ON and OFF states of the circuit respectively and we get the values of A_1 , B_1 , C_1 , D_1 from the ON state and A_2 , B_2 , C_2 , D_2 from the OFF state. Using the above equation (Eq. (3) and Eq. (4)) averaged large signal model is formed from the Eq. (5), where d denoted the duty ratio:

$$A = A_{1}d + A_{2}(1-d)$$

$$B = B_{1}d + B_{2}(1-d)$$

$$C = C_{1}d + C_{2}(1-d)$$

$$D = d_{1}d + D_{2}(1-d)$$
(5)

The average state space model of the reduced order Quadratic Boost Switched Capacitor Converter is shown in Eq. (6). Small signal model is arrived by replacing derivative $\dot{x} = 0$, duty cycle *d* is replaced as $\hat{d} \cdot A\hat{x} + B\hat{u}$ is termed as small signal model, here $\hat{x} \times \hat{d}$ assumed to be neglected and $\dot{x} = Ax + Bu = 0$.

$$\dot{\hat{x}} = A\hat{x} + B\hat{u} + \left[\left(A_1 - A_2 \right) x + \left(B_1 - B_2 \right) u \right] \hat{d}$$
(6)

$$\hat{y} = C\hat{x} + D\hat{u} + \left[\left(C_1 - C_2 \right) x + \left(D_1 - D_2 \right) u \right] \hat{d}$$
(7)

Similarly, the output state equation is given in Eq. (7). $x(t) = \begin{bmatrix} i_{L1} & i_{L2} & V_{C1} & V_{C2} & V_{C3} & V_{C4} \end{bmatrix}^T \in \mathbb{R}^4$ are the average values of the state vector, A is the matrix in $\mathbb{R}^{4\times 4}$ and B is a vector of \mathbb{R}^4 . The parasitic capacitance is comparatively small and is neglected for simplicity purpose. The representation of the matrix is nonlinear depends on the control signal \hat{d} . General small signal model state equation and output equations are written in the Eq. (8) and Eq. (9):

$$\dot{\hat{x}} = A\hat{x} + B\hat{u},\tag{8}$$

$$\hat{y} = C\hat{x} + D\hat{u}.\tag{9}$$

The voltage ripple in the all capacitor considered as zero and power loss in the switch also not considered. The small signal model state space equation for the Quadratic Boost Switched Capacitor Converter is given in Eq. (10):



Based on the Eq. (11), the transfer function of output voltage to duty ratio is derived and it expression is given in Eq. (12), where $\hat{e} = 0$.

$$\frac{\dot{V}}{\dot{d}} = C[SI - A]^{-1}B \tag{11}$$

$$\frac{\hat{V}}{\hat{d}} = \frac{2.5 \times 10^6 \, s^3 + 4 \times 10^{10} \, s^2 + 8.5 \times 10^{13} \, s + 1.3 \times 10^{20}}{s^4 + 4410 \, s^3 + 1.3 \times 10^7 \, s^2 + 1.1 \times 10^{13} \, s + 8.2 \times 10^{17}} \quad (12)$$

From the transfer function (output voltage to duty ratio). Zeros are located at (-4267, $13348 \pm i31447$), Poles are located at ($-31901 \pm i29981$, -28138). The operating frequency of the MOSFET is 40 kHz. The bode plot for the transfer function is given in Fig. 6.

Fuel cell output is unregulated and it is dynamic behavior, this output of the fuel cell is given to the Quadratic Boost Switched Capacitor Converter as an input. Due to dynamic behavior in the input source the converter delivers an output with large variation. Also large variation in load affects the performance of the converter, so the controller is necessary with high performance for fast transient response and good regulation when an unregulated source is used and load variation is occur. For achieving good dynamic and steady state response PID controller is extensively used. The proportional factor gives an overall control action which is proportional to the error signal through constant gain factor. Steady state error reduced through low-frequency compensation by an integrator. Similarly, transient response improved through high frequency compensation by a differentiator.

The main advantage of Fractional-order controller is that it provides more adjustable time and frequency responses of the control system allowing fulfillment of better as well as robust performance. So a fractional-order controller will always provide better response than integer-order controller if it is properly tuned whatever may



Fig. 6 Bode plot of QBSCC

be the type of plant (integer or fractional). It provides more degrees of freedom than its integer order counterpart.

The proposed QBSCC converter is behaving as non-minimum phase system. In order to reduce the complication, the optimization technique is used for obtaining the parameters present in controller. In this proposed work IOPID controller is designed and the gain of the controller is optimized by the genetic algorithm tuning method.

3 Fractional order PID controller

There are analytical, numerical and rule-based techniques and are presented for tuning the parameters of FOPID controller and those methods are explained in [22]. The parameters derived from nonlinear equations gives better results by satisfying phase margin and gain margin for the given specification [23]. If the system is first order and the equation is simple, then analytical method is appropriate. For the higher order systems like fourth order or fifth order systems, the design of the parameter of $PI^{\lambda}D^{\mu}$ for the given converter system, is discussed in the paper [24-27]. The rule based technique is also difficult, because of the unstable behavior of the controller plant [28–30]. Compared to the analytical and rule based system, numerical technique is more convenient for obtaining the controller parameters for higher order system, which is optimization based method. In [31], load disturbance constraint is addressed and also deals the integral gain optimization algorithm for tuning FOPI controller. Tuning and auto tuning algorithm are proposed in [32], MATLAB optimization toolbox is adopted to solve this problem:

$$aD_{t}^{r} = \begin{cases} \frac{d^{r}}{dt^{r}} & \mathbb{R}(r) > 0, \\ 1 & \mathbb{R}(r) = 0, \\ \int_{\alpha}^{t} (d\tau)^{-r} & \mathbb{R}(r) < 0 \end{cases}$$
(13)

The basic definition of fractional calculus is discussed in [33, 34]. The generalized operator function is given in Eq. (13).

"*r*" denotes as complex number. Rienmann-Liouville (RL) definition, Grunewald-Letnikov (GL) definition and Caputo fractional derivatives are coincide at zero initial conditions. All these three methods are suitable to eliminate the difference arising due to different initial conditions. The corresponding relations are given in the Eqs. (14)–(16):

$$aD_{t}^{r}f(t) = \frac{1}{\Gamma(n-\alpha)} \left(\frac{d}{dt}\right)^{n} \int_{\alpha}^{t} \frac{f(\tau)}{(t-\tau)^{\alpha-n+1}} d\tau, \qquad (14)$$

$${}_{a}^{C}D_{t}^{\alpha}f(t) = \lim_{h \to 0} h^{-\alpha} \sum_{j=0}^{\left\lfloor \frac{t-\alpha}{h} \right\rfloor} (-1)^{j} \binom{\alpha}{j} f(t-jh),$$
(15)

$${}_{a}^{C}D_{t}^{\alpha}f(t) = \frac{1}{\Gamma(n-\alpha)}\int_{\alpha}^{t}\frac{f^{n}(\tau)}{(t-\tau)^{\alpha+1-n}}d\tau.$$
(16)

 $(n-1) \le \alpha < n$, where α is a real number, and *n* is an integer. The general form of G(z) of discrete transfer function of the controlled system is represented by the Eq. (17):

$$G(z) = \frac{b_m \left(w(z^{-1})\right)^{\beta_m} + \ldots + b_0 \left(w(z^{-1})\right)^{\beta_0}}{a_n \left(w(z^{-1})\right)^{\alpha_n} + \ldots + b_0 \left(w(z^{-1})\right)^{\alpha_0}}.$$
(17)

The discrete value of Laplace operator denoted as $w(z^{-1})$ in the form of complex variable *z*. The generalized transfer function of the fractional order PID ($PI^{\lambda}D^{\mu}$) controller is presented in the Eq. (18):

$$C(s) = \frac{V_0(s)}{E(s)} = K_p + T_i s^{\lambda} + T_d s^{\mu}.$$
 (18)

The discrete value of Laplace operator denoted as $w(z^{-1})$ in the form of complex variable *z*. The generalized transfer function of the fractional order PID ($PP^{\lambda}D^{\mu}$) controller is presented in the Eq. (14). In Eq. (14) positive real numbers are denoted by λ and μ . K_p , T_i , T_d are proportional gain, integral time constant and derivative time constant respectively. The integer order PID controller can be obtained from the non-integer controller making the assumption of $\lambda = -1$ and $\mu = 1$. If the value of λ is kept as zero then the controller termed as PD controller. Correspondingly $\mu = 0$ will result in PI controller. The time domain function is stated and is given in Eq. (19):

$$u(t) = K_{p}e(t) + T_{i}D_{t}^{\lambda}e(t) + T_{d}D_{t}^{\mu}e(t).$$
(19)

 $PI^{\lambda}D^{\mu}$ controller accommodates more tuning parameter to enhance the control system performance. $PI^{\lambda}D^{\mu}$ is an infinite dimensional linear filter because of fractional order in differentiator and/or in integrator. Since PID control is omnipresent in portable hybrid electric vehicle and industrial process control, FO PID control will also become omnipresent once tuning and implementation techniques are well developed. Some typical fractional order controllers which are introduced in literature are namely, TID (Tilted Integral Derivative) controller, CRONE controller and fractional lead-lag compensator.

3.1 Objective function of genetic algorithm

Genetic algorithm optimization method is popular and operation is carried by natural way. It randomly generates the solution by population; it is believed that good solutions are to be evolved by applying the genetic operations, namely, cross over and mutation on some selected parents [35]. It is used to search the best solution that problem arises from maximizing the fitness function. The Integral Absolute Error (IAE) function is used as an objective function and is given in Eq. (20). The purpose of error function is to reduce the peak overshoot, fastening the settling time and improving the system performance:

$$IAE = \int |e(t)| dt.$$
⁽²⁰⁾

This fitness function is then optimized by GA such that the voltage and current errors get reduced with the optimized K_p , K_i and K_d . The performance measure used in this present case is the minimization of Integral of Average Error (IAE). The fitness function is given as the inverse of IAE. The optimum values obtained for the PID and FOPID controllers using the genetic algorithms were given in Table 1.

4 Performance analysis

The Quadratic Boost Switched Capacitor Converter with PID controller and FOPID controller were implemented using MATLAB/SIMULINK. The component designs are carried for the proposed system for the nominal power of 250 W, 400 V. It provides better voltage gain with reduced duty ratio (D = 0.5). The voltage gain expressed as a ratio of output voltage to input voltage given in Eq. (21):

$$\frac{V_o}{E} = \frac{N}{(1-D)^2}.$$
(21)

Here *N* represents number of diode capacitor pair. It has the provision for increasing the voltage gain either by increasing duty ratio or by adding diode capacitor pairs across load. The load resistor varies from 200 Ω to 600 Ω . The switch operates at the switching frequency of 40 kHz. The transfer function of output voltage to duty ratio $\frac{\hat{v}_o}{\hat{d}}$ exhibits the fourth

order relation. The components values are designed based on the relation given in [36]. The parameters are decided from the design formula given in Eq. (22) to Eq. (25):

$$L_1 = \frac{ED}{\delta i_{L1} f_{sw}},\tag{22}$$

$$L_2 = \frac{ED}{\delta i_{L2} (1-D) f_{sw}},$$
(23)

 Table 1 Parameters of PID and fractional order PID controller

parameter	K_p	K_{i}	K_{d}	λ	μ
FOPID	4.724	2.512	1.726	0.1229	0.6122
PID	1.009	1.682	2.94	1	1

$$C_{1} = \frac{I_{0}D}{(1-D)\Delta V_{C1}f_{sw}},$$
(24)

$$C_2 = C_3 = C_4 = \frac{I_0 D}{\Delta V_{C2} f_{sw}}.$$
 (25)

The parameters of the FOPID controllers were obtained using genetic algorithms optimization toolbox. The converter with fractional order PID controller design is given in Fig. 7, and the specification of the converter is given in Table 2.

Line regulation and load regulation analysis are carried and the performance in steady state and dynamic conditions were tested. Fig. 8 shows the responses of the system with PID and FOPID controllers. It is found that the initial peak overshoot is more for FOPID controller. But the performance of the FOPID controller is better during load changes. Fig. 8 exhibits the load variation from 600 Ω to 400 Ω , i.e., approximately 60 % of load variation. The load change is applied at 0.1 sec; undershoot of voltage present in PID controller for 0.03 sec with magnitude of 27 V. But this undershoot problem not present in FOPID controller. Also it has reduced voltage magnitude approximately 6 V.

The simulation results of Fig. 9 shows the line voltage variation results, when the line voltage is varied from 40 V to 50 V at 0.1 sec. It is found that the input voltage disturbance does not affect the system performance when a FOPID controller is used. In contrast a PID controller response has produce overshoot, when the input voltage changed.

The system with PID controller the peak overshoot value is around 460 V with short settling time 250 μ sec. The transient response of the proposed converter with FOPID controller operating at nominal load of 400 Ω does not show much peak overshoot. The performance comparison of the dynamic behavior of system under perturbations with PID and FOPID controller is given in Table 3. From the Table 3 it is found that the peak overshoot and settling time is much better for the system with FOPID controller.

5 Conclusion

In this work a fractional order PID controller was designed for the Quadratic Boost Switched Capacitor Converter using genetic algorithm optimization method. The Quadratic Boost Switched Capacitor Converter with FOPID controller was implemented using MATLAB/Simulink and its performance was analyzed. An integer order PID controller also designed and implemented for Quadratic Boost Switched Capacitor Converter and the performance of the converter with both the controller were compared.



Fig. 7 Fractional order PID controller for Quadratic Boost Switched Capacitor Converter

Table 2 Parameters of the QBSCC					
Input voltage (E)	50 V				
Output voltage (V_0)	400 V				
Duty cycle range (D)	0.5 to 0.9				
Capacitor 1 (C_1)	5 µF				
Inductor 1 (L_1)	156 µН				
Inductor 2 (L_2)	312 µH				
Load resistor (R)	200 Ω				
Capacitor (C_1, C_2, C_3)	10 µF				
Switching frequency (f_{sw})	40 kHz				

In load variations, the output is well regulated in both the controller. The steady state and dynamic response is better for FOPID controller. Settling time on load variation and line variation, FOPID controller works much better than PID. But during initial transient response condition the FOPID, has pronounced peak overshoot. While in PID peak overshoot is minimum in transient condition, but the settling time in PID. From the results suggest that FOPID controller is better than PID controller during input voltage variation and load current variation conditions.



Fig. 8 Comparison of transient response under changes on load from 600 Ω to 400 Ω



Fig. 9 Comparison of transient response under changes on input voltage from 40 V to 50 V

Table 3 Performance comparison									
Daramatar		Fractional order controller		Integer order controller					
Farameter		Settling time (sec)	Over shoot (%)	Settling time (sec)	Over shoot (%)				
Dynamic response	Load variation	0.001	1.25	0.003	6.7				
	Line variation	0.001	1.05	0.016	20				

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