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Can the Genericity Assumption Decrease the Rank of a Matrix?

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Abstract

The genericity assumption, supposing that the nonzero parameters of a system are algebraically independent transcendentals over the field of the rationals, often helps for the mathematical modelling of linear systems. Without this condition nonzero expansion members of a determinant can cancel out each other, decreasing the rank of a matrix. In this note we show that under some circumstances an increase is also possible. This counterintuitive phenomenon is explained using some tools from matroid theory, and is illustrated by a classical network of Carlin and Youla.

Keywords

circuit analysis, linear multiports, genericity

1 Introduction

The genericity assumption is often applied in the qualitative study of linear systems. For example, the network of Fig. 1 which contains a current controlled current source $i_4 = ci_2$, is uniquely solvable if and only if $R_2 + R_3 + (c+1) \times R_5 = 0$ does not hold. However, such an equation (or any other a priori given algebraic equation) cannot be satisfied if we suppose that the parameters of the network are algebraically independent transcendental numbers.

Similar situations arise in other engineering disciplines as well. For example, let the graph of a planar bar-and-joint framework be isomorphic to the Kuratowski graph $K_{3,3}$. Then the framework will be infinitesimally rigid [1] unless the six joints are on a common conic section [2] – this condition is equivalent to a quadratic equation among the 12 coordinates.

Therefore, one expects that special values of some system parameters can only decrease the rank of a matrix (see a more precise formulation in Section 2). However, we show that an increase is also possible. After a theoretical explanation (which requires some tools from matroid



Fig. 1 A network and its graph after replacing the independent current source by an open circuit

theory) we illustrate the phenomenon with a classical network of Carlin and Youla [3] and Carlin [4].

For the definitions of the concepts from matroid theory the reader is referred to [1] or [5]. We use standard notations of matroid theory, in particular, / denotes contraction and \lor denotes the union of matroids.

2 Term rank, genericity and an example

Let $r(\mathbf{M})$ denote the "usual" rank of a matrix \mathbf{M} . A set of nonzero entries in a matrix \mathbf{M} is a *transversal* if no pair of these entries share the same row or column. The size $t(\mathbf{M})$ of a maximum transversal is the *term rank* of \mathbf{M} . Clearly $t(\mathbf{M}) \ge r(\mathbf{M})$ since the determinant of a square matrix is the signed sum of products of entries along maximum size transversals but these products can cancel out each other. For example, the $p \times q$ matrix with ones in every position has rank 1 while its term rank is min(p, q) for every $p, q \ge 1$.

Such cancellations are impossible if the matrix is *generic*, that is, if its nonzero entries are algebraically independent over the field of the rational numbers. Hence the rank of the matrix can only *decrease* if we drop the genericity assumption. For example, if the independent current source I_1 is replaced by an open circuit in the network of Fig. 1, we have a system of 8 equations and the coefficient matrix has rank 8 or it reduces to 7 if $R_2 + R_3 + (c + 1) \times R_5 = 0$ holds. Similarly, there are plenty of examples that the degree of freedom of a

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network composed of multiports, capacitors and inductors decreases if we drop genericity.

Remark. There are several definitions of genericity in the literature. For a critical comparison the reader is referred to [6].

However, if a multiport arises as the interconnection of some others, a somewhat surprising phenomenon arises: the rank of the final multiport can also *increase* if we drop genericity.

In order to explain this recall that the interconnection of some multiports M_1, M_2, \ldots into a single multiport M is described by a graph G as illustrated in Fig. 2 where two 2-ports are interconnected to form a three-port. Both the ports of the original multiports and those of the obtained one correspond to edges of G. Observe that if terminal nodes of a multiport have internal connections (like the ones belonging to ports 1 and 2 of the upper 2-port) then this is reflected by G. Throughout we shall suppose that G contains neither loops nor bridges (coloops). However, G need not be 2-vertex-connected.

If a multiport *M* is described by Au + Bi = 0 with r(A|B) = r then the column space matroid of the matrix (A|B) will be denoted by $\mathcal{M}(M)$. Recall that if C is a nonsingular $r \times r$ matrix and we change the description of the multiport to the equivalent one (CA|CB) then the matroid remains the same.

The edge set E of the interconnection graph G is the union of the set E_{Int} of the *internal* edges (corresponding to the ports of the multiports M_1, M_2, \ldots) and the set E_{Ext} of the *external* edges (corresponding to the ports of the resulting multiport M). Since each port has a voltage and a current, let E^U and E^I denote the set of all the voltages and that of all the currents, respectively. These sets can also be decomposed into $E_{Int}^U \cup E_{Ext}^U$ and into $E_{Int}^I \cup E_{Ext}^I$, respectively.

Let \mathcal{G} denote the direct sum of the cycle matroid of G on the set E' and the cocycle matroid of G on the set E^U . Let \mathcal{A}' denote the direct sum of the matroids $\mathcal{M}(M_1), \mathcal{M}(M_2), \ldots$ on the set E_{Int} . Let us extend \mathcal{A}' with loops on the set E_{Ext} to



Fig. 2 Two 2-ports M_1 and M_2 interconnected to form a 3-port M, and the graph G of the interconnection

obtain a matroid \mathcal{A} . Observe that both matroids \mathcal{G} and \mathcal{A} are defined on $E^U \cup E^I$. If the genericity assumption holds then $\mathcal{M}(M) = (\mathcal{G} \lor \mathcal{A}) / (E_{Int}^U \cup E_{Int}^I)$ see [7, 8].

Suppose now that we drop the genericity and a cancellation occurs. Usually it decreases the rank of the multiport, but if this cancellation happens to be within the set $(E_{Int}^U \cup E_{Int}^I)$, then one will contract a subset of smaller rank, hence the rank of the final multiport can also increase.

A classical example of Carlin and Youla [3] (Fig. 3) is revisited to illustrate this.

The matroid $\mathcal{W}(C)$ of a 3-port circulator *C* is isomorphic to the cycle matroid of a complete graph on 4 vertices, see [6, 7, 8]. Hence the matroids \mathcal{G} and \mathcal{A} are the cycle matroids of the graphs of Figs. 4(a) and (b), respectively, their union is the uniform matroid $\mathcal{U}_{12,11}$, that is, a circuit of length 12. The subgraph formed by the edges with subscripts less than 6 is circuit-free and after contracting them we obtain a length 2 circuit, corresponding to a resistor, as expected in the generic case.

If we put $R_1 = 1$, $R_2 = -1$, the number of linearly independent equations *decreases* from 11 to 10. The coefficient



Fig. 4 The graphs representing the matroids in the example; a); b); c)

matrix of the system of equations determines a matroid which is different from $\mathscr{G} \lor \mathscr{A}$ but happens to be graphic again, see the graph of Fig. 4(c) for its representation – observe that it is not the length 12 circuit anymore but a graph containing two linearly independent circuits. The subgraph formed by the edges with subscripts less than 6 is still circuit-free, its contraction leads to two loops, corresponding to the norator – a *decrease* of the final rank, as expected.

If we put $R_1 = -1$, $R_2 = 1$, the number of linearly independent equations remains 11, but the matroid of the system becomes the direct sum of a length 8 circuit and 4 bridges, corresponding to u_5 , u_6 , i_5 and i_6 . Hence the subgraph formed by the edges with subscripts less than 6 does contain a circuit and after contracting these edges we obtain two bridges, corresponding to the nullator. Since the rank of the contracted subgraph decreased, we experience an *increase* in the rank of the resulting 1-port.

3 Further discussion

For the complete understanding of the behavior of this network it might be instructive to add some further remarks:

- 1. If $R_1 + R_2 = 0$ still holds but $R_1R_2 \neq -1$ then the number of linearly independent equations remains 11, but the matroid of the system becomes the direct sum of a length 10 circuit and 2 bridges, corresponding to i_5 and i_6 . Hence we obtain an open circuit.
- 2. If $R_1 + R_2 \neq 0$ but $R_1R_2 = -1$ still holds then the number of linearly independent equations remains 11, but the matroid of the system becomes the direct sum of a length 10 circuit and 2 bridges, corresponding to u_5 and u_6 . Hence we obtain a short circuit.
- If none of the relations R₁ + R₂ = 0 and R₁R₂ = −1 holds then the number of linearly independent equations remains 11, but the matroid of the system need not necessarily become *U*_{12,11}, as expected for the generic case. If, for example, we put R₁ = 1 and R₂ = 1, the matroid becomes the direct sum of a length 8 circuit and 4 bridges, corresponding to u₂, u₄, i₂ and i₄. Nevertheless, this does not change the final result since we must contract the subgraph formed by the edges with subscripts less than 6.

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 Recski, A. "Matroid Theory and its Applications in Electric Network Theory and in Statics", Springer-Verlag, Berlin, Heidelberg, Germany, 1989. https://doi.org/10.1007/978-3-662-22143-3 4. Recall that in the generic case the network behaves like a resistor. In the "traditional" way, without using matroid theory, we can solve the system of the 11 equations describing the network and obtain the relation between the current and the voltage of port 6 (i.e. the resistance of the port) as a function of the values of the resistances terminating ports 3 and 4.

$$u_6 = \frac{R_1 R_2 + 1}{R_1 + R_2} i_6$$

We can plot this resistance value as a surface, to visualize the behavior of this network, see Fig 5. Aside from the generic case it is immediately clear that:

- if $R_1 + R_2 = 0$, the resistance of this port is infinite and therefore it behaves like an open circuit, and
- if $R_1R_2 = -1$ holds then this resistance becomes zero and we obtain a short circuit.

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Fig. 5 The resistance of port 6 as a function of R_1 and R_2

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