

Performance Analysis of Universal Power Quality Conditioner Systems Based on Seven-level NPC Inverter Using PD-SPWM with Fuzzy Control Scheme

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Received: 16 March 2022, Accepted: 17 August 2022, Published online: 09 September 2022

Abstract

This paper presents novel Unified Power Quality Conditioner (UPQC) system based on seven-level Neutral Point Clamped (NPC) inverter using combined PD-SPWM and fuzzy control scheme. The proposed UPQC is adopted to mitigate source current harmonics and compensate all voltage disturbances simultaneously. It is designed by the combination of series and shunt Active Filters (AFs) connected by a common DC link capacitor. The DC voltage at common DC bus is maintained constant using proportional integral voltage controller. The Synchronous Reference Frame (SRF) method is used to get the shunt APF reference signals and the power reactive theory (P-Q theory) for the series APF. Conventional control schemes require complex calculations, the use of intelligent systems help to reduce the control system size and the operation complexity. The shunt and series Active Power Filter (APF) reference signals derived from the control algorithm are injected in Fuzzy intelligent controllers to generate switching signals. The functionality of proposed UPQC system and its control system is evaluated using Matlab-Simulink software and SimPowerSystem Toolbox under various operation conditions in cases of most common power quality problems such as voltage sag, voltage swell, current harmonic compensation of nonlinear loads and unbalanced load. The simulation results show UPQC performances to improve the power quality in steady and transient conditions operation at the point of common coupling on power distribution under unbalanced and distorted voltage conditions.

Keywords

seven-level (NPC) inverter, UPQC, fuzzy logic control, PD-SPWM, voltage disturbance compensation, power quality enhancement, Total Harmonic Distortion (THD)

1 Introduction

With the proliferation of the power electronics devices, nonlinear loads and unbalanced loads, the Power Quality (PQ) in the power distribution network has degraded significantly [1]. To improve the power quality, some solutions have been proposed by several authors. Among them the shunt [2] and series active power filters have proven as an important and flexible alternative to compensate most important voltage and current related power quality problems in the distribution system [3]. In the past, these identified power quality problems were mitigated by using switched capacitor and thyristor controlled inductor coupled with conventional passive filters [4]. But their limitations, such as fixed compensation, resonance with source impedance and the difficulty in tuning time dependence of filter parameters, have ignited the need of Active Power

Filters (APFs) [5]. APFs are considered as one of the promising solutions that are proposed to address various power quality problems. A Unified Power Quality Conditioner (UPQC) has been extensively investigated for its power quality improvement capability in the distribution network. Various topologies of the UPQC have been proposed for application at different power levels and usage requirements [6]. Having the capability to resolve multiple power quality issues simultaneously, the UPQC is the most comprehensive APF that can be employed [7]. UPQC does not compensate only for the short-term voltage disruptions and variations but also improves Total Harmonic Distortion (THD) and decreases losses by canceling out voltage and current harmonics and compensating for reactive power [8, 9]. It is the integration of shunt and series

APFs through a common DC link capacitor. UPQC has been widely studied to eliminate or mitigate the disturbances propagated from the source side and the other loads interconnected [10]. In the normal operation, the shunt APF control circuit calculates the harmonic currents compensation and generates the inverter pulses to power circuits (shunt APF). The series APF compensates the harmonics and all other voltage disturbances by the injection of voltage compensation using three isolated transformers [11]. In general, when a UPQC is used in a power distribution system, the series filter is installed ahead of the shunt filter [12]. The most powerful converter used has been the two-level voltage source inverter [13, 14]. However, due to power handling capabilities of power semiconductors, these inverters are limited for low power applications [15]. The neutral-point-clamped (NPC) converter topology has been the center of research and development effort for several applications, including medium- and high-voltage electric motor drives, static compensators (STATCOMs) and other utility type of power electronic systems for almost three decades now [16, 17]. Their advantages are lower voltage harmonics on the ac side, smaller filter size, lower switching losses, lower electromagnetic interference, lower voltage stress of power semiconductors, and lower acoustic noise; these advantages can reduce the construction cost of active filter in the medium and high voltage applications [18].

The controller is the core of any APF operation and has been the subject of numerous researches in recent years. The conventional control scheme to generate pulses, based on hysteresis technique control, presents several drawbacks such as uneven switching frequency that causes acoustic noise and difficulty in designing input filters in case of SAPF. To improve the APF performance, the tendency has been to use intelligent control techniques [19, 20] particularly fuzzy logic [21]. The use of these techniques in power electronics applications has generated considerable interest [22]. Their advantages are robustness, ability to control nonlinear systems and no need accurate mathematical model, etc. For the proposed UPQC System, the series and shunt APFs are controlled with combined PD-SPWM and fuzzy logic techniques.

This paper investigated the performance analysis of UPQC system based on seven-level (NPC) inverter for power quality improvement. The validity of the proposed system is verified using MATLAB-Simulink software and SimPowerSystems Toolbox.

2 Unified power quality conditioner

The Fig. 1 shows the proposed UPQC system. It consists of two seven-level (NPC) inverters connected back-to-back with each other sharing a common dc link, one used for the shunt and the other for series active filter. The DC link is connected to a 3000 μF common DC capacitor [23]. The series filter is connected between the supply and load terminals using three single phase transformers with turn's ratios of 1:1 to regulate the load voltage. In addition to injecting the voltage, these transformers are used to filter the switching ripple of the series active filter. A small capacity rated C_{sf} filter is used with inductance to eliminate the high switching ripple content in the series active filter [7, 24]. The three leg shunt active filter are connected ahead of a series filter using a small capacity rated inductive filter used to absorb current harmonics, compensate reactive power and negative-sequence current. The UPQC strategy control is based on the synchronous reference frame detection method for the shunt AF and instantaneous reactive power theory for the series AF [16]. These two VSCs require two control algorithms to generate reference voltages and the reference currents. These reference signals are compared with the sensed voltages/currents signals to generate gating pulses for these VSCs [25].

The shunt APF operates in current control mode in a way that load current follows the reference value. The injected current from shunt APF is derived as

$$I_{sh} = i_{s-ref} - i_L \tag{1}$$

I_{sh} is regarded as the injected current by the shunt APF i_L represent the load current and i_{s-ref} the reference value.

Correspondingly, the series APF operates in voltage control mode in a way that voltage at the Point of Common Coupling (PCC) remains sinusoidal and balanced. This

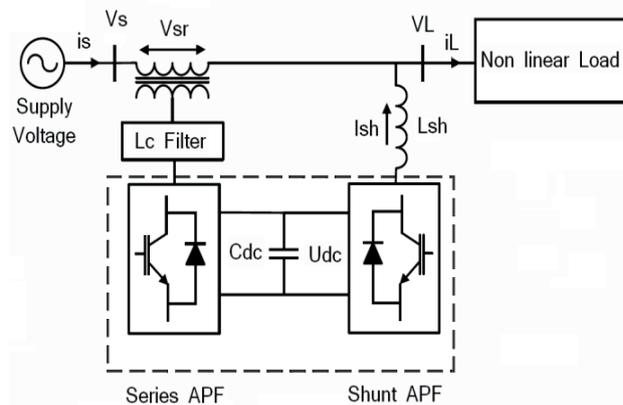


Fig. 1 Basic UPQC configuration system

goal is fulfilled by generating a particular voltage V_{comp} on the winding of the series transformer by series APF according to

$$V_{com} = V_{s-ref} - V_L \quad (2)$$

V_{s-ref} stands for reference source voltage and V_L represents load voltage.

3 Seven-level (NPC) inverter

In recent years, multilevel converters have shown some significant advantages over traditional two-level converters [26, 27], especially for high-power and high-voltage applications. Seven-level inverter is one of the most popular converters employed in high power applications. In addition to their superior output voltage quality, they can also reduce voltage stress across switching devices. Since the output voltages have multiple levels, lower dv/dt is achieved, which greatly alleviates electromagnetic interference problems due to high-frequency switching [28]. But their major drawback is that they require a large number of switches. In general a converter with more voltage levels has less harmonic and better output voltages; however, the increase in converter complexity and number of switching devices is a major concern for a multilevel converter. It has been shown that although more voltage levels generally mean lower Total Harmonic Distortion (THD), the gain in THD is marginal for converters with more than seven levels [29]. The conventional three-phase NPC n -level inverter based on voltage-source will need a number of $(n - 1)$ dc-link capacitors, $2(3n - 3)$ switches and $(6n - 12)$ diodes-clamped (despite anti-parallel diodes of inverter switches). In this inverter, the maximum voltage across each capacitor is equal to $U_{dc}/(n - 1)$ [30].

The power circuit of the seven-level neutral point clamped inverter is given by Fig. 2, the DC bus capacitor is split into six, providing a three neutral-point. Each arm of the inverter is made up of twelve bi-directional IGBTs (Insulated Gate Bipolar Transistor) devices. These switches should not be simultaneously open or closed in order to prevent the short circuit of the DC source of the inverter input. Each switch consists of a transistor with a diode in anti-parallel and ten clamping diodes connected to the neutral-point; these clamping diodes are used to block the reverse voltage and used to create the connection with the point of reference to obtain midpoint voltages. Take note that the required numbers of clamping diodes are quite high and for higher number of voltage levels the NPC topology will be impractical due to this fact. This

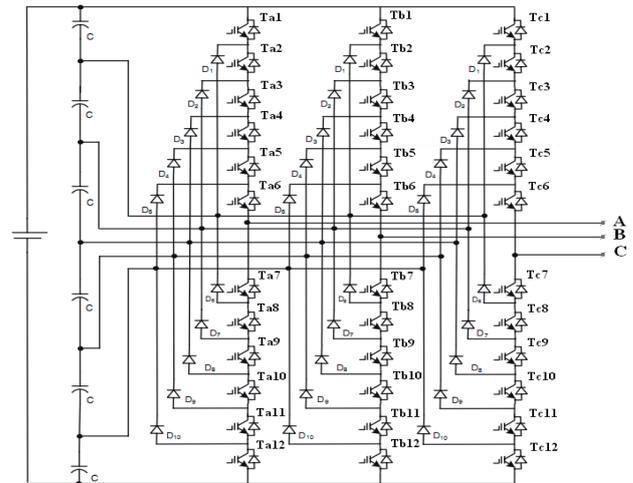


Fig. 2 Seven-level (NPC) inverter

structure allows the switches to endure larger dc voltage input on the premise that the switches will not raise the level of their withstand voltage.

For this structure, seven output voltage levels can be obtained, namely, $U_{dc}/2$, $U_{dc}/3$, $U_{dc}/6$, 0 , $-U_{dc}/6$, $-U_{dc}/3$ and $-U_{dc}/2$ corresponding to seven switching states A , B , C , 0 , D , E and F [31]:

- Voltage level $V_{an} = U_{dc}/2$; turn on all upper switches S_1, S_2, S_3, S_4, S_5 and S_6 .
- Voltage level $V_{an} = U_{dc}/3$, turn on the switches S_2, S_3, S_4, S_5, S_6 and S_7 .
- Voltage level $V_{an} = U_{dc}/6$, turn on the switches S_3, S_4, S_5, S_6, S_7 and S_8 .
- Voltage level $V_{an} = 0$, turn on the switches S_4, S_5, S_6, S_7, S_8 and S_9 .
- Voltage level $V_{an} = -U_{dc}/6$ turn on the switches S_5, S_6, S_7, S_8, S_9 and S_{10} .
- Voltage level $V_{an} = -U_{dc}/3$ turn on the switches $S_6, S_7, S_8, S_9, S_{10}$ and S_{11} .
- Voltage level $V_{an} = -U_{dc}/2$; turn on all lower switches $S_7, S_8, S_9, S_{10}, S_{11}$ and S_{12} .

Table 1 shows the switching states of this inverter.

4 Control strategies

The control strategy is the way to generate reference signals for both shunt and series APFs of UPQC. The compensation effectiveness of the UPQC depends on its ability to follow with a minimum error and time delay the reference signals [32]. The conventional techniques reported in literature produce poor results under distorted and/or unbalanced input/utility voltages, and they involve many calculations [20]. The proposed control scheme is a simple

Table 1 Seven-level (NPC) witching states

Switch	A	B	C	0	D	E	F
S1	1	0	0	0	0	0	0
S2	1	1	0	0	0	0	0
S3	1	1	1	0	0	0	0
S4	1	1	1	1	0	0	0
S5	1	1	1	1	1	0	0
Switching states	S6	1	1	1	1	1	0
	S7	0	1	1	1	1	1
	S8	0	0	1	1	1	1
	S9	0	0	0	1	1	1
	S10	0	0	0	0	1	1
	S11	0	0	0	0	0	1
	S12	0	0	0	0	0	0
Output voltages $E = U_{dc}$	$E/2$	$E/3$	$E/6$	0	$-E/6$	$-E/3$	$-E/2$

method to achieve effective compensation for source current harmonics, reactive power compensation and voltage harmonic mitigation under distorted and/or unbalanced input/utility voltages.

4.1 Shunt APF

The shunt APF control strategy adopted to compensate harmonic currents is the synchronous reference frame detection method. The principle of this technique is described below [33, 34]. The three-phase load currents i_{La} , i_{Lb} and i_{Lc} are transformed from three phase (abc) reference frame to two phase's ($\alpha-\beta$) stationary reference frame currents i_α and i_β using [18, 35]:

$$\begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} = \sqrt{2/3} \begin{bmatrix} 1 & -1/2 & 1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{bmatrix} \begin{bmatrix} i_{La} \\ i_{Lb} \\ i_{Lc} \end{bmatrix}. \quad (3)$$

Using a Phase Locked Loop (PLL), $\cos(\theta_{est})$ and $\sin(\theta_{est})$ can be generated from the phase voltage source U_{sa} , U_{sb} and U_{sc} . The expression of currents i_α and i_β in ($d-q$) reference frame are given by

$$\begin{bmatrix} i_d \\ i_q \end{bmatrix} = \begin{bmatrix} \sin(\theta_{est}) & -\cos(\theta_{est}) \\ \cos(\theta_{est}) & \sin(\theta_{est}) \end{bmatrix} \begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix}. \quad (4)$$

The i_d current is transformed to DC and harmonic components using a low pass filter:

$$\begin{bmatrix} i_d \\ i_q \end{bmatrix} = \begin{bmatrix} \bar{i}_d + \tilde{i}_d \\ i_q \end{bmatrix}. \quad (5)$$

The expression of the reference current $i_{\alpha-ref}$ and $i_{\beta-ref}$ are given by

$$\begin{bmatrix} i_{\alpha-ref} \\ i_{\beta-ref} \end{bmatrix} = \begin{bmatrix} \sin(\theta_{est}) & -\cos(\theta_{est}) \\ \cos(\theta_{est}) & \sin(\theta_{est}) \end{bmatrix} \begin{bmatrix} i_d \\ i_q \end{bmatrix} \quad (6)$$

$$\begin{bmatrix} i_{\alpha-ref} \\ i_{\beta-ref} \end{bmatrix} = \begin{bmatrix} \sin(\theta_{est}) & -\cos(\theta_{est}) \\ \cos(\theta_{est}) & \sin(\theta_{est}) \end{bmatrix} \begin{bmatrix} \bar{i}_d + \tilde{i}_d \\ i_q \end{bmatrix}. \quad (7)$$

The correspondent reference currents in the (abc) frame are given by

$$\begin{bmatrix} i_{a-ref} \\ i_{b-ref} \\ i_{c-ref} \end{bmatrix} = \sqrt{2/3} \begin{bmatrix} 1 & 0 \\ -1/2 & \sqrt{3}/2 \\ 1/2 & -\sqrt{3}/2 \end{bmatrix}. \quad (8)$$

Finally, the compensation currents i_{comp-a} , i_{comp-b} and i_{comp-c} are given by

$$\begin{bmatrix} i_{comp-a} \\ i_{comp-b} \\ i_{comp-c} \end{bmatrix} = \begin{bmatrix} i_{a-ref} \\ i_{b-ref} \\ i_{c-ref} \end{bmatrix} - \begin{bmatrix} i_{La} \\ i_{Lb} \\ i_{Lc} \end{bmatrix}. \quad (9)$$

To compensate the switching inverter losses and regulate the DC link voltage U_{dc} , a proportional integral voltage controller is used. The control loop consists of the comparison of the measured voltage ($U_{dc1} + U_{dc2}$) with the reference voltage U_{dc-ref} . The correspondent current $I_{c,los}$ is given by Eq. (10):

$$I_{c-los} = K_p \Delta U_{dc} + K_i \int \Delta U_{dc} dt. \quad (10)$$

4.2 Series APF

The control strategy used to extract the reference voltages of series APF is based on the $p-q$ theory [36]. When the three-phase voltage source is symmetric and distorted:

$$\begin{bmatrix} U_{sa} \\ U_{sb} \\ U_{sc} \end{bmatrix} = \begin{bmatrix} \sum_{n=1}^{\infty} \sqrt{2} U_n \sin(n\omega t + \theta_n) \\ \sum_{n=1}^{\infty} \sqrt{2} U_n \sin((n\omega t - 2\pi/3) + \theta_n) \\ \sum_{n=1}^{\infty} \sqrt{2} U_n \sin((n\omega t + 2\pi/3) + \theta_n) \end{bmatrix}, \quad (11)$$

where U_n and θ_n are respectively the rms voltage and initial phase angle, n is the harmonic order. When $n = 1$, it means three-phase fundamental voltage source:

$$\begin{bmatrix} U_{sa} \\ U_{sb} \\ U_{sc} \end{bmatrix} = \begin{bmatrix} \sum_{n=1}^{\infty} \sqrt{2}U_1 \sin(n\omega t + \theta_1) \\ \sum_{n=1}^{\infty} \sqrt{2}U_1 \sin((\omega t - 2\pi/3) + \theta_1) \\ \sum_{n=1}^{\infty} \sqrt{2}U_1 \sin((\omega t + 2\pi/3) + \theta_1) \end{bmatrix}. \quad (12)$$

Equation (12) is transformed into $(\alpha-\beta)$ reference frame:

$$\begin{bmatrix} U_{s\alpha} \\ U_{s\beta} \end{bmatrix} = C_{32} \begin{bmatrix} U_{sa} \\ U_{sb} \\ U_{sc} \end{bmatrix} = \sqrt{3} \begin{bmatrix} \sum_{n=1}^{\infty} U_n \sin(n\omega t + \theta_n) \\ \sum_{n=1}^{\infty} \pm U_n \sin(n\omega t + \theta_n) \end{bmatrix} \quad (13)$$

$$C_{32} = \sqrt{2/3} \begin{bmatrix} 1 & -1/2 & 1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{bmatrix} \quad (14)$$

The three-phase positive fundamental current template is given by Eq. (15):

$$\begin{bmatrix} i_{sa} \\ i_{sb} \\ i_{sc} \end{bmatrix} = \sqrt{2/3} \begin{bmatrix} \sin(\omega t) \\ \sin(\omega t - 2\pi/3) \\ \sin(\omega t + 2\pi/3) \end{bmatrix}. \quad (15)$$

Equation (13) is transformed to $(\alpha-\beta)$ reference frame:

$$\begin{bmatrix} i_{s\alpha} \\ i_{s\beta} \end{bmatrix} = C_{32} \begin{bmatrix} i_{sa} \\ i_{sb} \\ i_{sc} \end{bmatrix} = \begin{bmatrix} \sin(\omega t) \\ -\cos(\omega t) \end{bmatrix}. \quad (16)$$

According to the instantaneous reactive power theory, then:

$$\begin{bmatrix} p \\ q \end{bmatrix} = \begin{bmatrix} u_{s\alpha} & u_{s\beta} \\ u_{s\beta} & -u_{s\alpha} \end{bmatrix} \begin{bmatrix} i_{s\alpha} \\ i_{s\beta} \end{bmatrix}, \quad (17)$$

where DC and AC components are included:

$$\begin{bmatrix} p \\ q \end{bmatrix} = \begin{bmatrix} \bar{p} & + & \tilde{p} \\ \bar{q} & + & \tilde{q} \end{bmatrix}, \quad (18)$$

where p and q are passed through Low Pass Filter (LPF), and DC component are obtained by

$$\begin{bmatrix} \bar{p} \\ \bar{q} \end{bmatrix} = \begin{bmatrix} U_1 \cos(\theta_1) \\ U_1 \sin(\theta_1) \end{bmatrix}. \quad (19)$$

According to Eq. (17), transformation is made:

$$\begin{bmatrix} p \\ q \end{bmatrix} = \begin{bmatrix} u_{s\alpha} & u_{s\beta} \\ u_{s\beta} & -u_{s\alpha} \end{bmatrix} \begin{bmatrix} i_{s\alpha} \\ i_{s\beta} \end{bmatrix} = \begin{bmatrix} i_{s\alpha} & i_{s\beta} \\ -i_{s\beta} & i_{s\alpha} \end{bmatrix} \begin{bmatrix} u_{s\alpha} \\ u_{s\beta} \end{bmatrix}. \quad (20)$$

The fundamental voltages in $(\alpha-\beta)$ reference frame are:

$$\begin{bmatrix} U_{s\alpha} \\ U_{s\beta} \end{bmatrix} = \begin{bmatrix} i_{s\alpha} & i_{s\beta} \\ -i_{s\beta} & i_{s\alpha} \end{bmatrix}^{-1} \begin{bmatrix} \bar{p} \\ \bar{q} \end{bmatrix} = \begin{bmatrix} i_{s\alpha} & -i_{s\beta} \\ i_{s\beta} & i_{s\alpha} \end{bmatrix} \begin{bmatrix} \bar{p} \\ \bar{q} \end{bmatrix}. \quad (21)$$

The three-phase fundamental voltages are given by

$$\begin{bmatrix} U_{sa-f} \\ U_{sb-f} \\ U_{sc-f} \end{bmatrix} = C_{23} \begin{bmatrix} U_{s\alpha} \\ U_{s\beta} \end{bmatrix} = \sqrt{2}U_1 \begin{bmatrix} \sin(\omega t + \theta_1) \\ \sin(\omega t + \theta_1 - 2\pi/3) \\ \sin(\omega t + \theta_1 + 2\pi/3) \end{bmatrix}, \quad (22)$$

where

$$C_{23} = \sqrt{2/3} \begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & \sqrt{3}/2 \end{bmatrix}^T. \quad (23)$$

5 Logic control and switching generation

Recently, there has been an increase in the application of Fuzzy Logic Controllers (FLCs) for control of power electronic converters; these controllers have been shown to offer excellent dynamic responses in more power electronics application [37]. The fuzzy control rules are not derived from a heuristic knowledge of system behavior; neither precise mathematical modeling nor complex computations are needed. Fuzzy logic deal with problems that have vagueness, uncertainty or imprecision and uses membership functions with values varying between 0 and 1. There are four main parts for fuzzy logic approach; the first part is "fuzzification unit" to convert the input variable to the linguistic variable or fuzzy variable; the second part is "knowledge base" to keep the necessary data for setting the control method by the expert engineer; finally the "decision making logic" or the inference engine is the third part to imitate the human decision using rule bases and data bases from the second part [38, 39]. The final part is "defuzzification unit" to convert the fuzzy variable to easy understanding variable [38, 39]. The fuzzy controllers proposed in this paper are designed to improve compensation capability of shunt and series APFs by adjusting the error using fuzzy rules. The desired inverter switching signals are determined according the error between the injected and reference of voltage or current. In this case, the fuzzy logic controller has two inputs, error e and change of error de and one output S [40]. To convert it into linguistic variable, we use seven fuzzy sets: NL (Negative Large), NM (Negative Medium), NS (Negative Small), ZE (Zero), PS (Positive Small), PM (Positive Medium) and PL (Positive Large) [41]. Triangles or Triangular Membership Function (TMF) have been frequently used in several applications and are preferred due to simplicity, easy implementation, symmetrical along the axis [42]. The Fuzzy Inference Systems (FIS) combine the human knowledge to control the system [43]. Fig. 3 shows the normalized triangular and trapezoidal membership functions for the input and output variables. The fuzzy controller is characterized by:

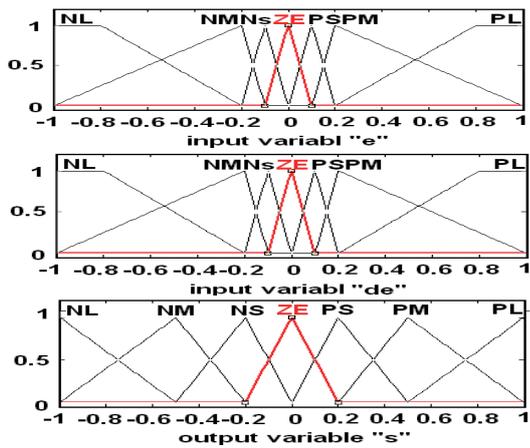


Fig. 3 Membership function (inputs and output variables)

- seven fuzzy sets for each input, seven fuzzy sets for output,
- triangular and trapezoidal membership function for the inputs and output,
- implication using the "min" operator,
- mamdani fuzzy inference mechanism based on fuzzy implication,
- defuzzification using the "centroid" method.

Errors for each phase are discretized by the zero order hold blocks; the error rate is derivative of the error and it is obtained by the use of unit delay block; the saturation block imposes upper and lower bounds on a signal [44]. When the input signal is within the range specified by the lower and upper limit parameters, the input signal passes through unchanged otherwise the input signal is outside these bounds in this case the signal is clipped to the upper or lower bound [20]. The outputs of these fuzzy logic controllers are used in generation of pulses switching signals of the seven-level inverter. The switching signals are generated by means of comparing a six carrier signals with the output of the fuzzy logic controller. The shunt APF control scheme based on seven-level (NPC) inverter using fuzzy controller is given by Fig. 4.

The logic control for the seven-level (NPC) inverter developed using Simulink is shown in Fig. 5.

Algorithm 1 generate switching pulses for seven-level (NPC) inverter based on the output voltage while respecting the midpoint M of an arm k is given.

6 Simulation results and discussion

Fig. 6 displays the model of the proposed UPQC system. The simulation is carried using Matlab-Simulink and SimPowerSystem software. The performances are evaluated

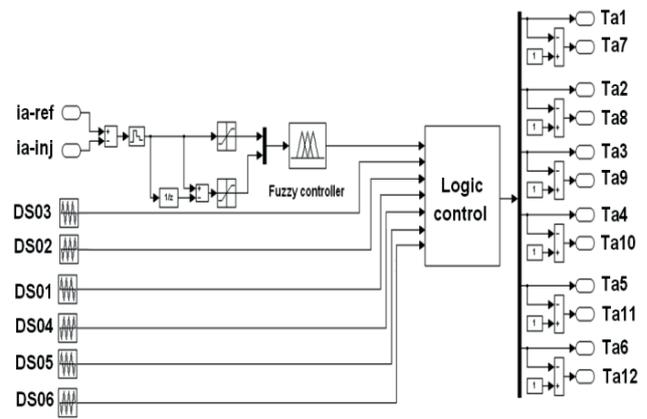


Fig. 4 Seven-level (NPC) Shunt APF control scheme

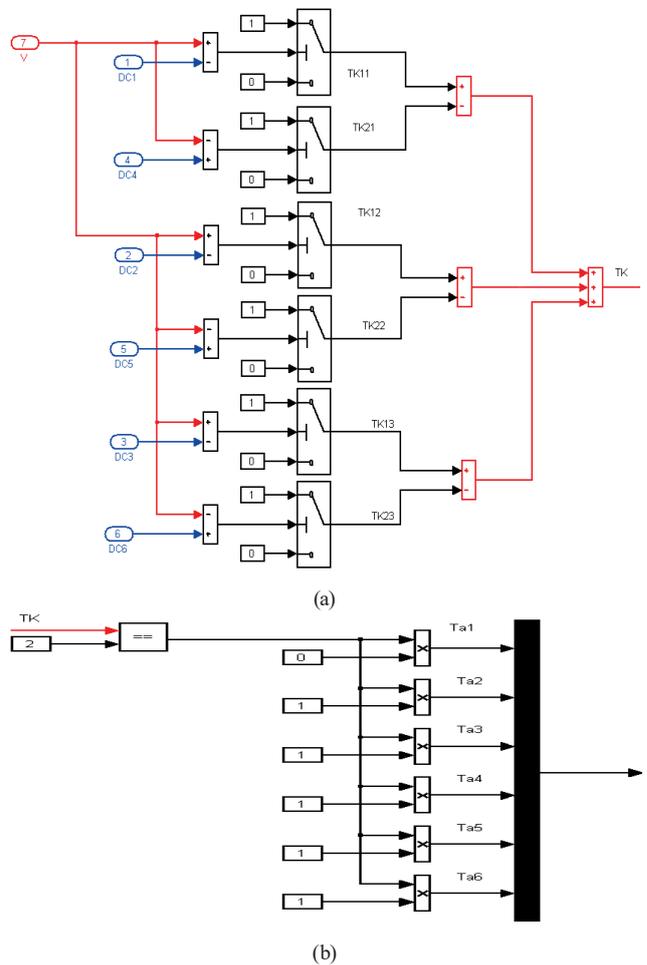


Fig. 5 Seven-level (NPC) inverter logic control, (a) TK evaluation, (b) pulses generation for upper leg in case of $TK = 2$ ($TK: -3, -2, -1, 0, 1, 2, 3$)

in terms of sags, swells and voltage unbalances compensation in steady state. The parameters of the proposed UPQC are $V_s = 220$ V, frequency $f_s = 50$ Hz, resistor $R_s = 0.1$ m Ω , inductance $L_s = 0.0002$ mH, resistor $R_1 = 48.6$ Ω , inductance $L_1 = 40$ mH, $C_{dc} = C_1 = C_2 = C_3 = C_4 = C_5 = C_6 = 3000$ μ F, resistor $R_c = 0.27$ m Ω , and $L_c = 0.8$ mH.

Algorithm 1 Seven-level (NPC) inverter switching pulses generation

If $V_{ref1} \geq V_{p1j}$, then $T_{k1j} = 1$;
 if $V_{ref1} < V_{p1j}$, then $T_{k1j} = 0$;
 if $V_{ref1} \leq V_{p1j}$, then $T_{k2j} = 1$;
 if $V_{ref1} > V_{p1j}$, then $T_{k2j} = 0$;
 $K = 1, 2, 3$ and $j = 1, 2, 3$,
 $TK = (T_{k11} - T_{k21}) + (T_{k12} - T_{k22}) + (T_{k13} - T_{k23})$;
 if $TK = 3$, then $VK = +U_{dc}/2$;
 if $TK = 2$, then $VK = +U_{dc}/3$;
 if $TK = 1$, then $VK = +U_{dc}/6$;
 if $TK = 0$, then $VK = 0$;
 if $TK = -3$, then $VK = -U_{dc}/2$;
 if $TK = -2$, then $VK = -U_{dc}/3$;
 if $TK = -1$, then $VK = -U_{dc}/6$.

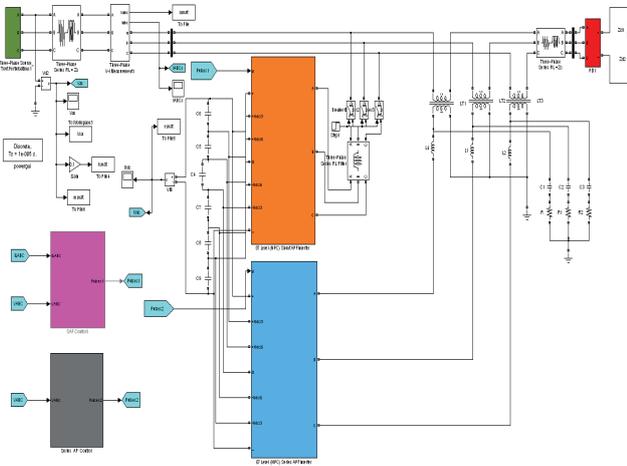


Fig. 6 Matlab-Simulink UPQC system model based on seven-level (NPC) inverter

6.1 Performances of UPQC system for all voltage disturbances compensation

The performance of proposed UPQC system is tested under all voltage disturbances simultaneously. The simulation results are shown in Fig. 7. The voltage sags (25%) is introduced voluntarily between $t_1 = 0.06$ s and $t_2 = 0.12$ s. After that, a voltage swells (35%) is introduced between $t_2 = 0.12$ s and $t_3 = 0.18$ s. The voltage harmonics is introduced between $t_3 = 0.18$ s and $t_4 = 0.24$ s. The unbalances is injected between $t_4 = 0.24$ s and $t_5 = 0.3$ s. After $t_5 = 0.3$ s the system is again at normal working condition. The waveform of source current before and after compensation is depicted in Fig. 7 (d), it is sinusoidal and in phase with the correspondent phase voltage. The proposed UPQC is capable to mitigate all voltage disturbances and does not show any significant effect of disturbance type present in the utility voltages on its compensation capability.

6.2 Dynamic performances of UPQC system for the sudden change of load

In order to evaluate the performance of the proposed UPQC system during transient condition, the load on the system is changed suddenly. The simulation results during this condition are shown in the Fig. 8. Before time $t_1 = 0.05$ s, the shunt and series APFs are not working, the source current is highly distorted. After $t_1 = 0.05$ s the shunt active filter is only on operation (the source current after compensation is nearly sinusoidal and in phase with the source voltage). When the sudden load current disturbance is introduced voluntarily between $t_2 = 0.1$ s and $t_3 = 0.2$ s, the UPQC controller acts immediately without any delay, the shunt APF injects a current equals to sum of harmonic.

In all dynamic conditions, the dc voltage is maintained constant and equal to the reference value $U_{dc-ref} = 800$ V using proportional integral voltage controller. It is observed that the dc voltage passes through a transitional period of 0.02 s before stabilization and reaches its reference with moderate peak voltage approximately equal to 3 V. Before Shunt AF application the source current is distorted with poor power factor, after compensation the source current shown in Fig. 8 (a) is sinusoidal and in phase with the source voltage for all voltage disturbances. The effectiveness of the UPQC in reducing the supply current and load voltage harmonics for all disturbances conditions is proved.

The line-neutral voltage U_{AN} (V) delivered by the seven-level (NPC) inverter used for the Shunt APF is shown in Fig. 9 and the line-to-line voltage U_{AB} (V) in Fig. 10.

The proposed UPQC system based on seven-level (NPC) inverter topologies has been validated through simulation using MATLAB-Simulink software and SimPowerSystem toolbox. Through visualization Fig. 7 (d) and Fig. 7 (g), we are able to conclude that the operation of the proposed UPQC is successful. Before the application of shunt APF, the source current is equal to non-linear load current; it is highly distorted and rich in harmonic with poor power factor. After compensation, the current becomes sinusoidal and the load voltage is instantly improved for separate or simultaneously voltage disturbances such us sags, swells, unbalances and harmonics. When the sudden load current disturbance is introduced between 0.1 s and 0.2 s, the UPQC controller acts immediately without any delay. The dc voltage is maintained at the reference value $U_{dc-ref} = 800$ V using PI controller. It is observed in Fig. 8 (b) that the dc voltage reaches its reference $U_{dc-ref} = 800$ V with moderate peak voltage approximately equal to 3 V.

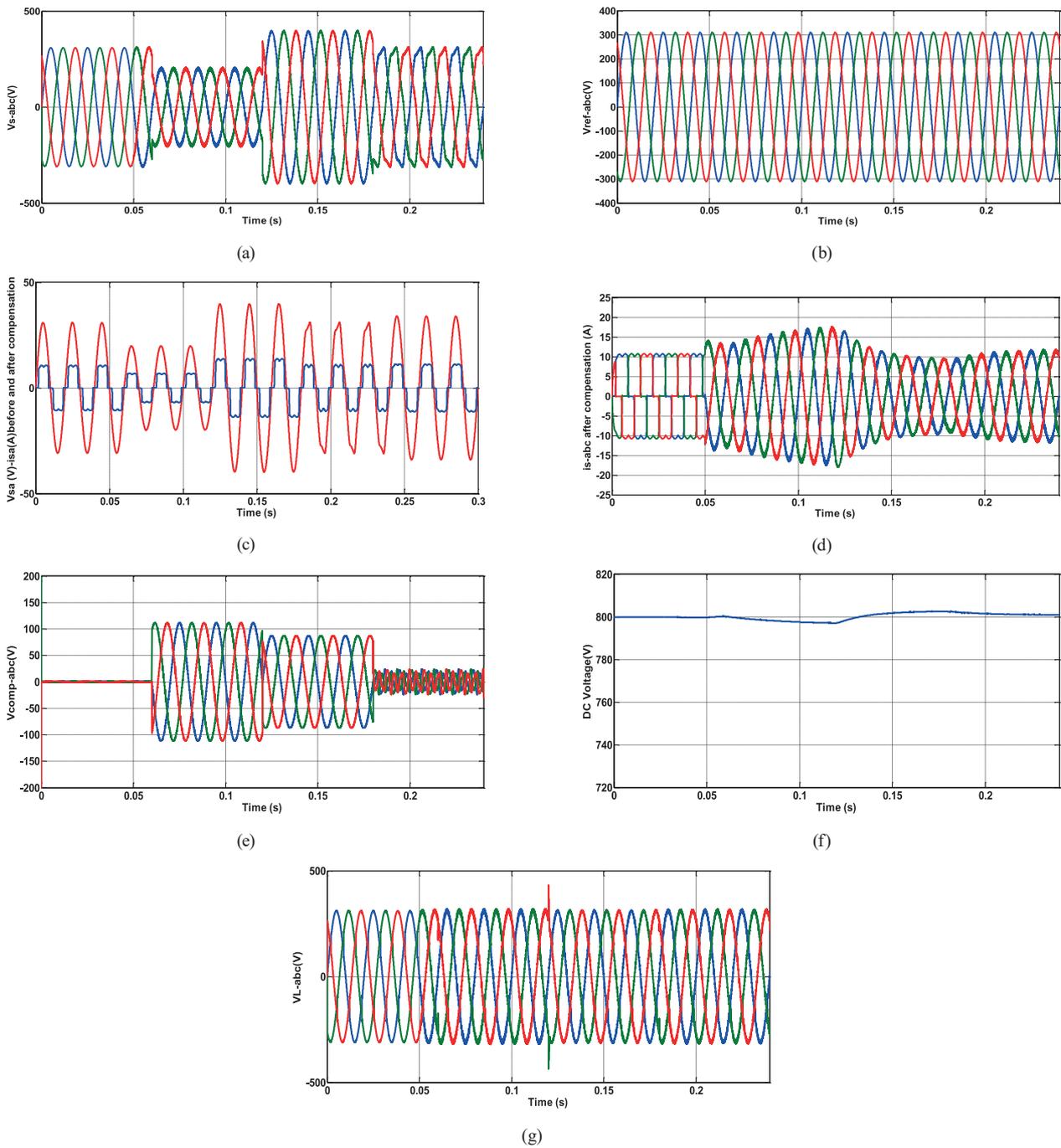


Fig. 7 UPQC performances for all voltage disturbances compensation, (a) load voltage before compensation, (b) reference voltages, (c) source current and voltage before compensation, (d) source current after compensation, (e) compensation voltages, (f) DC link voltage, (g) load voltage after compensation

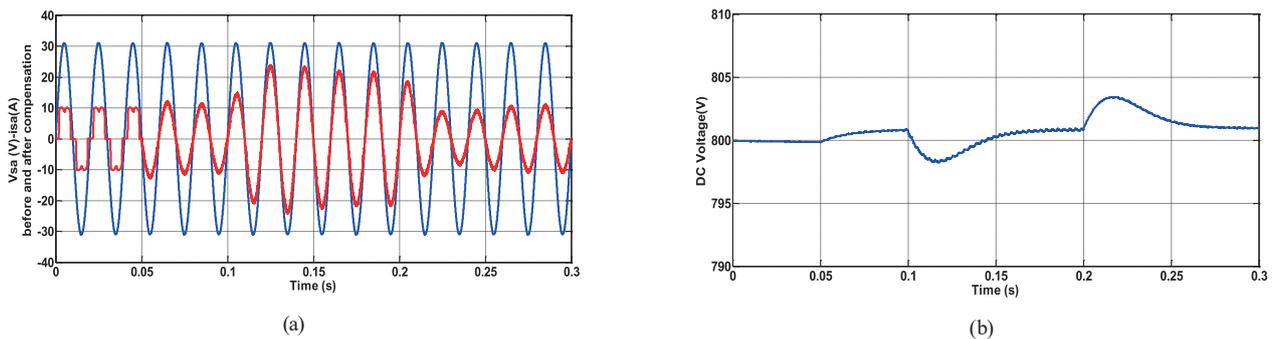


Fig. 8 UPQC performance in transient condition, (a) source current i_{sa} (A) and source voltage v_{sa} (V), (b) DC link voltage

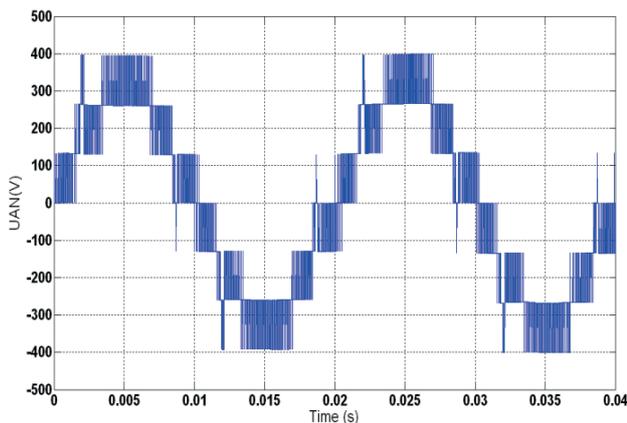


Fig. 9 Line to neutral voltage U_{AN} (V)

7 Conclusion

To enhance the power quality by reducing the source current harmonics and improving the voltage delivered to sensitive or critical loads, a novel UPQC configuration based on seven-level (NPC) inverter topologies has been proposed in this paper. The control strategy adopted is based on the instantaneous reactive power method for the series APF and synchronous reference frame detection method for the shunt APF. The developed model is validating through numerical simulation using Matlab-Simulink software and SimPowerSystems Toolbox. The performance

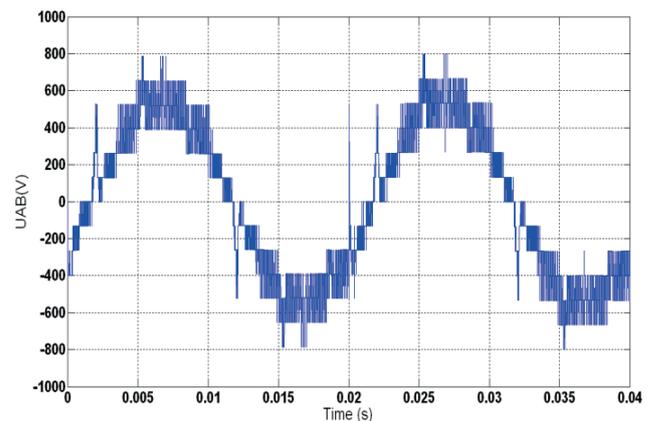


Fig. 10 Line-to-line voltage delivered by the seven-level (NPC) inverter U_{AB} (V)

of proposed UPQC systems has been found satisfactory for various power quality improvements like voltage harmonics mitigation, voltage sag, swell and unbalance compensation and current harmonic mitigation. The UPQC performance during transient conditions has been found satisfactory, the UPQC controller acts immediately without any delay in the operation with fast dynamic response. The result of this study may be useful for potential UPQC applications based on multi-level inverters.

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