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Parity Generators for Nanocommunication Systems Using QCA Nanotechnology

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Abstract

Quantum-dot cellular automata (QCA) nanotechnology has the capability to design highly-dense, ultra-low power, and high-speed digital circuits at ultra-deep sub-micron (ultra-DSM) level. QCA nanostructure provides a transistor-free operation that saves large energy dissipation as compared to the conventional metal oxide semiconductor field effect transistor (MOSFET) technology. In this paper, 3-input exclusive-OR (XOR) and exclusive-NOR (XNOR) gates are presented using QCA cells. XOR and XNOR (XOR-XNOR) gates are further utilized to design the 2-, 3-, 4-, and 5-bit even and odd parity generators. The QCA-based 3-input XNOR gate is constructed using only 10 QCA cells and two clock phases. The target of the presented designs is to use the minimum count of QCA cells in a simplistic way to form the higher bit-size parity generators. The comparative analyses for the different performance metrics are showing that the developed designs are performing well for the cell count, latency, area, and layout cost as compared to the existing designs. Energy dissipation for the designs is calculated to check the energy efficiency by using the QCA Designer-E and QCA Pro tools.

Keywords

XOR, XNOR, parity generator, energy dissipation, QCA, QCA Pro

1 Introduction

Area-efficient, high-speed, and low-power dissipation are the fundamental requirements in the field of very large-scale integration technology for today's portable gadgets. The technology scaling is needed to get an area-efficient design. But, the scaling of MOSFET technology is not feasible under the ultra-DSM regime due to the material's fundamental limitations [1]. Hence, QCA nanotechnology is the best possible replacement for the MOSFET technology in the ultra-DSM regime. QCA circuits are highly-dense, which provide high-speed and low-power operation as compared to other available alternative options for the MOSFET technology [2]. Therefore, researchers are working for the advancement of QCA nanotechnology.

The fundamental unit for QCA nanotechnology is the QCA cell. A QCA cell consists of four quantum-dots [3]. Cell-to-cell interaction permits the data flow in QCA nanotechnology. Unlike other technologies, no physical charge is available in a QCA cell that makes it an energy-efficient technology. A QCA cell generates the binary value in terms of the availability of the electrons in the quantum-dots. Columbic force limits the two electrons in a QCA cell [4]. Hence, two types of polarizations; +1 and −1 are possible in a cell [5, 6]. When polarization (P) is +1 then it shows binary 1 and when P is −1 then it shows binary 0. Fig. 1 is showing the binary equivalent values in a QCA cell. Black circles are depicting the position of the electrons.

The data flow in a QCA circuit is possible if the QCA cells are arranged in a form of wire. It uses the concept of cell-to-cell interaction and exhibits the Columbic force. Fig. 2 is depicting a QCA wire. The length of the wire is decided by the number of QCA cells in a QCA design [7, 8].

(a) (b)

Fig. 1 Binary logic representation in a QCA cell (a) logic 1 or $P = +1$ (b) logic 0 or $P = -1$

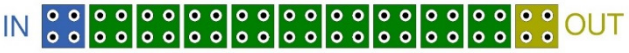

Fig. 2 QCA wire used for data flow

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A complex QCA circuit requires passing the wires from different locations. For that purpose, crossover methods are utilized to pass the QCA wires. The commonly used crossover methods are planar, multilayer, and logical [9, 10]. The planar crossover method consists of both types of QCA cells i.e. regular (90°) and rotated (45°) cells. The multilayer crossover method contains multiple layers in a QCA circuit, while precise clocking information is mandatorily required for the logical crossover [11].

The clocking system is the backbone of QCA nanotechnology. It controls the transfer of information from one end to another end because the data flow in a QCA circuit changes the energy barrier. The clocking system includes four phases: switch, hold, release, and relax. The phase difference between the consecutive clock phases is 90° [12, 13]. The QCA clocking system is displayed in Fig. 3.

The switch phase is the first phase, where polarization is started. QCA cell is completely polarized in the second phase. Thus, the movement of the data is only possible in the switch and hold phases. The release phase is the reverse operation of the switch phase, where the cell is going to de-polarize. Relax phase is showing the inverse operation of the hold phase, where the QCA cell is fully de-polarized.

It is necessary to design the fundamental logic gates first before designing any complex circuit. The fundamental logic gates are AND, OR, and NOT. The specific configuration of the QCA cells is the basis for the different logic designs. AND and OR logics are generated by using the majority voter (MV) concept [14]. The fundamental logic gates using the QCA nanotechnology are presented in Fig. 4.

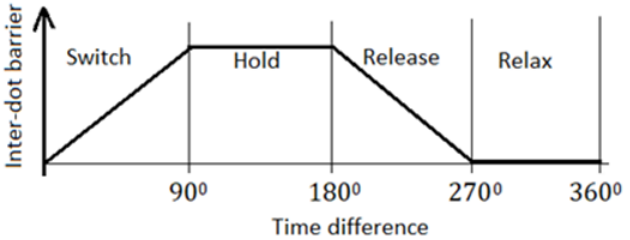


Fig. 3 QCA clocking system

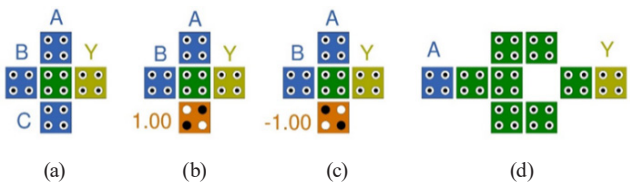


Fig. 4 Key QCA gates (a) MV (b) 2-input OR (c) 2-input AND (d) inverter or NOT

MV consists of three primary inputs; *A*, *B*, *C*, and one output *Y*. The input-output relationship for MV is given in Eq. (1):

$$Y(A,B,C) = AB + BC + CA\,. \tag{1}$$

From Eq. (1), a 2-input AND gate can be designed if the input $C = 0$. 2-input OR gate can be implemented if the input $C = 1$.

This research paper presents the nanostructures for the 3-input XOR-XNOR gates using the minimum number of QCA cells. The presented XOR-XNOR gates are further utilized to design the 2-, 3-, 4-, and 5-bit even and odd parity generators.

The paper is further divided into the following sections:

- The existing literature is mentioned in Section 2.
- The different bit-size parity generator circuits are proposed in Section 3.
- Section 4 compared the QCA designs with the existing works.
- The conclusion of the paper is given in Section 5.

2 Previous works

The parity generator is commonly used in the communication system. Even and odd are the two types of parity generators. If the number of 1's in a message is even then it is even parity, otherwise, it is odd parity. Even and odd parity generators are designed with the help of XOR and XNOR gates, respectively. So, many researchers have developed QCA-based XOR-XNOR gates and parity generators. The previous works are briefed in Section 2.

NAND-NOR-inverter and 5-input MV were utilized for an XOR gate [15]. The proposed XOR gate has 27 QCA cells and 0.75 latency in a single layer. No crossover was required for the XOR gate. A 4-bit parity generator was also proposed using the proposed XOR gate. The 4-bit parity generator uses a total of 85 QCA cells and 1.25 latency.

A 2-input XOR gate using a single layer was proposed [16]. It has 28 QCA cells and 0.75 latency. No crossover was used for the design. A 4-bit parity generator was developed based on the proposed XOR gate. The 4-bit parity generator uses a total of 87 QCA cells and 1.75 latency.

Two novel structures for the XOR gate were proposed [17]. The best proposed XOR gate consists of 20 QCA cells and 0.75 latency. A 4-bit parity generator was developed. The 4-bit parity generator has 86 QCA cells and 1.50 latency. Multi-layer crossover method was used for the design of a 4-bit parity generator.

An XOR gate using 27 QCA cells and 0.75 clock latency was proposed [18]. A 4-bit parity generator was reported based on the XOR gate. The 4-bit parity generator uses a total of 85 QCA cells and 1.25 latency.

A 3-input XOR gate was proposed using explicit cell interaction [19]. The proposed 3-input XOR gate can be used as a 2-input XOR gate by fixing an input. Therefore, cell count, latency, and layout area are the same for 2- and 3-input XOR gates. The proposed structure uses only 17 cells and 0.50 latency.

The novel structures for 2-input XOR-XNOR gates were developed using 13 QCA cells and 0.25 latency [20]. A single-layered 4-bit parity generator was further designed using 40 cells and 0.50 latency.

A QCA layout for a 3-input XOR gate was proposed using 14 QCA cells and 0.50 latency [21]. One input is situated inside the circuit, which creates an issue during the design of certain logic.

2- and 3-input XOR-XNOR gates were investigated [22]. The minimum numbers of QCA cell-based 2- and 3-input XOR-XNOR gates are consisting of 11 QCA cells and 0.50 clock latency.

A 2-input XOR gate was developed using 11 QCA cells and 0.25 clock latency [23]. The layout is single-layered without any crossover.

3- and 5-input MV gates were utilized for the formation of the 2-input XOR gate [24]. A total of 29 QCA cells and 0.75 clock latency were applied for the suggested 2-input XOR gate. A 4-bit parity generator was also formed using the suggested 2-input XOR gate. The 4-bit parity generator contains 92 QCA cells and 1.75 clock latency.

3 Proposed designs

XOR-XNOR gates are very important logic and are commonly used in many computer-related applications such as arithmetic operation, error detection and correction, code converters, etc. Many researchers have designed XOR-XNOR gates using QCA nanotechnology as reported in Section 2. But, these are limited by the number of cells and clock latencies. In Section 3, novel structured and single-layered different bit-size parity generators are proposed using QCA cells. 3-input XOR-XNOR gates contain three primary inputs (A, B, C) and one external output (Y). The output response for the primary input combinations of the 3-input XOR-XNOR gates is provided in Table 1.

It can be observed from Table 1 that the output of the XOR gate; Y (XOR) will be at logic 1 if the number of 1's in the primary input combination is odd. It means XOR logic can be used as an even parity generator. Similarly,

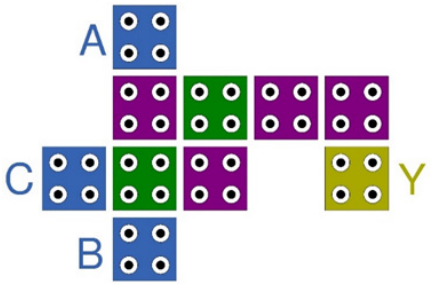
Table 1 Truth table for the 3-input XOR-XNOR gates

A	B	C	Y (XOR)	Y (XNOR)
0	0	0	0	1
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	0

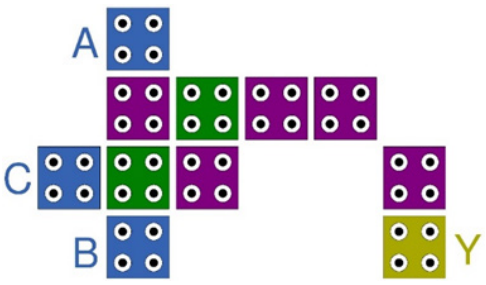
XNOR logic is treated as an odd parity generator because Y (XNOR) will be at logic 1 if the number of 1's in the primary input combination is even. The QCA nanostructures for the 3-input XOR-XNOR gates are given in Fig. 5. All the proposed QCA layouts are designed and simulated by using the QCA Designer-E tool [22].

The presented XOR-XNOR gates generate cell-to-cell interaction to form the logic. Therefore, the 3-input XNOR gate contains only 10 QCA cells and 0.50 clock latency. The 3-input XOR gate is obtained by inverting the output of the XNOR gate as shown in Fig. 5 (b). The 3-input XOR gate contains only 11 QCA cells and 0.50 clock latency. The input-output responses for the nanostructured 3-input XOR-XNOR gates are shown in Fig. 6.

2-input XOR-XNOR gates can be achieved using 3-input XOR-XNOR gates, where one input is fixed at a certain polarization value. It can also be verified by Table 1. From Table 1, if input C is fixed at logic 0 then the 3-input XNOR



(a)



(b)

Fig. 5 QCA-based 3-input gate (a) XNOR (b) XOR

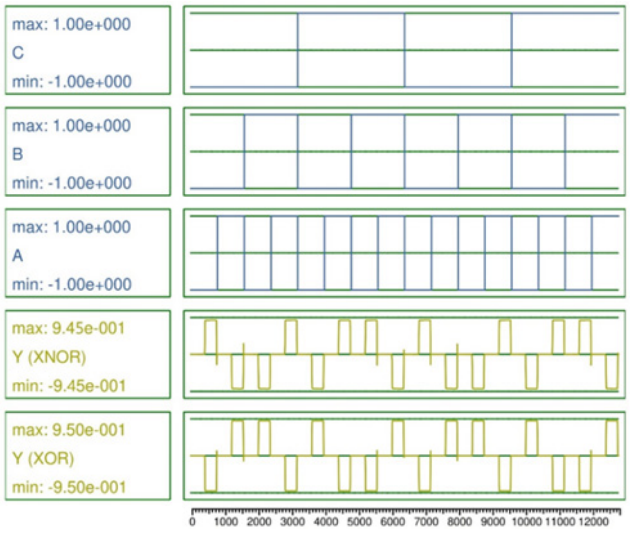


Fig. 6 Input-output responses for the 3-input XOR-XNOR gates

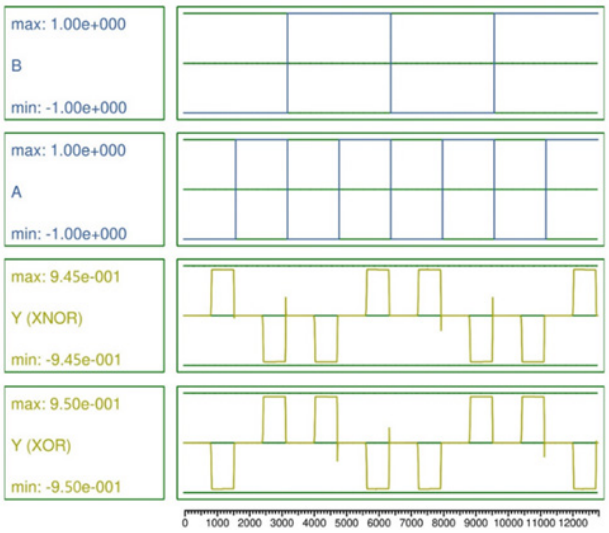


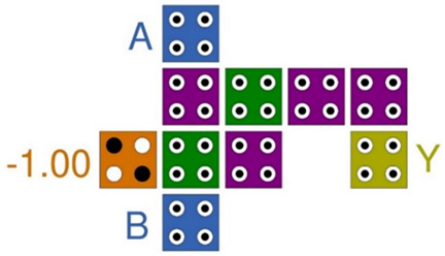
Fig. 8 Input-output responses for the 2-input XOR-XNOR gates

gate behaves as a 2-input XNOR gate. Similarly, if input *C* is fixed at logic 1 then the 3-input XNOR gate is behaving as a 2-input XOR gate. The layouts for the 2-input XOR-XNOR gates are presented in Fig. 7.

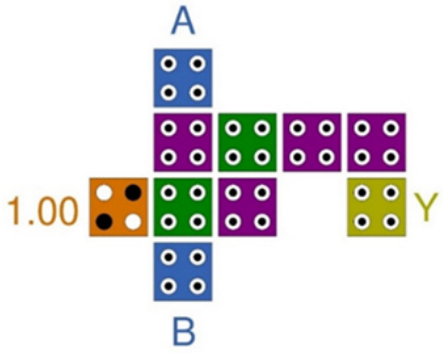
The input-output responses for the 2-input XOR-XNOR gates are shown in Fig. 8.

The 3-input XOR-XNOR gates are further used for the designing of the different bit-size parity generators. A 4-bit parity generator is further designed using the 3-input XNOR gates. Two 3-input XNOR gates are connected in series to form the 4-bit parity generator. The layouts for the proposed 4-bit parity generators using the 3-input XNOR gates are depicted in Fig. 9.

The proposed 4-bit XNOR (odd parity) and XOR (even parity) logics consist of only 19 QCA cells and 0.75 latency. The input-output responses for the 4-bit parity generators are depicted in Fig. 10.

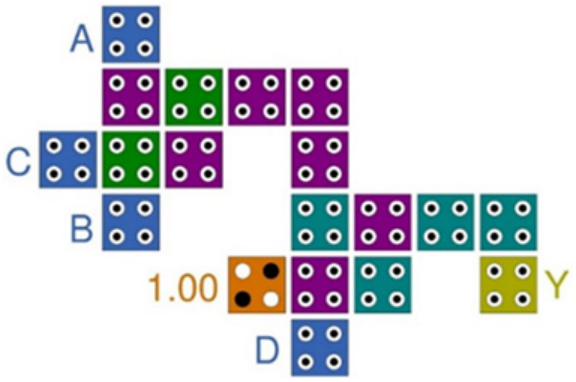


(a)

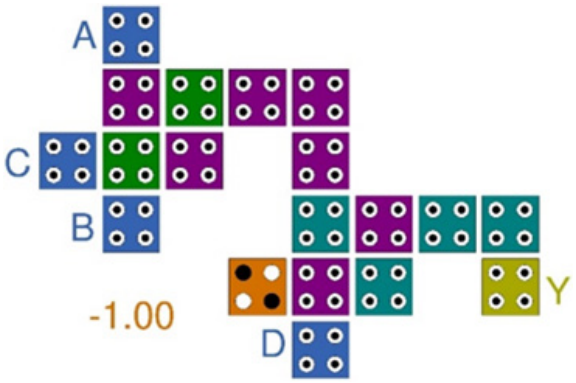


(b)

Fig. 7 Nanostructured 2-input gate using QCA cells (a) XNOR (b) XOR



(a)



(b)

Fig. 9 Proposed 4-bit parity generators using QCA nanotechnology (a) XNOR (b) XOR

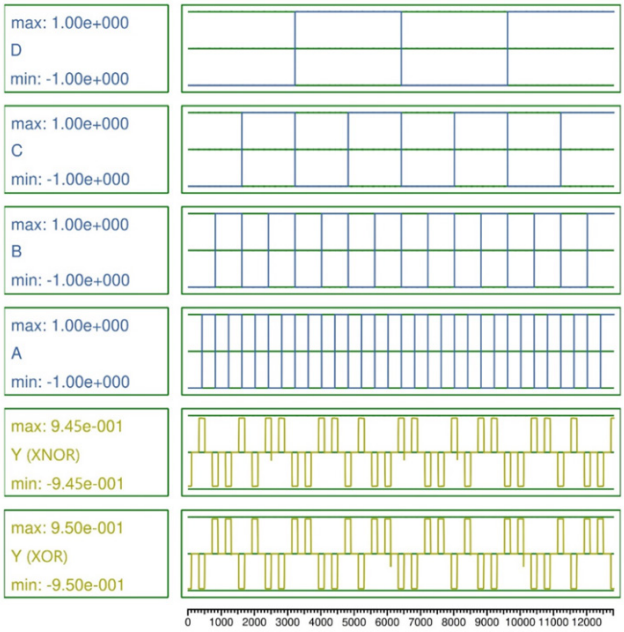


Fig. 10 Input-output responses for the proposed 4-bit XOR-XNOR gates

The layouts for the 5-bit parity generators are also designed in a similar manner and shown in Fig. 11. Here, odd parity is generated using the inversion of logic at the output.

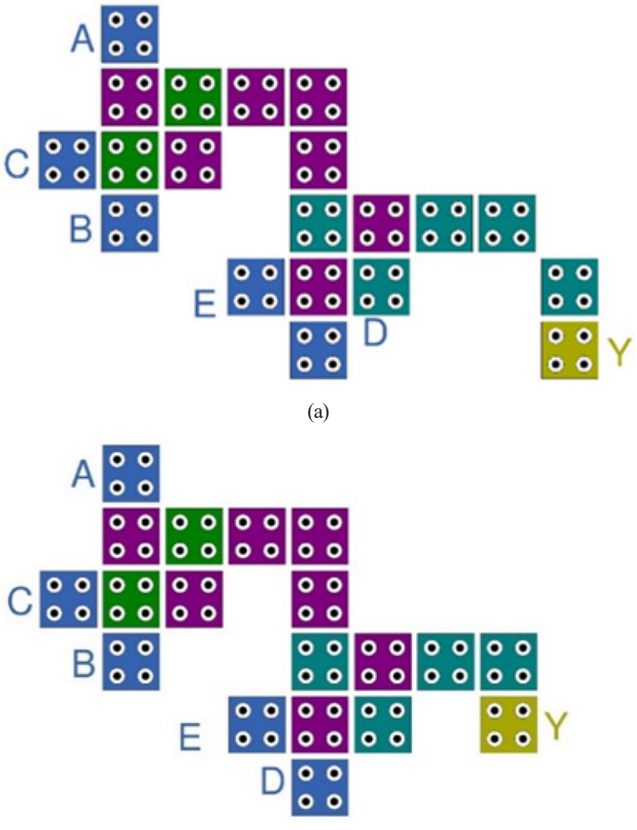


Fig. 11 Proposed 5-bit parity generator using QCA nanotechnology (a) XNOR (b) XOR

The input-output responses for the 5-bit parity generators are depicted in Fig. 12.

From the implementation of 2-, 3-, 4-, and 5-bit XOR-XNOR gates, it can be concluded that any bit-size parity generator can easily be designed using the 3-input XOR-XNOR gates. In the case of an even number ($2n$, n = 1, 2, 3, …) of parity bit-size, the number of QCA cells, latency, and layout area are the same in odd and even parity generators. The XOR gate produces even parity, while the XNOR gate generates odd parity. Therefore, higher bit-size even and odd parity generators can easily be implemented using the 3-input XOR-XNOR gates. The 3-input XOR-XNOR gates can also be utilized for the formation of different circuits such as adders, subtractors, code converters, comparators, shift registers, encryption methods, etc.

4 Comparison and analysis

In Section 4, the existing similar QCA designs are compared with the developed designs and analyzed. In this paper, 3-input XOR-XNOR gates are presented using QCA nanotechnology. 2-, 4-, and 5-bit parity generators are further implemented using the 3-input XOR-XNOR gates. The proposed designs are compared with the existing designs for performance evaluation. No crossover is required for any developed design. QCA layouts and the input-output responses are obtained by using the QCA Designer-E simulation tool. The default values of Bistable approximation are applied for the QCA circuits for the comparison of the different performance metrics [25].

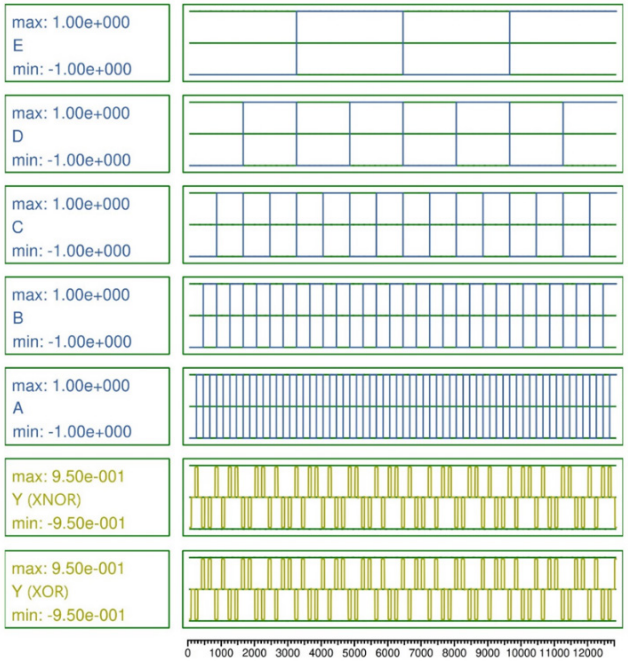


Fig. 12 Input-output responses for the proposed 5-bit XOR-XNOR gates

The comparisons of the different performance metrics are taken as the number of QCA cells, total cell area, total covered layout area, % utilization of area, latency/clock, and layout cost of the circuits. The existing similar works mentioned in Section 2 have been taken for comparison purposes. The comparison among the different bit-size parity generators is reflected in Table 2.

The computation of the total cell is showing the total used QCA cells in a layout. The area of a QCA cell is 18 nm × 18 nm. The cell area is estimated by the product of the total cells and the area of a QCA cell. The total covered layout area is evaluated by the multiplication of the total number of rows, the total number of columns, and the area of a QCA cell. The total QCA cells utilized in the horizontal plane are the number of columns, while the total QCA cells utilized in the vertical plane are the number of rows. Area utilization is the ratio of the total cell area to the total covered layout area. The logic delay of the QCA circuits is measured by checking the utilized QCA clocking system. Therefore, clock latency is the number of used clock phases for obtaining a proper function. A large latency shows a large input-output delay. The product of cells, covered area, and clock latency is used for the estimation of layout cost [21]. Low design cost is mandatory for an efficient layout.

The proposed parity generators are having the minimum number of QCA cells as observed in Table 2. It helps to reduce the total cell area. The proposed 4-bit parity generator consists of only 19 QCA cells, while the best-reported existing 4-bit parity generator [20] contained 40 QCA cells. The minimization of the number of QCA cells is possible only with the help of the optimized 3-input XOR-XNOR gates.

The energy-efficient capability of the QCA circuits is also measured. The QCA Designer-E and QCA Pro tools are used for the estimation of energy levels [25, 26]. The whole QCA layout is divided into many coordinates. It depends on the horizontally and vertically used QCA cells in a layout. The QCA Designer-E works for the summation of the energy levels of all the coordinates. The different

Table 2 The comparisons for different parity generators

Layout	Total cell	Cell area (μm²)	Covered area (μm²)	% area utilization	Clock	Layout cost
			2-bit			
[15]	27	0.009	0.016	56.25	0.75	0.324
[16]	28	0.009	0.017	52.94	0.75	0.357
[17]	20	0.006	0.016	37.50	0.75	0.240
[18]	27	0.009	0.018	50.00	0.75	0.365
[19]	17	0.006	0.016	37.50	0.50	0.136
[20]	13	0.004	0.008	50.00	0.25	0.026
[22]	11	0.004	0.008	50.00	0.50	0.044
[23]	11	0.004	0.008	50.00	0.25	0.022
[24]	29	0.009	0.020	45.00	0.75	0.435
This paper	10	0.003	0.006	50.00	0.50	0.030
			3-bit			
[19]	17	0.006	0.016	37.50	0.50	0.136
[21]	14	0.005	0.005	100.00	0.50	0.035
[22]	11	0.004	0.008	50.00	0.50	0.044
This paper	10	0.003	0.006	50.00	0.50	0.030
			4-bit			
[15]	85	0.028	0.073	38.36	1.25	7.756
[16]	87	0.028	0.072	38.89	1.75	10.962
[18]	85	0.028	0.078	35.90	1.25	8.288
[20]	40	0.013	0.035	37.14	0.50	0.700
[24]	92	0.030	0.087	34.48	1.75	14.007
This paper	19	0.006	0.016	37.50	0.75	0.228
			5-bit			
This paper	19	0.006	0.016	37.50	0.75	0.228

energy components are; the clock energy of a cell (*E_clk*), input-output energy (*E_io*), energy bath (*E_bath*), input energy (*E_in*), environment energy (*E_env*), and the output energy (*E_out*) [27]. The computation of the energy error (*E_Error*) is provided in Eq. (2) [28]:

$$E\_error = E\_env - E\_clk - E\_io\,. \tag{2}$$

Ideally, no energy is dissipated to the environment, but practically, few are dissipating in the environment during the de-polarization state. The positive value of the energy is showing that it is transferred to the clock energy, input-output energy, and environment energy.

During the calculation of the energy dissipation in the QCA Designer-E tool, the default values of the Coherence simulation engine are used. The sample size is 500,000 for running the simulation. Table 3 depicts the total and average energy bath ($\sum E\_bath$) per clock cycle with errors for the proposed parity generators. No existing work is showing the energy estimation using the QCA Designer-E tool. So, the comparison is not possible with the existing similar designs.

Here, *E_error* is negative because $\sum E\_clk + E\_io > E\_env$. Energy dissipation and the corresponding *E_error* values are increasing for the QCA circuits having a large number of cells and can be verified easily from Table 3.

The energy dissipations for the proposed parity generators are also calculated using the QCA Pro tool. QCA Pro tool is widely accepted for the estimation of energy dissipations for the QCA circuits. The approximation method is utilized in the QCA Pro to estimate the energy dissipation values [29, 30]. Leakage and switching energy dissipation are the two types of energy dissipation calculations in the QCA Pro tool. Three-dimensional (3D) Coherence and energy vectors are used for the energy dissipations in the QCA Pro tool. Energy dissipation for a clock cycle from $-L$ to L is shown in Eq. (3) [30]:

$$E_{diss} = \frac{\hbar}{2}\int_{-L}^{L}\vec{\Gamma}\cdot\frac{d\vec{\lambda}}{dt}dt = \frac{\hbar}{2}\left(\left[\vec{\Gamma}\cdot\vec{\lambda}\right]_{-L}^{L} - \int_{-L}^{L}\vec{\lambda}\cdot\frac{d\vec{\Gamma}}{dt}dt\right). \tag{3}$$

Here, $\hbar$ is the plank's coefficient, $\vec{\Gamma}$ is the 3D energy vector, and $\vec{\lambda}$ is the 3D Coherence vector. The QCA Pro tool estimates the energy dissipations for the three (0.5, 1.0, 1.5) Kink energy levels. Kink energy shows the energy level cost for the +1 and −1 polarized of the two cells. Kink energy for the neighboring cells (i, j) is given in Eq. (4):

$$E_{i,j} = \frac{1}{4\pi\varepsilon_0\varepsilon_r}\sum_{n=1}\sum_{m=1}\frac{q_{i,n}q_{j,m}}{\left|r_{i,n} - r_{i,m}\right|}\,. \tag{4}$$

Table 4 lists the average values of the leakage and the switching energy dissipations for all the Kink energy levels.

Table 3 Energy dissipation using the QCA Designer-E tool for the developed circuits

Parity generator	Total energy bath (eV)	±Error (eV)	Average energy bath (eV)	±Error (eV)
2-bit	4.55e-003	−4.53e-004	4.14e-004	−4.12e-005
3-bit	9.57e-003	−1.06e-003	8.70e-004	−9.60e-005
4-bit	1.61e-002	−1.72e-003	1.46e-003	−1.57e-004
5-bit	1.98e-002	−2.14e-003	1.80e-003	−1.95e-004

Table 4 Average energy dissipation for different layouts using the QCA Pro

Layout	Leakage (meV)			Switching (meV)			Total (meV)		
	0.5 E_K	1.0 E_K	1.5 E_K	0.5 E_K	1.0 E_K	1.5 E_K	0.5 E_K	1.0 E_K	1.5 E_K
2-bit									
[15]	9.58	27.00	46.32	27.92	22.89	18.69	37.50	49.89	65.01
[16]	10.78	28.57	48.15	25.43	21.71	18.40	36.21	50.28	66.55
[20]	3.28	9.90	17.83	19.62	17.16	14.85	22.90	27.06	32.68
This work	2.46	7.39	12.54	7.53	6.26	5.16	9.99	13.65	17.70
3-bit									
[19]	7.30	17.77	28.56	8.61	6.57	5.15	15.91	24.34	33.71
This work	2.90	7.78	13.14	8.35	6.92	5.73	11.25	14.70	18.87
4-bit									
[15]	31.01	85.51	146.64	89.27	74.81	62.48	120.28	160.32	209.12
This work	5.84	14.98	26.13	9.72	7.54	7.07	15.56	22.52	33.20
5-bit									
This work	6.38	16.47	27.26	13.52	10.86	8.79	19.90	27.33	36.05

Very few previously published similar works have reported the average energy dissipations for the parity generators.

Power dissipation mappings are also obtained for all the Kink energy levels. The mappings for the proposed parity generators are illustrated in Fig. 13 at 2 K temperature and 1.5 E_K Kink energy level.

5 Conclusion

High-power dissipation and non-scalability in the ultra-DSM regime are the most challenging problems for the MOSFET technology. QCA nanotechnology is an advanced alternative technology, which can replace the MOSFET technology completely in near future. QCA nanotechnology provides area-efficient designs with minimum energy dissipation. In a communication system, it is a difficult task to convey a message safely. Parity generators are widely used for sending information from source to destination securely. Parity bits are added at the source side so that the encoded message reached the destination without malpractice of the information. Therefore, this paper develops 2-, 3-, 4-, and 5-input parity generators using QCA nanotechnology. The developed designs are novel, single-layered, optimum, and without any cross-over. The proposed design layouts are comprehensively analyzed and compared with the existing similar designs by considering the total cells, total layout area, total covered layout area, % area utilization, clock, and layout cost.

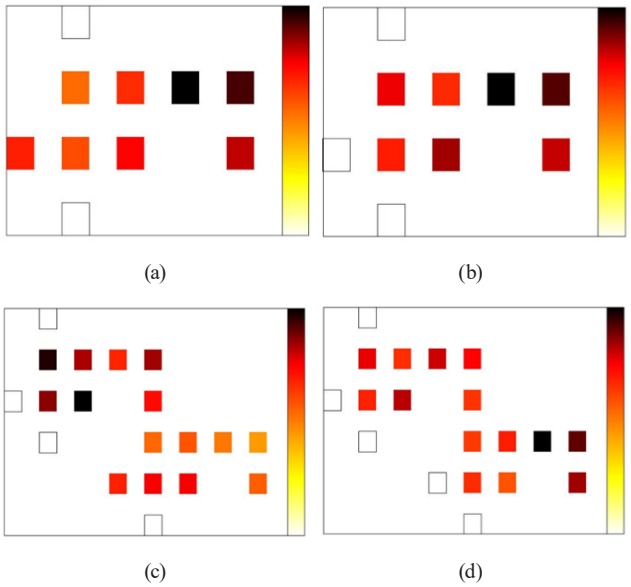


Fig. 13 Power dissipation mapping at 1.0 E_K for the proposed parity generator (a) 2-bit (b) 3-bit (c) 4-bit (d) 5-bit

The proposed 4-bit parity generator reduces 54.29% the layout area in comparison with the best existing work. The calculations of the energy dissipations are taken by using the QCA Designer-E and QCA Pro tools. No existing work has estimated energy dissipation using the QCA Designer-E tool. The proposed 4-bit parity generator has 87.06% less average total energy dissipation for 0.5 Kink energy level using the QCA Pro tool in comparison with the existing best work.

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