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Adaptive Interval Type II Fuzzy Logic Controller with Interface Inductor Bank Pulse Generator Based Three-Phase Four-Wire DSTATCOM Device for Power Quality Improvement

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Abstract

It goes without saying that the electrical distribution system is facing many power-quality issues these days. The main cause of these issues is the wide spread of nonlinear load integrated with the electrical distribution system. Moreover, the DSTATCOM device with interface inductor has different control algorithms. These encompass proportional integral controller, Interval type I fuzzy logic and interval type II fuzzy logic along used for improving the power quality issues. Before integration with the electrical distribution grid, these controllers need the tune processing. The combination of DSTATCOM with the load, which is different from the tuned one, and the wrong selection of the interface inductor leads to the failure of DSTATCOM device in the mitigation of source current harmonics. This study suggests that the use of adaptive interval type II fuzzy logic with the interface bank pulse generator based DSTATCOM device with self-tunning process and self-selection of the interface inductor would be suitable for all load types integrated into the distribution system within the rated power of DSTATCOM device. The adaptive interval type II fuzzy logic with the interface bank pulse generator based DSTATCOM device mitigates the source current harmonics and gives fast DC capacitor bus voltage response. Employing the suggested control algorithm based DSATCOM device makes the DC capacitor voltage signal settling time at almost 50 ms and total harmonic distortion of the source current at almost 4% for all cases of the load connected with the distribution system within the rated power of DSTATCOM device.

Keywords

DSTATCOM device, interval type II fuzzy logic controller, interface inductor bank, harmonics mitigation, source power factor improving

1 Introduction

The need for green energy arises these days to decrease global warming which become one of the community priorities. The governments started to depend on renewable energy sources and apply them to the distribution grid. It is predicted that the application of it as a primary energy supply will reach the percentage of 63% in 2050 [1, 2]. The proliferation of unbalanced loads and nonlinear loads these days which most of them are reactive power consumers such as fans and pumps decrease the power factor and value of active power able to flow in the distribution system unless increasing the size of transmission and distribution grids [3]. The brushless DC motor BLDC structure of diode bridge rectifier DBR with DC-link capacitor consumes non-sinusoidal current from the source causing the worsening of the source current THD to the value of 65–70% with a low power factor of 0.6–0.7 [4, 5]. The utilization of renewable energy along with nonlinear loads spread power quality issues in the distribution grids. These power issues are reactive power burden, harmonic current, load unbalanced, excessive neutral current, power factor reduction, damaging appliances and overheating [6, 7]. The hospital contains many sensitive devices that need a pure sinusoidal source current and voltage waveforms to work, and stopping these devices such as intensive care unit and critical care unit may lead for loss of human life. The need of supplying these sensitive loads with a pure active power, the need to overcome the burdens of renewable energy spreading and wide spread of using nonlinear loads make the utilization of power quality improvement devices necessary in electrical distribution grids [8, 9].

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Passive filters or static VAR compensators are used to improve the power quality in the distribution system but it has drawbacks such as causing of additional power losses because of the large inductors and capacitors size, limited harmonic bandwidth elimination because it tuned to specific harmonics and in some cases the causing of the parallel resonance with the system impedance which may affect the system impedance and load characteristic [10]. The power factor conditioner PFC can guide the power factor to unity value and eliminate the harmonic, but the switches may face high voltage stress in some conditions. The shunt active power filter is a solution for mitigating the harmonics and improving the power factor [11]. Distributed flexible AC transmission system DFACTS devices contain distribution static compensator DSTATCOM, dynamic voltage restorer DVR and unified power quality conditioner UPQC. They used recently to improve the power quality issues due to the application of renewable energy and it is proved that they are better than the passive filters or static VAR compensators. The first type of these devices is connected in shunt to improve the power quality of the current such as DSTATCOM. The second type of DFACTS is connected in series to enhance the power quality of the voltage at the point of common coupling such as DVR. The third type can mitigate the power quality issue in both the current and the voltage such as UPQC [12]. DSTATCOM device offers many features over the other custom power devices CPDs by injecting the necessary reactive power needed by loads and supporting the voltage during the connecting or disconnecting of the loads [13]. The DSTATCOM device three phase three wire is widespread in the distribution system for mitigating of harmonics and power factor improving but it can't deal with the excessive neutral current in the three phase four wire distribution system which in some cases reached 1.73 times of the phase current. Three phase four wire DSTACOM device came into light in the three phase four wire distribution system as a solution to deal with the excessive neutral current [14, 15].

The effectiveness of DSTATCOM device depends on the control algorithm. The conventional algorithms used to control DSTATCOM device are instantaneous reactive power theory, Synchronous reference frame theory, instantaneous symmetrical component and cross vector theory, while the adaptive control algorithms are adaptive linear element theory (Adaline), adaptive least mean square theory (ALMS) and adaptive recursive least square (ARLS). The researcher started to validate and apply the adaptive algorithms because of their simple structure, the increment of control response speed, decreasing the steady state error and they need less computational efforts [1, 16].

Proportional Integral (PI) is one of the conventional controllers which is used to control the capacitor DC voltage. The researcher started to apply artificial neural network (ANN), type I fuzzy logic and recently interval type II fuzzy logic to the conventional and adaptive control algorithms and comparing them with PI controller in mitigation the source current THD. PI controller is tuned to control the capacitor DC voltage for a specific range of the loads and sometimes fails to keep it at the reference value in the case of load variation. Besides the PI controller need a precise mathematical model which is hard to obtain in practical [17]. The utilization of PI controller based on a modified instantaneous reactive power theory based on generating compensating current references is presented in [18]. The new design of control algorithm for DSTATCOM device is produced to suite the distribution GTO thyristor-controlled series capacitor D-GCSC feeding R and RL loads consists of two loops of PID controller for generating d-axis and q-axis source current for the mitigation of source current harmonics [19]. The solution for that is the type I fuzzy logic controller, which doesn't need any complicated mathematical equation and can deal with imprecise inputs. The high number of the rules and inputs requires special hardware with specific parameters and high cost, which is hard to obtain [20, 21]. The new technique of type I fuzzy-logic-based source-voltage-current algorithm to control shunt active power filter and the comparison with PI controller is presented in [22]. The new membership functions of the error signal consist from seven membership functions with different size and shape for interval type I fuzzy logic-based DSTATCOM device improves the working of DSTATCOM in the mitigation of current harmonics below the 2% [23]. The application of interval type II fuzzy logic can deal with uncertain data by using the low and upper membership functions which leads improving the THD harmonics better than other artificial intelligence, minimizing the number of rules in comparison with type I fuzzy logic and as a result reducing the hardware specifications needed. The installation of Interval type II fuzzy logic tools in MATLAB Simulink, how to enter of the inputs, rule bases and outputs and the tuning process are presented in [24]. Interval type II fuzzy logic with new membership functions for the error signal based STATCOM device which is connected to high voltage bus bar to make the STATCOM able to compensate the reactive power and mitigate the current harmonic

for low voltage loads and high voltage loads at the same time is presented in [25]. The artificial neural network is superior to conventional controller because of fast convergence, less steady state, adaptation to different conditions and the variation of the loads [26]. The artificial neural network-based instantaneous reactive power theory for controlling the three-phase four-wire DSTATCOM and how to train the artificial neural network depending on the PI controller are presented in [27]. The neural network for controlling three phase four wire DSTATCOM is presented in [28]. A neuro fuzzy logic controller-based shunt active power filter is applied to overcome the tuning process of PI controller and to make the active power filter self-tunning with respect to variation of the load by applying a training algorithm is explained in [29]. The poor transient response of DC capacitor voltage and grid currents caused by using PI-based DSTATCOM device due to the variation of the load can be solved by using the new technique of online training algorithm wavelet Takagi-Sugeno-Kang fuzzy neural network (WTSKFNN) based DSTATCOM device [30].

A self-tuning control algorithm based conventional control algorithm along with automatic interface inductor integration DSTATCOM is used in this paper. The interface inductor bank with four groups is added to the DSTATCOM device to suit all load apparent power rates within the apparent power rate of the DSTATCOM device. The new construction of applying adaptive interval type II fuzzy logic controller along with a new loop to generate pulses to interface inductor bank gives the control algorithm the ability to tune itself with respect to load currents. The comparison of adaptive interval type II fuzzy logic with normal type II fuzzy logic is made using MATLAB environment®.

2 DSTATCOM three phase four wire device with interface inductor bank

DSTATCOM device is one of the devices that has been used recently to improve the power quality in the distribution system. It monitors the harmonics in the source current generated by the load and then generates the opposite signals to eliminate them, leading to decrease of the current total harmonic distortion. It monitors the reactive power needed by load and generates the compensating reactive power, leading to improve the source power factor and making it near to the unity value [14]. The difference between three-phase four-wire and three-phase three-wire DSTATCOM device is that it monitors the load neutral current, and in the cases of the fault, it generates an opposite compensating current which eliminates the load neutral current and leads to the zero neutral source current [12, 27]. DSTATCOM device three-phase four-wire consists of DC capacitor C_{DC}, interface inductor L_f, six IGBT thyristors for the three phases and two thyristors for the neutral [14].

In Table 1:

- m: is the modulation index and is considered as 1;
- V_{DC}: is the reference DC voltage (V_{DC} = 700 V);
- V_{DC1}: is the minimum voltage level of DC bus (V_{DC1} = 696.5 V);
- a: is the overloading factor (a = 1.2);
- V: is the phase voltage (V = 239.60 V);
- I: is the phase current;
- t: is the time by which the DC bus voltage to be recovered (t = 350 uS);
- $i_{cr(p-p)}$: current ripple ($i_{cr(p-p)} = 0.05 \times I$);
- f_s: switching frequency (f_s = 10 kHZ).

In this paper interface inductor bank is used instead of an interface inductor. It consists of a series inductor L_{f0} = 2 mH connected to one of the following branches in series: inductor breaker B, interface inductor bank first group L_{f1} = 39 mH for the coupling of DSTATCOM device when load between 0–3.5 kVA, interface inductor bank second group of L_{f2} = 19 mH for the coupling of DSTATCOM device when load between 3.5–7 kVA, interface inductor bank third group L_{f3} = 8 mH for the coupling of DSTATCOM device when load between 7–14 kVA and interface inductor bank forth group L_{f4} = 5 mH for the coupling of DSTATCOM device when load between 14–20 kVA. Each group has a breaker that opens and closes by the mean of pulses generated by the interface inductor bank pulse generator in the

Table 1 The DSTATCOM device parameter

	Formula	2 Kva (4.107 A)	4 Kva (8.01 A)	8 Kva (16.83 A)	12 Kva (24.05 A)
V_{DC}	$V_{DC} > \left[2 \times \sqrt{2} \times \frac{V_{LL}}{\sqrt{3}} \times m\right]$	700 V	700 V	700 V	700 V
C_{DC}	$\frac{1}{2} C_{DC}\left[\left(V_{DC}^2\right) - \left(V_{DC1}^2\right)\right] = 3V(aI)t$	507 uF	991 uF	2082 uF	2955 uF
IIB	$L_F = \frac{\sqrt{3} \times m \times V_{DC}}{12 \times a \times f_s \times i_{cr(p-p)}}$	L_{f1} (41 mH)	L_{f2} (21 mH)	L_{f3} (10 mH)	L_{f4} (7 mH)

controller system. The calculations of the capacitor, the interface inductor bank and the capacitor DC voltage are depicted in Table 1 [31] (see Fig. 1).

3 Control algorithms

3.1 Adaptive interval type II fuzzy logic-based instantaneous reactive power theory control algorithm with interface inductor bank pulse generator

This control algorithm generates six pulses for the six thyristors of the three legs of DSTATCOM, two pulses for the two thyristors of the fourth leg DSTATCOM and five pulses for the five breakers of the interface inductor bank groups (see Figs. 2 and 3).

3.1.1 Instantaneous reactive power theory

The main idea of the instantaneous reactive power theory is to provide the three-phase PWM with three error signals to generate the six pulses mentioned by comparing the source current reference signals with the sensed current signals. The desired source current reference should contain the component of the load active power after filtering from the harmonics by using a low pass filter, zero reactive power component to make the power factor of the source at the unity value and the active power adjusting component Padj generated by the new adaptive interval type II fuzzy logic controller. It also provides the neutral PWM with the error signal to generate two pulses mentioned by comparing the desired source neutral current, which is the zero value, with the sensed source neutral current. abc-$\alpha\beta$ and $\alpha\beta$-abc transformations are used in this theory [32].

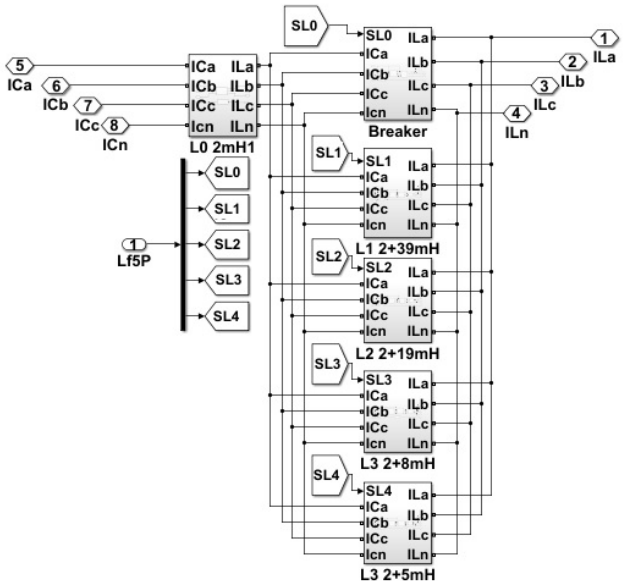

Fig. 1 The interface inductor bank

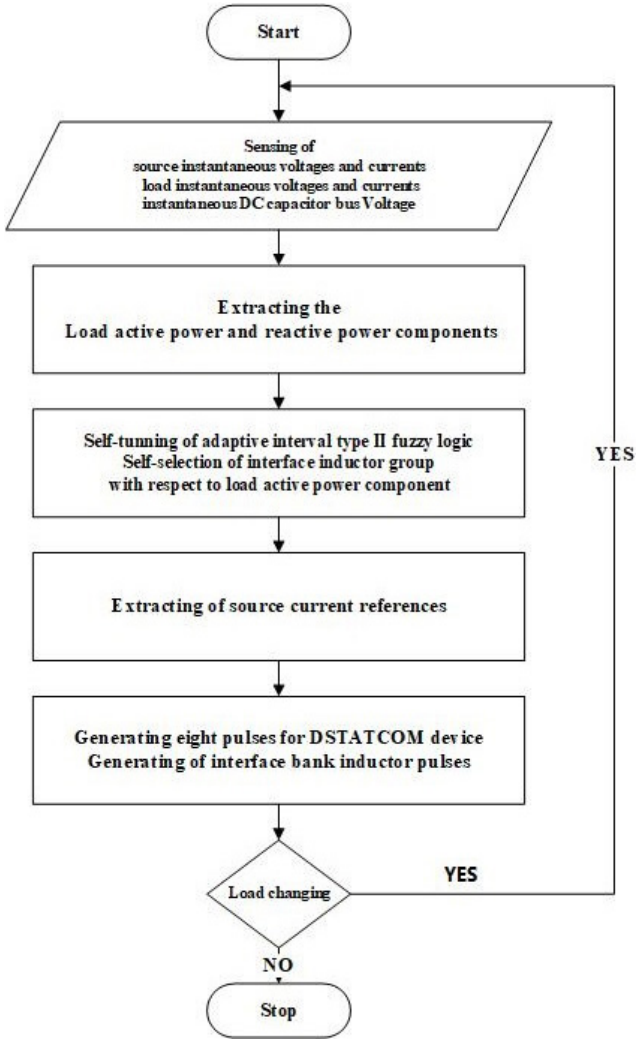

Fig. 2 Flow chart of implementation of adaptive interval type II fuzzy logic-based instantaneous reactive power theory controller in MATLAB

$$\begin{bmatrix} V_\alpha \\ V_\beta \\ V_0 \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 1 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix} \begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} \tag{1}$$

$$\begin{bmatrix} I_\alpha \\ I_\beta \\ I_0 \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 1 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix} \begin{bmatrix} I_{La} \\ I_{Lb} \\ I_{Lc} \end{bmatrix} \tag{2}$$

The load instantaneous active power P_L and the instantaneous reactive power q_L can be calculated by using Eqs. (3)–(5):

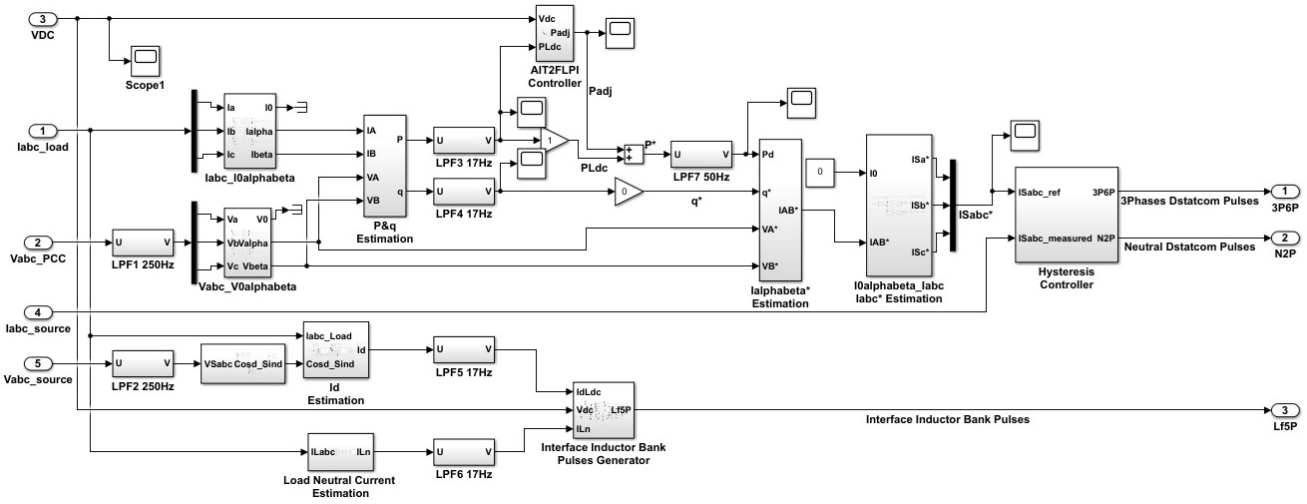

Fig. 3 Adaptive interval type II fuzzy logic-based instantaneous reactive power algorithm controller

$$\begin{bmatrix} P_L \\ q_L \end{bmatrix} = \begin{bmatrix} V_\alpha & V_\beta \\ -V_\beta & V_\infty \end{bmatrix} \begin{bmatrix} I_\alpha \\ I_\beta \end{bmatrix}, \tag{3}$$

$$P_L = V_\alpha \times I_\alpha + V_\beta \times I_\beta, \tag{4}$$

$$q_L = -V_\beta \times I_\alpha + V_\alpha \times I_\beta. \tag{5}$$

The active power signal has two components: the alternating active power component $P^{\sim}$ and the filtered component P_{LF}. The reactive power signal has two components: the alternating reactive power component $q^{\sim}$ and the filtered reactive power component q_{LF} as Eqs. (6) and (7):

$$P_L = P^{\sim} + P_{LF}, \tag{6}$$

$$q_L = q^{\sim} + q_{LF}. \tag{7}$$

The desired source active power reference P_S^* and source reactive power reference q_S^* as Eqs. (8) and (9):

$$P_S^* = P_{Lf} + P_{adj}, \tag{8}$$

$$q_S^* = 0. \tag{9}$$

The desired reference source current signals in $\alpha\beta$ form $I_{S\alpha}^*$, $I_{S\beta}^*$ can be calculated as Eqs. (10)–(13):

$$\begin{bmatrix} I_{S\alpha}^* \\ I_{S\beta}^* \end{bmatrix} = \frac{1}{V_\alpha^2 + V_\beta^2} \begin{bmatrix} V_\alpha & -V_\beta \\ V_\beta & V_\alpha \end{bmatrix} \begin{bmatrix} P_{LF} + P_{adj} \\ 0 \end{bmatrix}, \tag{10}$$

$$I_{S\alpha}^* = \frac{1}{V_\alpha^2 + V_\beta^2} \times \left(V_\alpha \times \left(P_{LF} + P_{adj} \right) \right), \tag{11}$$

$$I_{S\beta}^* = \frac{1}{V_\alpha^2 + V_\beta^2} \times \left(V_\beta \times \left(P_{LF} + P_{adj} \right) \right). \tag{12}$$

The desired reference source current signals in ABC form I_{Sa}^*, I_{Sb}^*, I_{Sc}^* can be calculated as the following equations:

$$\begin{bmatrix} I_{Sa}^* \\ I_{Sb}^* \\ I_{Sc}^* \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & 1 & \frac{1}{\sqrt{2}} \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} & \frac{1}{\sqrt{2}} \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} & \frac{1}{\sqrt{2}} \end{bmatrix} \begin{bmatrix} I_{S\alpha}^* \\ I_{S\beta}^* \\ I_0 \end{bmatrix}. \tag{13}$$

The desired error signals which will be used as input signals for the pulse width modulation can be calculated by comparing the desired reference source current signals I_{Sa}^*, I_{Sb}^*, I_{Sc}^* with the sensed source current signals I_{Sa_m}, I_{Sb_m}, I_{Sc_m} as Eqs. (14)–(16):

$$Erra = I_{Sa}^* - I_{Sa_m}, \tag{14}$$

$$Errb = I_{Sb}^* - I_{Sb_m}, \tag{15}$$

$$Errc = I_{Sc}^* - I_{Sc_m}. \tag{16}$$

3.1.2 Adaptive interval type II fuzzy logic controller-based IRP

The advantage of this controller is that there is no need for tuning process due to the changing of the loads. This controller can tune itself according to the filtered load active power P_{LF}. It consists of the interval type II fuzzy logic controller connected to the adaptive proportional integral controller. It has two inputs capacitor DC voltage V_{DC} and filtered load active power P_{LF} and it has one output active power adjusting signal P_{adj} which increases or decreases the filtered load active power component to make the electrical source generate active power needed by the load along with the power

loses in the DSTATCOM device to keep the capacitor DC voltage at the reference value of 700 V (see Fig. 4).

The interval type II fuzzy logic consists of the fuzzifier, fuzzy inference engine with rule base, type reducer and the de-fuzzifier. The fuzzifier transfers the crisp input into type II fuzzy sets by using the interval membership function which has lower and upper regions, the inference fuzzy engine along with rule bases generates the output type II fuzzy set, type reducer reduces the output type II fuzzy sets to type I fuzzy sets, de-fuzzifier transform the output type I fuzzy set into the crisp value [8, 24].

The interval type II fuzzy logic used in this paper has two inputs and one output. The first input is error 'E' with a range of [−2, 2] with upper triangular membership function and lower Gaussian membership function. The second input is change of the error 'CE' with a range of [−1, 1] with upper triangular membership function and lower Gaussian membership function. The membership functions are L (low), N (normal) and H (high). The role base used in this paper is nine rules and depicted in Table 2. The output is active power adjusting percentage signal '$P_{adj\%}$', which is used as the input for the adaptive proportional-integral controller. The use of IT2FL decreases the number of rules used and computational time, leading to the increase of capacitor DC voltage response to the control system in comparison with IT1FL [8, 24] (see Fig. 5).

Table 2 The rule base used in the AIT2FL-based IRP

Change of Error	Error		
	L	N	H
L	L	L	N
N	L	N	H
H	N	H	H

The error signal E and change of the error CE can be calculated from Eqs. (17) and (18):

$$E_{(n)} = V_{\mathrm{DC}}^{*} - V_{\mathrm{DC}(n)}, \tag{17}$$

$$CE_{(n)} = E_{(n)} - E_{(n-1)}. \tag{18}$$

When the change of error is normal, there are three situations, the error is low (L), normal (N) and high (H). When the error is low $V_{\mathrm{DC}(n)} > V_{\mathrm{DC}}^{*}$ which means that the value of DC capacitor voltage is greater than the reference value; in this case, the output of controller $P_{adj\%}$ will be Low which means that the controller will generate $P_{adj\%}$ below the stable value to decrease the active power generated by the electrical source lower than the stable value to make the capacitor discharge, leading the DC capacitor voltage to decrease and reach the reference value. When the error is normal $V_{\mathrm{DC}(n)} > V_{\mathrm{DC}}^{*}$ which means that the DC capcitor voltage at the reference value. In this case, the output of the controller $P_{adj\%}$ will be normal which means

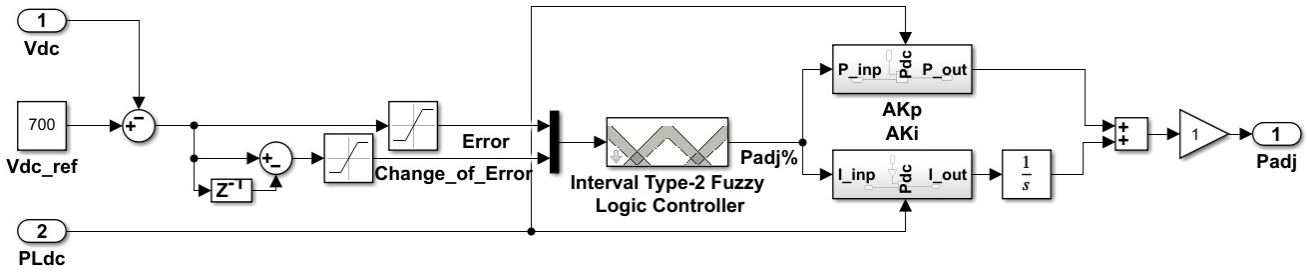

Fig. 4 Adaptive interval type II fuzzy logic controller

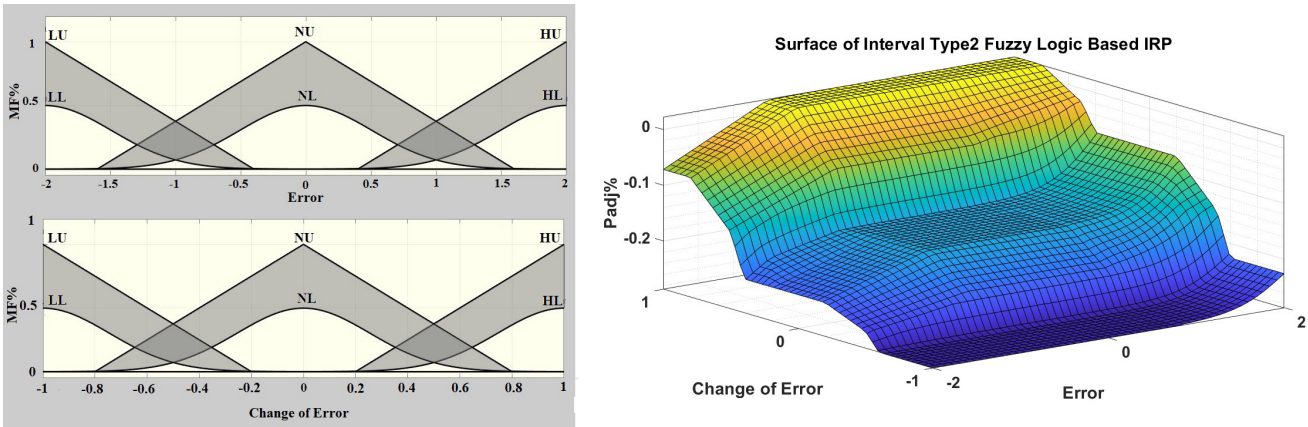

Fig. 5 MF of first input 'Error', MF of second input 'Change of Error', surface view AIT2FL-based IRP

that the controller will generate $P_{adj\%}$ at the stable value to keep the active power generated by the electrical source at the stable value to keep the DC capacitor voltage at the reference value. When the error is high $V_{\mathrm{DC}(n)} > V_{\mathrm{DC}}^{*}$ which means that the DC capacitor voltage is lower than the reference value; In this case, the output of the controller $P_{adj\%}$ will be high which means that the controller will generate $P_{adj\%}$ above the stable value to increase the active power generated by the electrical source higher than the stable value to make the capacitor charge, leading the DC capacitor voltage to increase and reach the reference value.

When the error is normal (the DC capacitor voltage at the reference value), there three situations, the change of error is low (L), normal (N) and high (H). When the change of load is low $E_{(n-1)} > E_{(n)}$; $V_{\mathrm{DC}(n-1)} < V_{\mathrm{DC}(n)}$ which means that the DC capacitor voltage is increasing. In this case, the output of the controller $P_{adj\%}$ will be low which means that the controller will generate $P_{adj\%}$ below the stable value to decrease the active power generated by the electrical source trying to keep the DC capacitor at the reference value. When the change of error is normal $E_{(n-1)} = E_{(n)}$; $V_{\mathrm{DC}(n-1)} = V_{\mathrm{DC}(n)}$ which means that the DC capcitor voltage is stable. In this case, the output of the controller $P_{adj\%}$ will be normal which means that the controller will generate $P_{adj\%}$ at the stable value to keep the active power generated by the electrical source at the stable value to keep the DC capacitor voltage at the reference value. When the change of load is high $E_{(n-1)} \left\langle E_{(n)};\ V_{\mathrm{DC}(n-1)} \right\rangle V_{\mathrm{DC}(n)}$ which means that the DC capacitor voltage is decreasing. In this case, the output of the controller $P_{adj\%}$ will be high which means that the controller will generate $P_{adj\%}$ above the stable value to increase the active power generated by the electrical source trying to keep the DC capacitor at the reference value.

When the error is low and change of error is low which means that DC capacitor voltage is higher than the reference value and increasing; in this case, the output of the controller $P_{adj\%}$ will be low which means that the controller will generate $P_{adj\%}$ below the stable value to decrease the active power generated by the electrical source lower than the stable value to make the capacitor discharge leading the DC capacitor voltage to decrease and reach the reference value. When the error is low and change of error is high which means that DC capacitor voltage is greater than the reference value and decreasing; in this case, the output of the controller $P_{adj\%}$ will be normal which means that the controller will generate $P_{adj\%}$ in the stable value because the DC capacitor voltage is decreasing by itself, and it is heading to the reference value.

When the error is high and change of error is low which means that DC capacitor voltage is lower than the reference value and increasing; in this case, the output of the controller $P_{adj\%}$ will be normal which means that the controller will generate $P_{adj\%}$ in stable value because the DC capacitor voltage is increasing by itself, and it is heading to the reference value. When the error is high and change of error is high which means that DC capacitor voltage is lower than the reference value and decreasing; in this case, the output of the controller $P_{adj\%}$ will be high which means that the controller will generate $P_{adj\%}$ above the stable value to increase the active power generated by the electrical source higher than the stable value to make the capacitor charge leading the DC capacitor voltage to increase and reach the reference value.

The adaptive proportional integral controller has an adaptive K_p and adaptive K_i. The new structure of this adaptive controller changes the value of K_p and K_i with respect to filtered load active power, which means it tunes itself with respect to the load changing.

The adaptive proportional integral controller in this paper has two inputs and one output. The first input is the active power adjusting percentage signal $P_{adj\%}$ and the second input is the filtered load active power P_{LF}. The output is the active power adjusting signal 'P_{adj}', which will be used to keep the DC capacitor voltage at the reference value as mentioned before:

$$P_{adj(n)} = P_{adj(n-1)} + AK_{p(n)}\left(P_{adj\%(n)} - P_{adj\%(n-1)}\right) + Ak_{I(n)}P_{adj\%(n)}, \tag{19}$$

$$AK_{p(n)} = P_{LF(n)};\ \ Ak_{I(n)} = 2 \times P_{LF(n)}, \tag{20}$$

where:

- $P_{adj(n)}$: the active power adjusting signal, which is the output of the adaptive PI controller at the nth sampling instant;
- $P_{adj\%(n)}$: the active power adjusting percentage signal, which is the output of the IT2FL controller and input of Adaptive PI controller at the nth sampling instant;
- $AK_{p(n)}$: adaptive proportional constant at the nth sampling instant;
- $Ak_{I(n)}$: adaptive integral constant at the nth sampling instant;
- $P_{LF(n)}$: filtered load active power at the n^{th} sampling instant.

3.2 Adaptive interval type II fuzzy logic-based synchronous reference frame theory control algorithm with interface inductor bank pulse generator

This control algorithm generates six pulses for the six thyristors of the three legs of DSTATCOM, two pulses for the two thyristors of the fourth leg of DSTATCOM and five pulses for the five breakers of the interface inductor bank groups (see Figs. 6 and 7).

3.2.1 Synchronous reference frame theory

The main idea of the synchronous reference frame is to provide the three-phase PWM with three error signals to generate the six pulses mentioned by comparing the source current reference signals with the sensed current signals.

The desired source current reference should contain the direct load current component after filtering from the harmonics I_{dLF} by using a low pass filter, zero quadrature load current component I_{qL} to make the power factor of the source at the unity value and the direct current adjusting component I_{dadj} generated by the new adaptive interval type II fuzzy logic controller. It also provides the neutral PWM with the error signal to generate two pulses mentioned by comparing the desired reference source neutral current, which is the zero value, with the sensed source neutral current. abc-0$\alpha\beta$, 0$\alpha\beta$-0dq, 0dq-0$\alpha\beta$ and 0$\alpha\beta$-abc transformations are used in this theory [12, 33].

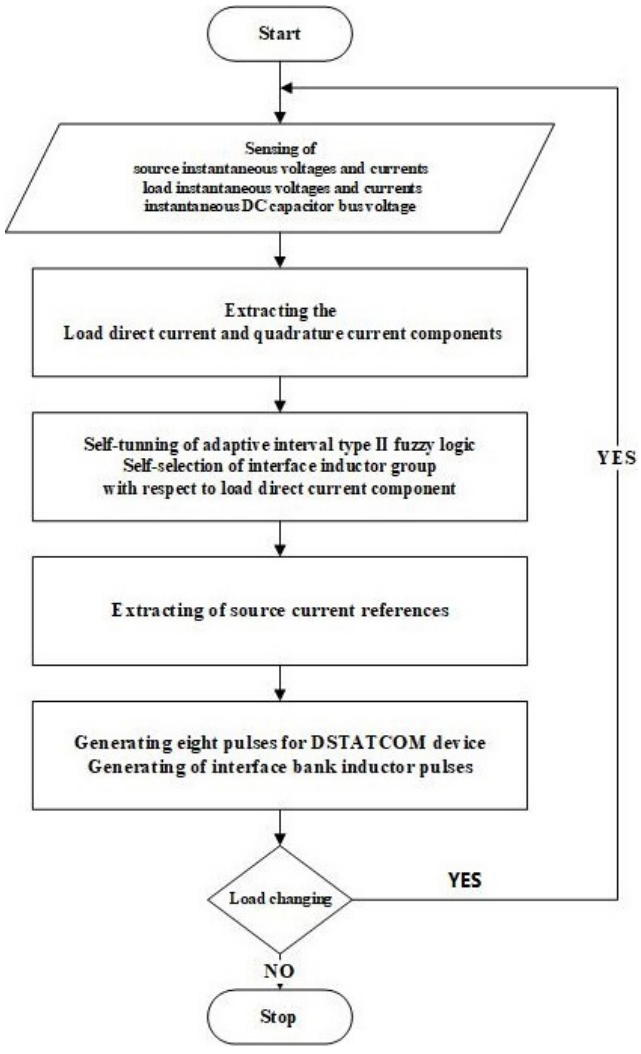

Fig. 6 Flow chart of implementation of adaptive interval type II fuzzy logic-based synchronous reference frame theory controller in MATLAB

$$\begin{bmatrix} V_\alpha \\ V_\beta \\ V_0 \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 1 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix} \begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} \tag{21}$$

$$\begin{bmatrix} I_\alpha \\ I_\beta \\ I_0 \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 1 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix} \begin{bmatrix} I_{La} \\ I_{Lb} \\ I_{Lc} \end{bmatrix} \tag{22}$$

The source voltage signals are used with the phase locked loop PLL to extract the angel θ as Eqs. (23) and (24):

$$\cos\theta = \frac{V_\alpha}{\sqrt{V_\alpha^2 + V_\beta^2}}, \tag{23}$$

$$\sin\theta = \frac{V_\beta}{\sqrt{V_\alpha^2 + V_\beta^2}}. \tag{24}$$

The direct load current component I_d and the quadrature load current component I_q can be calculated by Eqs. (25)–(27):

$$\begin{bmatrix} I_0 \\ I_d \\ I_q \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 \\ 0 & \cos\theta & \sin\theta \\ 0 & -\sin\theta & \cos\theta \end{bmatrix} \begin{bmatrix} I_0 \\ I_\alpha \\ I_\beta \end{bmatrix}, \tag{25}$$

$$I_d = \cos\theta \times I_\alpha + \sin\theta \times I_\beta, \tag{26}$$

$$I_q = -\sin\theta \times I_\alpha + \cos\theta \times I_\beta. \tag{27}$$

The direct load current component I_d has two components: the AC direct load current component $\tilde{I_d}$ and the filtered direct load current component I_{dLF}. The quadrature load current component has two components: I_q the AC quadrature load current component $\tilde{I_q}$ and the DC quadrature load current component I_{qLF} as Eqs. (28) and (29):

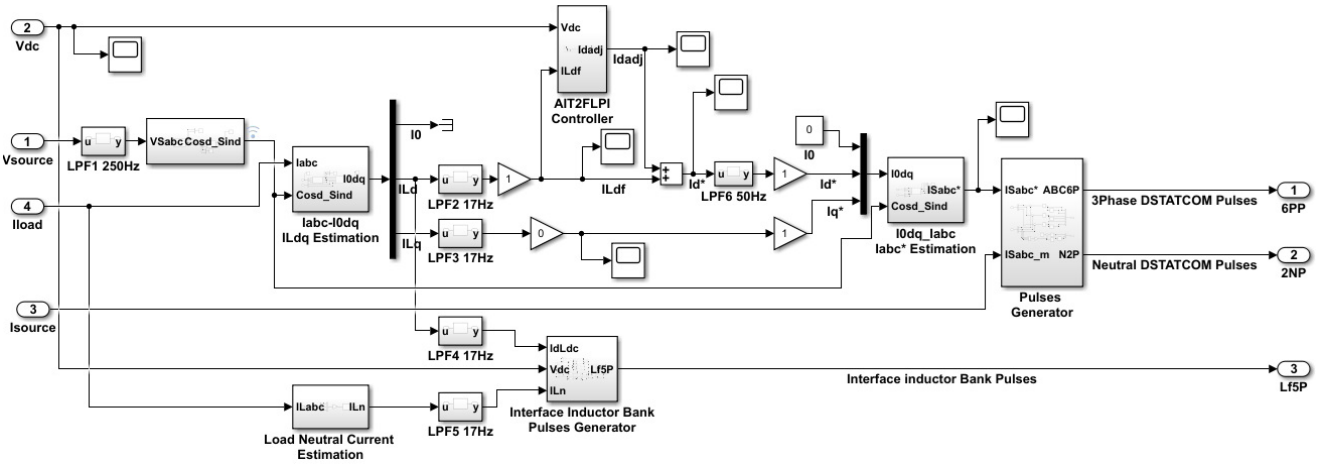

Fig. 7 Adaptive interval type II fuzzy logic-based synchronous reference frame theory control algorithm

$$I_d = I_d^{\sim} + I_{dLF}, \tag{28}$$

$$I_q = I_q^{\sim} + I_{qLF}. \tag{29}$$

The reference source current direct and quadrature components of the desired reference source current I_{Sd}^*, I_{Sq}^* are mentioned in Eqs. (30) and (31):

$$I_{Sd}^* = I_{dLF} + I_{dadj}, \tag{30}$$

$$I_{Sq}^* = 0. \tag{31}$$

The desired reference source current signals in $\alpha\beta$ form $I_{S\alpha}^*$, $I_{S\beta}^*$ can be calculated as Eqs. (32)–(34):

$$\begin{bmatrix} I_{S0}^* \\ I_{S\alpha}^* \\ I_{S\beta}^* \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 \\ 0 & \cos\theta & -\sin\theta \\ 0 & \sin\theta & \cos\theta \end{bmatrix} \begin{bmatrix} 0 \\ I_{dLF} + I_{dadj} \\ 0 \end{bmatrix}, \tag{32}$$

$$I_{S\alpha}^* = \cos\theta \times \left(I_{dLF} + I_{dadj}\right), \tag{33}$$

$$I_{S\beta}^* = \sin\theta \times \left(I_{dLF} + I_{dadj}\right). \tag{34}$$

The desired reference source current signals in ABC form I_{Sa}^*, I_{Sb}^*, I_{Sc}^* can be calculated as Eq. (35):

$$\begin{bmatrix} I_{Sa}^* \\ I_{Sb}^* \\ I_{Sc}^* \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & 0 & 0 \\ 0 & -\frac{1}{2} & \frac{\sqrt{3}}{2} \\ 0 & -\frac{1}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} I_{S0}^* \\ I_{S\alpha}^* \\ I_{S\beta}^* \end{bmatrix}. \tag{35}$$

The desired error signals which will be used as input signals for the pulse width modulation can be calculated by comparing the desired reference source current signals I_{Sa}^*, I_{Sb}^*, I_{Sc}^* with the sensed source current signals I_{Sa_m}, I_{Sb_m}, I_{Sc_m} as Eqs. (36)–(38):

$$Erra = I_{Sa}^* - I_{Sa_m}, \tag{36}$$

$$Errb = I_{Sb}^* - I_{Sb_m}, \tag{37}$$

$$Errc = I_{Sc}^* - I_{Sc_m}. \tag{38}$$

3.2.2 Adaptive interval type II fuzzy logic controller-based SRF

The interval type II fuzzy logic-based SRF used in this paper has two inputs and one output. The first input is error 'E' with a range of [−2, 2] with upper triangular membership functions and lower Gaussian membership functions. The second input is the change of the error 'CE' with range of [−1,1] with upper triangular membership functions and lower Gaussian membership functions. The membership functions are L (low), N (normal) and H (high). The rule base used is nine rules and depicted in Table 3. The output is direct current adjusting percentage signal '$I_{dadj\%}$', which is used as the input for the adaptive proportional-integral controller.

The adaptive proportional integral controller has an adaptive K_p and adaptive K_i. The new structure of this adaptive controller changes the value of K_p and K_i with respect to filtered direct load current component 'I_{LdF}', which means it tunes itself with respect to the load changing. The adaptive proportional-integral controller in this controller has two inputs and one output. The first input is the direct current adjusting percentage signal $I_{dadj\%}$ and the second input is the filtered direct load current component

Table 3 The rule base used in the AIT2FL-based SRF

Change of Error	Error		
	L	N	H
L	L	L	N
N	L	N	H
H	N	H	H

I_{LdF}. The output is the direct current adjusting signal 'I_{dadj}' (Eqs. (39) and (40)), which will be used to keep the DC capacitor voltage at the reference value as mentioned before (see Figs. 8 and 9):

$$I_{dadj(n)} = I_{dadj(n-1)} + AK_{p(n)}\left(I_{dadj\%(n)} - I_{dadj\%(n-1)}\right) + Ak_{I(n)}I_{dadj\%(n)}, \quad (39)$$

$$AK_{p(n)} = I_{LdF(n)};\ \ Ak_{I(n)} = 2 \times I_{LdF(n)}, \quad (40)$$

where:

- $I_{dadj(n)}$: the direct current adjusting signal, which is the output of the adaptive PI controller at the nth sampling instant;
- $I_{dadj\%(n)}$: the direct current adjusting percentage signal, which is the output of the IT2FL-based SRF controller and input of adaptive PI controller at the n^{th} sampling instant;
- $AK_{p(n)}$: adaptive proportional constant at the nth sampling instant;
- $Ak_{I(n)}$: adaptive integral constant at the n^{th} sampling instant;
- $I_{LdF(n)}$: filtered direct load current component at the nth sampling instant.

3.3 Interface inductor bank pulse generator

The interface inductor bank pulse generator is used to support the adaptive interval type II fuzzy logic proportional-integral-based IRP and SRF controller in making the DSTATCOM device a plug-and-play device without the needing of a tuning process. It has three inputs the direct load current component 'I_{dL}', capacitor DC voltage V_{DC} and the load neutral current I_{Ln}. It generates five pulses as an output to the breakers of the interface inductor bank groups and defines which group will work under a specific load. The working principle of this new pulse generator is as follows (see Fig. 10):

- when there is a changing of the capacitor DC voltage V_{DC} (switching on of DSTATCOM device), it generates pulses to switch on the breaker and switch off all the other interface inductor groups in the interface inductor bank to increase rising time, peak time and settling time of the control system;
- when there is a changing of the direct load current component I_{dL} (changing of the connected load), it generates the pulses to switch on the breaker and switch off all the other interface inductor groups. The changing of direct load current component differentiates when there is unbalance or fault in the load. The load neutral current is used as a signal to check if there is unbalance or fault in the load;
- when the capacitor DC voltage and direct load current component is constant, it generates pulses to switch on only the first interface inductor group L_{f1} when the direct load current component between 0–5 A, to switch on only the second interface inductor group L_{f2} when

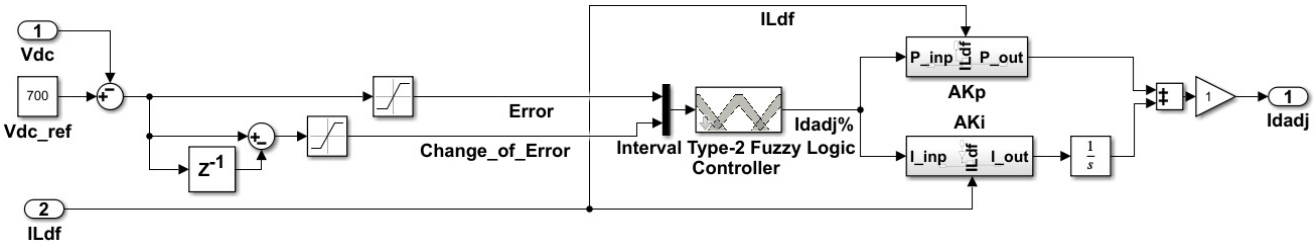

Fig. 8 Adaptive interval type II fuzzy logic-based SRF

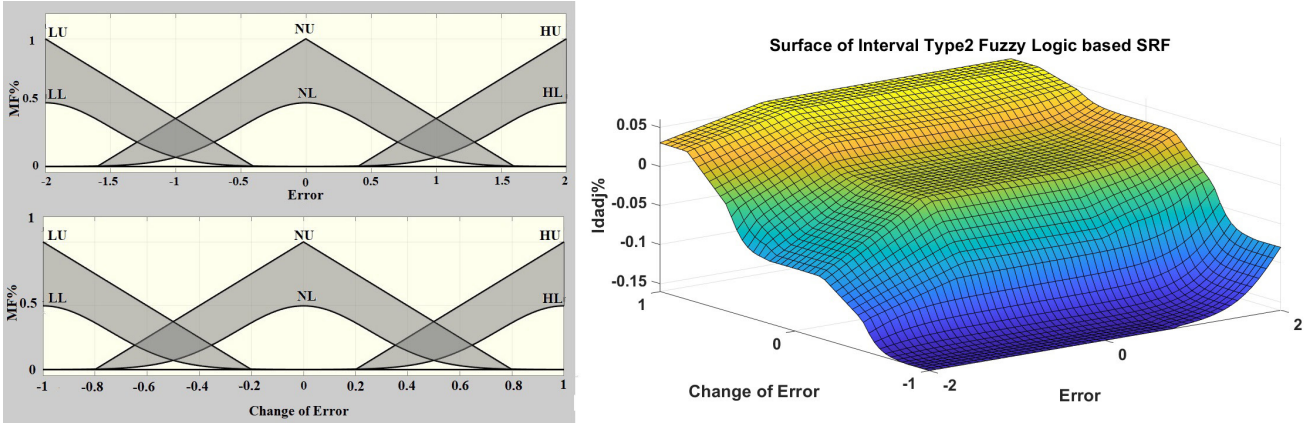

Fig. 9 MF of first input 'Error'; MF of second input 'Change of Error'; surface view for AIT2FL-based SRF

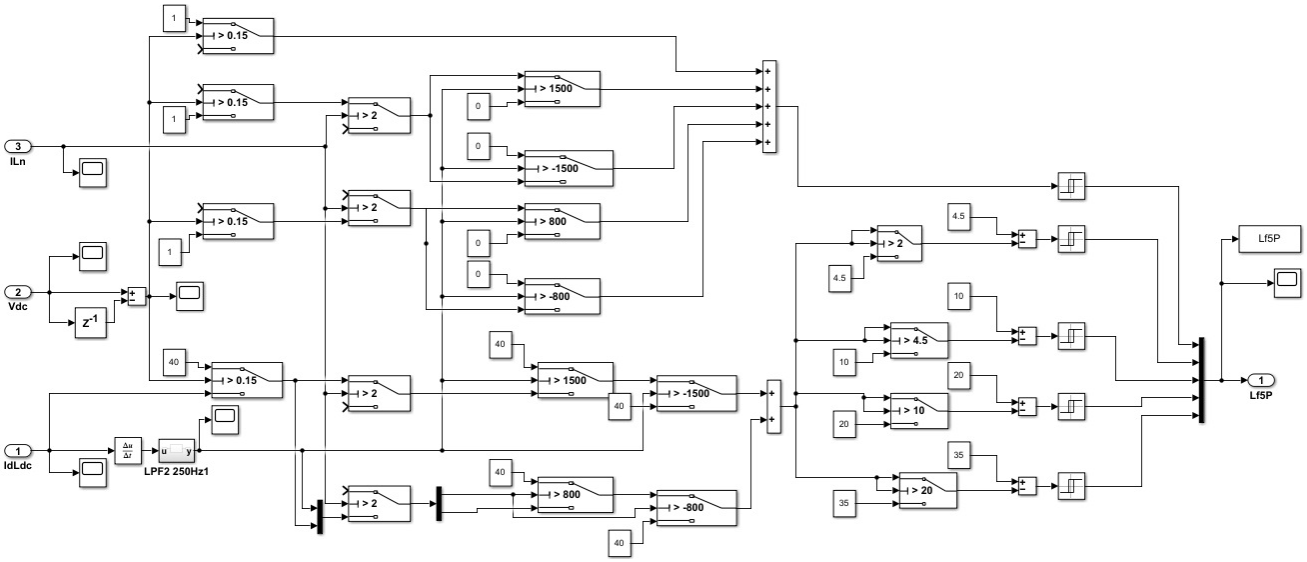

Fig. 10 Interface inductor bank pulse generator

the direct load current component 5–10 A, to switch on only the third interface inductor group L_{f3} when the direct load current component 10–20 A and to switch on only the fourth interface inductor group L_{f4} when the direct load current component above 20 A.

4 Simulation and results

The simulation was done by using MATLAB R2021a environment with simulation type of 'discrete' and sample time of '1 × 10^{-5}'. The interval type II fuzzy logic controller toolbox used in the simulation and information on how to install and use it is mentioned in [12].

The electrical grid used in this Simulink is depicted in Fig. 11. It consists of the electrical source with a phase-to-phase voltage of 415 V, a transmission line with an impendence of $r = 0.01$ Ω, $L = 2$ mH, three-phase four-wire DSTATCOM device at an apparent power rate of 12 kVA with different control algorithms for power quality improvement, interface inductor bank and different load interface inductor bank and different load situations. The control algorithms used in this paper were interval type II fuzzy logic controller-based instantaneous reactive power theory, adaptive interval type II fuzzy logic controller-based instantaneous reactive power theory with interface inductor pulse

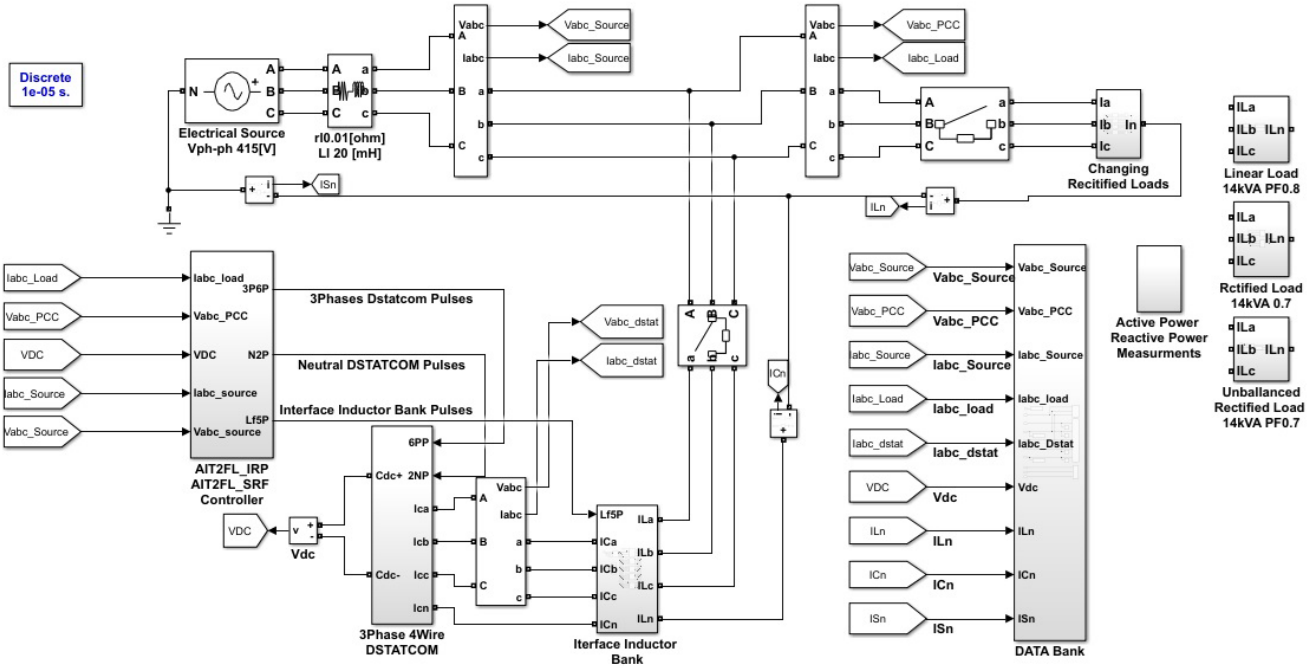

Fig. 11 The studied electrical grid, it contains electrical source, DSTATCOM device at apparent load rating of 12 kVA, AIT2FL_IRP/AIT2FL_SRF controller and different load situations

generator, interval type II fuzzy logic controller-based synchronous reference frame theory and adaptive interval type II fuzzy logic controller-based synchronous reference frame theory with interface inductor pulse generator. These different control algorithms were tested with different load situations constant linear load 13 kVA 0.8 PF, constant nonlinear rectified load 4 kVA 0.7 PF, constant nonlinear rectified load 14 kVA 0.7 PF, load changing between four nonlinear rectified loads (2 kVA 0.7 PF, 8 kVA 0.7 PF, 4 kVA 0.7 PF and 12 kVA 0.7 PF) and unbalanced nonlinear rectified load 14 kVA 0.7 PF to figure out the efficiency of applying AIT2FL controller-based conventional control algorithms in comparison with normal IT2FL controller along with the conventional control algorithms. The AIT2FL-based conventional control algorithm was tested when apparent load power was near to the maximum apparent power rate of the DSTACOM device (see Fig. 11).

4.1 Constant loads

The parameters used in this paper to compare the different control algorithms are: first, electrical source parameters, which include source current total harmonic distortion (THD) and source power factor (PF); second, capacitor DC voltage signal response to the control system parameters, which include rising time (RT), peak time (PT), settling time (ST) and overshoot percentage (OS%) (see Tables 4 and 5).

First, constant linear load = 13 kVA 0.8 PF. The use of IT2FL-based SRF DSTATCOM device with interface inductor L_f = 7 mH makes the source parameters and capacitor DC voltage response as source current THD = 1.18%, 0.98 source PF, RT = 37.5 mS, PT = 73 mS and ST = 80 mS. The use of AIT2FL with IIBPG-based SRF DSTATCOM device with interface inductor bank makes the source parameters and capacitor DC voltage response as source current THD = 1.19%, 0.98 source PF, RT = 7.3 mS, PT = 13 mS and ST = 50 mS with no overshoot (see Fig. 12).

The application of the AIT2FL with IIBPG-based on the conventional control algorithm IRP and SRF improves capacitor DC voltage response in a good margin and the source current THD and source PF in the small margin in comparison with the normal IT2FL-based conventional controller at linear load 13 kVA 0.8 PF (greater than the apparent power rate of DSTATCOM device 12 kVA).

Second, constant rectified nonlinear load 4 kVA 0.7 PF. The use of IT2FL-based SRF DSTATCOM device with interface inductor L_f = 21 mH, with respect to the load 4 kVA, makes the source parameters and capacitor DC voltage response as source current THD 4.51%, 0.98 source PF, RT = 63.1 mS, PT = 104 mS and ST = 118 mS. The use of IT2FL-based SRF DSTATCOM device with interface inductor L_f = 7 mH, trial to improve capacitor DC voltage response, makes the source parameters and capacitor DC voltage response as source current THD = 8.34%, 0.98 source PF, RT = 38.5 mS, PT = 76 mS and ST = 90 mS. The use of interface inductor L_f = 7 mH instead of L_f = 21 mH improves the capacitor DC voltage response, but it worsens the source current THD. While using of inference inductor L_f = 21 mH as the calculation mentioned in Table 1, the source current THD was accepted by the IEEE standards, whereas the capacitor DC

Table 4 Capacitor DC voltage signal response comparison at different constant load situations

Constant load (kVA)	Controller	L_f (mH)	Capacitor DC voltage parameter				
			RT (ms)	PT (ms)	ST (ms)	OS (%)	P (V)
Linear load	AIT2FL_IRP	A–L_f	7.3	13	60	0%	700
Apparent power	IT2FL_IRP	L_f = 7	59	126	135	0.1%	700.7
13 kVA	AIT2FL_SRF	A–L_f	7.3	13	50	0%	700
0.8 PF	IT2FL_SRF	L_f = 7	37.5	73	80	0.5%	703.5
Nonlinear load	AIT2FL_IRP	A–L_f	7.1	13	40	0.581%	704.7
Apparent power	IT2FL_IRP	L_f = 21	85.3	182	190	0%	700
		L_f = 7	73.2	162	170	0%	700
4 kVA	AIT2FL_SRF	A–L_f	7.1	13	40	0.178%	701.25
0.7 PF	IT2FL_SRF	L_f = 21	63.13	104	118.5	0.457%	703.2
		L_f = 7	38.5	76	90	0.4%	702.8
Nonlinear load	AIT2FL_IRP	A–L_f	7.3	13	50	0%	700
Apparent power	IT2FL_IRP	L_f = 7	30.5	88	98	0.25%	701.8
12 kVA	AIT2FL_SRF	A–L_f	7.4	13	40	0%	700
0.7 PF	IT2FL_SRF	L_f = 7	26.1	59	70	0.62%	704.4

Table 5 Source current THD and Source PF comparison at different constant load situations

Constant load kVA	Controller	L_f (mH)	Electrical source parameter			
			I_s–THD	P_s (W)	Q_s (VAR)	Source PF
Linear load	W-DSTATCOM	–	0.08%	10950	8200	0.8
	AIT2FL_IRP	A–L_f	1.22%	10980	2170	0.98
Apparent power	IT2FL_IRP	L_f = 7	1.20%	10970	2170	0.98
13 kVA	AIT2FL_SRF	A–L_f	1.19%	10980	2160	0.98
0.8 PF	IT2FL_SRF	L_f = 7	1.18%	10970	2150	0.98
Nonlinear load	W-DSTATCOM	–	11%	2840	2805	0.7
	AIT2FL_IRP	A–L_f	4.27%	2860	530	0.983
Apparent power	IT2FL_IRP	L_f = 21	5.79%	2860	475	0.986
		L_f = 7	8.41%	2850	540	0.98
4 kVA	AIT2FL_SRF	A–L_f	4.21%	2860	530	0.983
0.7 PF	IT2FL_SRF	L_f = 21	4.51%	2860	530	0.983
		L_f = 7	8.34%	2880	520	0.98
Nonlinear load	W-DSTATCOM	–	10.93%	9840	9700	0.7
	AIT2FL_IRP	A–L_f	3.63%	9880	1870	0.982
Apparent power	IT2FL_IRP	L_f = 7	3.19%	9850	1870	0.982
12 kVA	AIT2FL_SRF	A–L_f	3.19%	9850	1860	0.982
0.7 PF	IT2FL_SRF	L_f = 7	4.37%	9860	1860	0.982

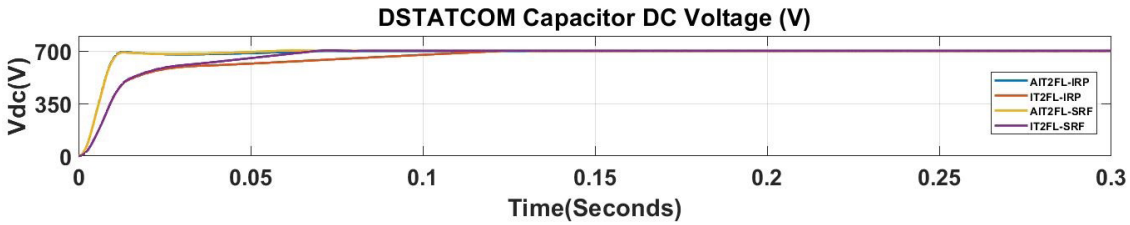

Fig. 12 Capacitor DC voltage signal response comparison at linear 13 kVA 0.8 PF

voltage response was somehow slow. In contrast, the use of inference inductor L_f = 7 mH, the source current THD was not accepted by IEEE standard, whereas the capacitor DC voltage response was somehow faster in comparison with the use of L_f = 21 mH.

The use of AIT2FL with IIBPG-based SRF DSTATCOM device with interface inductor bank makes the source parameters and capacitor DC voltage response as source current THD = 4.21%, 0.98 source PF, RT = 7.1 ms, PT = 13 ms and ST = 40 ms with minimal overshoot (see Fig. 13).

The application of the AIT2FL with IIBPG-based the conventional control algorithm IRP and SRF improves capacitor DC voltage response and the source current THD and source PF in a good margin in comparison with the normal IT2FL-based conventional controller at constant rectified nonlinear load 4 kVA 0.7 PF.

Third, constant rectified nonlinear load 14 kVA 0.7 PF. The use of IT2FL-based SRF DSTATCOM device with interface inductor L_f = 7 mH, with respect to the load 14 kVA, makes the source parameters and capacitor DC voltage response as source current THD 4.37%, 0.98 source PF, RT = 26.1 ms, PT = 59 ms and ST = 70 ms. The use of AIT2FL with IIBPG-based SRF DSTATCOM device with interface inductor bank makes the source parameters and capacitor DC voltage response as source current THD = 3.19%, 0.98 source PF, RT = 7.4 ms, PT = 13 ms and ST = 40 ms with no overshoot (see Fig. 14).

The application of the AIT2FL with IIBPG-based on the conventional control algorithm IRP and SRF improves capacitor DC voltage response and the source current THD and source PF in a good margin in comparison with the normal IT2FL-based conventional controller at a constant rectified nonlinear load 14 kVA 0.7 PF.

Before switching on the DSTATCOM device, the source current was deformed with THD of 10.93%, and the electrical source supplied the load with reactive power of 9700 VAR, which makes 0.7 source PF, which is away from the unity value. The AIT2FL-IIBPG-based SRF DSTATCOM device

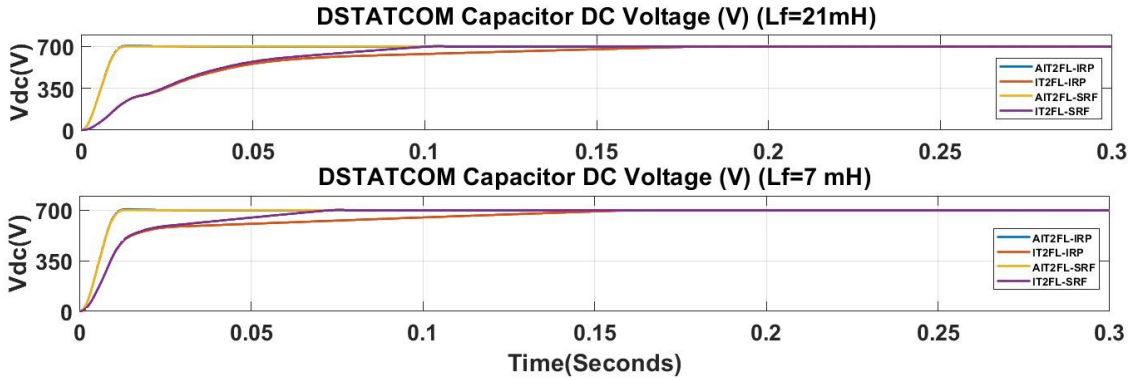

Fig. 13 Capacitor DC voltage signal response comparison at rectified nonlinear load 4 kVA 0.7 PF

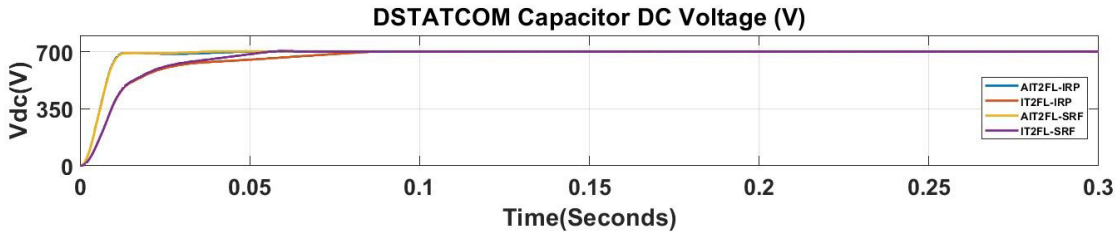

Fig. 14 Capacitor DC voltage signal response comparison at rectified nonlinear load 14 kVA 0.7 PF

starts to work at the time $t = 0.1$ s, and as the Fig. 15 depicts, it has a fast capacitor DC voltage response within a settling time of 40 ms. It improves the source current wave shape making it sinusoidal and smooth with THD of 3.19%, and it improves the source PF to the value 0.98 near to the unity because the DSTATCOM device supplied the load with reactive power needed 7840 VAR while the electrical source supplied the load with only 1860 VAR after the compensating process started (see Figs. 15 and 16).

4.2 Changing rectified nonlinear loads

Table 6 shows source current THD and Source PF comparison at changing rectified loads.

The purpose of this situation is to test the new control algorithm AIT2FL-IIBPG-based IRP and SRF under changing loads, and to compare its working along with the normal IT2FL-based IRP and SRF and without using the DSTATCOM device. The applied loads changed between four rectified loads in the time 0–1 s. The first rectified load applied is 2 kVA 0.7 PF between the time 0–0.3 s, the second rectified load applied is 8 kVA 0.7 PF between time 0.3–0.5 s, the third rectified load is 4 kVA 0.7 PF between time 0.5–0.8 s, the fourth load 14 kVA 0.7 PF between time 0.8–1 s. The source parameter without using the DSTATCOM device was source current THD 11.17% at load 2 kVA between 0–0.3 s, 11.01% at load 8 kVA between 0.3–0.5 s, 11.03% at load 4 kVA between 0.5–0.8 s and 10.85% at 12 kVA between 0.8–1 s with 0.7 source PF. The use of normal IT2FL-based SRF with interface inductor $L_f = 7$ mH for compensating makes the source parameters, source current THD, as 16.27% at load 2 kVA between 0–0.3 s, 4.55% at load 8 kVA between 0.3–0.5 s, 8.41% at load 4 kVA between 0.5–0.8 s, 4.08% at 12 kVA between 0.8–1 s with 0.98 source PF.

The IT2FL-based SRF control algorithm failed in improving the source current THD at the load 2 kVA and 4 kVA because it is tuned to the load 12 kVA and it uses the interface inductor, which is specialized to 12 kVA, and it shows a slow capacitor DC voltage response in comparison with the new control algorithm. The use of the new AIT2FL-IIBPG-based IRP with interface inductor bank for compensating makes the source parameters, source current THD, as 4.91% at load 2 kVA between 0–0.3 s, 3.90% at load 8 kVA between 0.3–0.5 s, 4.19% at load 4 kVA between 0.5–0.8 s, 3.95% at 12 kVA between 0.8–1 s with 0.98 source PF. The use of the new AIT2FL-IIBPG-based SRF with interface inductor bank for compensating makes the source parameters, source current THD, as 4.77% at load 2 kVA between 0–0.3 s, 3.80% at load 8 kVA between 0.3–0.5 s, 4.23% at load 4 kVA between 0.5–0.8 s, 3.37% at 12 kVA between 0.8–1 s with 0.98 source PF (see Figs. 17 and 18).

The application of the new AIT2FL-IIBPG-based conventional controller improves the source parameters source current THD and PF at all different rectified loads within the apparent rate of DSTATCOM device without tuning process because the new control algorithm tunes itself with respect to the load current value and generates pulses

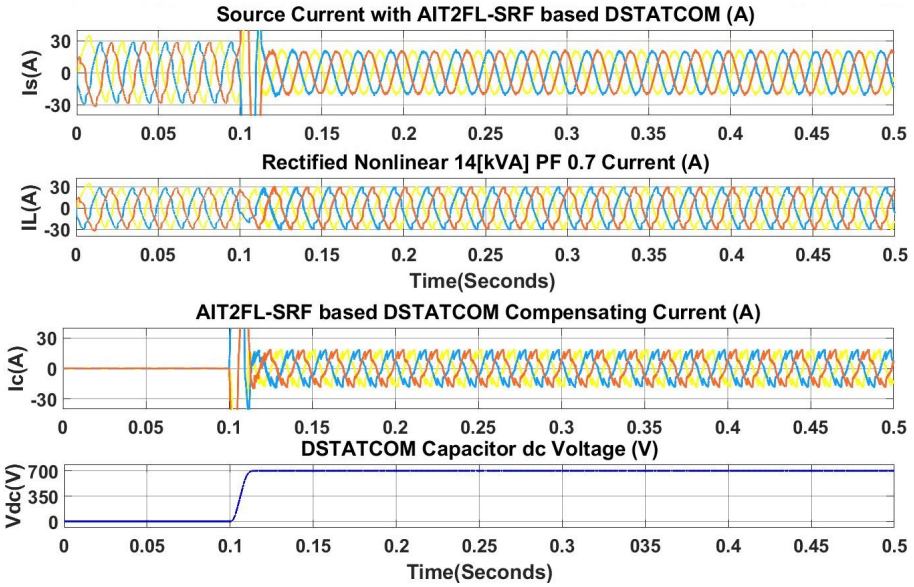

Fig. 15 Electrical grid waveforms at the rectified nonlinear load of 14 kVA 0.7 PF while using AIT2FL-IIBPG-based SRF DSTATCOM device for compensating starting from $t = 0.1$ s

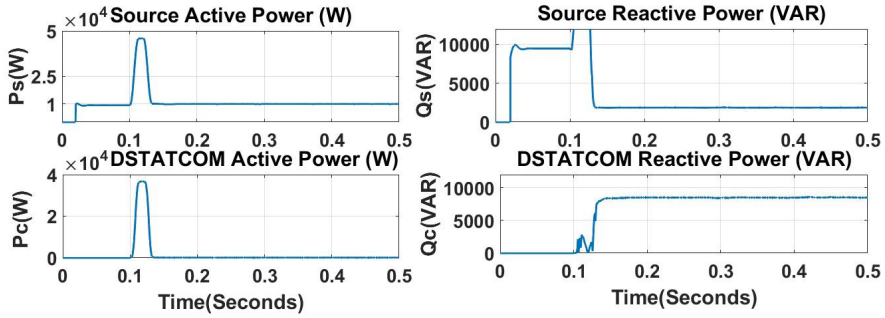

Fig. 16 DSTATCOM, source active and reactive power at the rectified nonlinear load of 14 kVA while using AIT2FL-IIBPG-based SRF DSTATCOM device for compensating starting from $t = 0.1$ s

Table 6 Source current THD and source PF comparison at changing rectified loads

Controller	L_f (mH)	Rectified load 2 kVA 0.7 PF $t = 0$–0.3 s		Rectified load 8 kVA 0.7 PF $t = 0.3$–0.5 s		Rectified load 4 kVA 0.7 PF $t = 0.5$–0.8 s		Rectified load 14 kVA 0.7 PF $t = 0.8$–1 s	
		THDs	PFs	THDs	PFs	THDs	PFs	THDs	PFs
W-DSTATCOM	–	11.17%	0.7	11.01%	0.7	11.03%	0.7	10.85%	0.7
AIT2FL_IRP	A–L_f	4.91%	0.98	3.90%	0.98	4.19%	0.98	3.95%	0.98
IT2FL_IRP	$L_f = 7$	7.54%	0.98	4.71%	0.98	8.53%	0.98	3.19%	0.98
AIT2FL_SRF	***A*–L_f**	**4.77%**	**0.98**	**3.80%**	**0.98**	**4.23%**	**0.98**	**3.37%**	**0.98**
IT2FL_SRF	$L_f = 7$	16.27%	0.98	4.55%	0.98	8.41%	0.98	4.08%	0.98

via interface inductor bank pulse generator to switch on the suitable interface inductor group with respect to the load in the interface inductor bank. The AIT2FL-IIBPG-based SRF is better than AIT2FL-IIBPG based IRP in improving the source parameters THD and PF. First, between the time 0–0.3 s the interface inductor bank pulse generator generates signals to the breaker because of the changing of capacitor DC voltage (DSTATCOM switch on period), so it improves capacitor DC voltage response and makes the settling time at the value of 50 ms, and when there is no changes in the capacitor DC voltage, it generates the pulse to the breaker of the first interface inductor group L_{f1} to switch it on with respect to the load current value, which improves the source current THD at this period. Second, between the time 0.3–0.5 s, the interface inductor bank generator generates a pulse to the breaker of

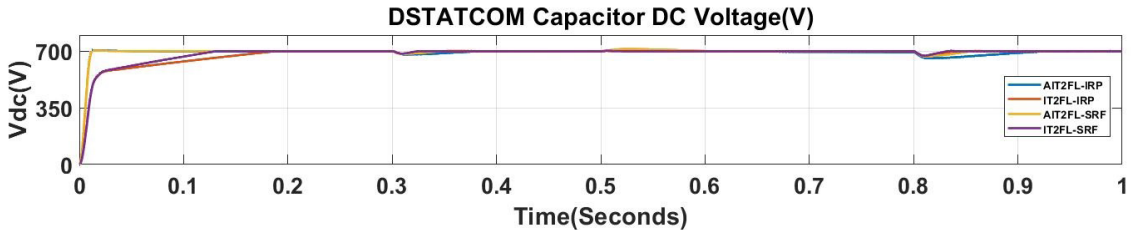

Fig. 17 Capacitor DC voltage signal response comparison at changing rectified nonlinear loads

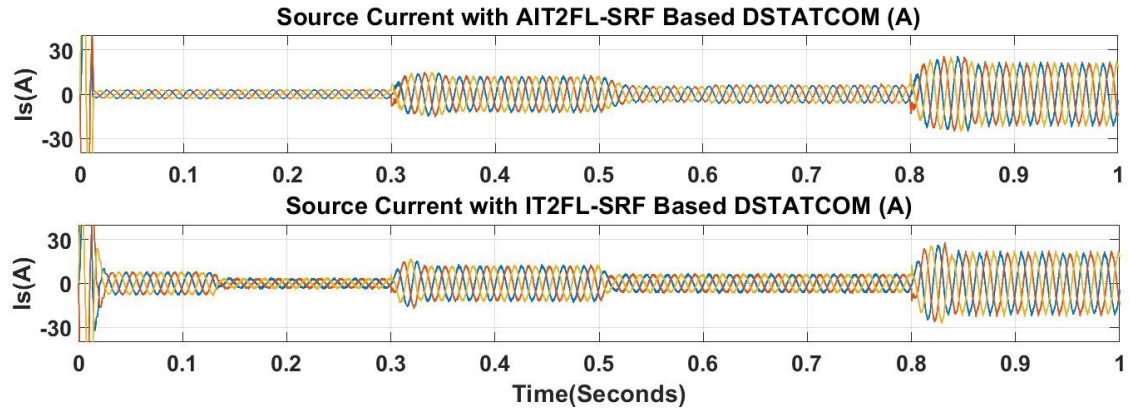

Fig. 18 Source current waveform comparison between AIT2FL-SRF and IT2FL-SRF at changing rectified nonlinear loads

the third interface inductor bank group L_{f3} to switch it on with respect to the current load value, which improves the THD at this period. Third, between the time 0.5–0.8 s, the interface inductor bank generator generates a pulse to the breaker of the second interface inductor bank group L_{f2} to switch it on with respect to the current load value, which improves the THD at this period. Fourth, between the time 0.8–1 s, the interface inductor bank generator generates a pulse to the breaker of the fourth interface inductor bank group L_{f4} to switch it on with respect to the current load value, which improves the THD at this period (see Fig. 19).

4.3 Unbalanced rectified load 14 kVA 0.7 PF

The purpose of this situation is to test the new control algorithm AIT2FL-IIBPG-based IRP and SRF under an unbalanced load and compare its working along with the normal IT2FL-based IRP and SRF. The rectified nonlinear load 14 kVA 0.7 PF is used in this situation. The three-phase load is connected from time 0–0.2 s and 0.5–0.6 s. Phase A is switched off between 0.2–0.5 s and phase B is switched off between 0.3–0.4 s.

In other words, one-phase load is switched off between 0.2–0.3 s and 0.4–0.5 s and two-phase load is switched off between 0.3–0.4 s. The use of normal IT2FL-based SRF makes the electrical source parameters as source current THD 3.74% when three phases are on, 14.27% when one phase is off and 26.76% when two phases are off with 0.98 PF. The use of new AIT2FL-IIBPG-based IRP makes the electrical source parameters as source current THD 3.26% when three phases are on, 4.87% when one phase is off and 9.48% when two phases are off with 0.98 PF. The use of new AIT2FL-IIBPG-based SRF makes the electrical source parameters as source current THD 3.26% when three phases are on, 3.28% when one phase is off and 5.89% when two phases are off with 0.98 PF (see Figs. 20 and 21, and Table 7).

The application of the new AIT2FL-IIBPG-based conventional controller keeps the source current sinusoidal and balanced with an acceptable THD rate through the different situations of severe unbalanced load and increases the capacitor DC voltage response keeping it constant at the reference value of 700 V (see Fig. 22). The new control algorithm works to improve the working of the DSTATCOM device as follows. First, AIT2FL controller, which tunes itself with respect to the load current, improves the source current THD and keeps the capacitor DC voltage at the reference rate. Second, IIBPG switches on the suitable interface inductor bank group with respect to load current and improves the source current THD. Third, it mentors the neutral load current and generates pulses to the fourth leg of DSTATCOM devices to generate neutral compensating current to keep the neutral source current at zero value (see Figs. 23 and 24).

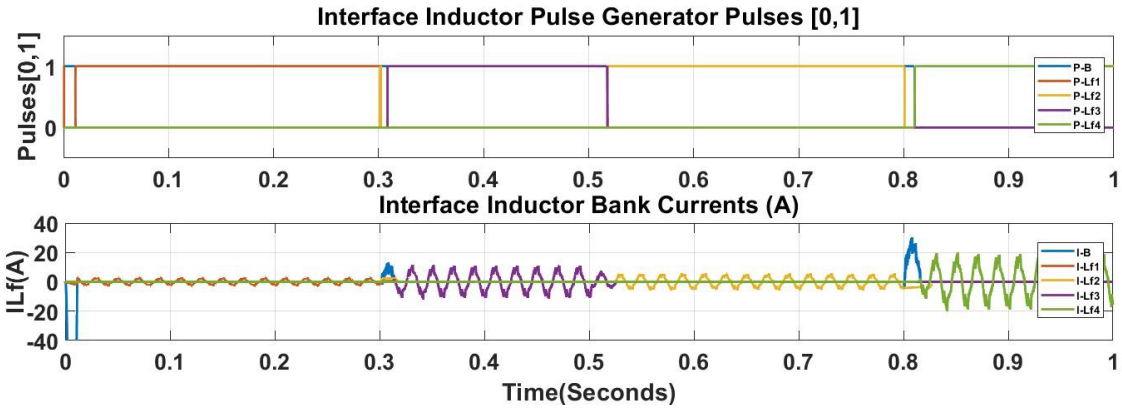

Fig. 19 Interface inductor bank pulse generator and the response of interface inductor bank groups during the changing of rectified loads while using AIT2FL-IIBPG-based SRF DSTATCOM

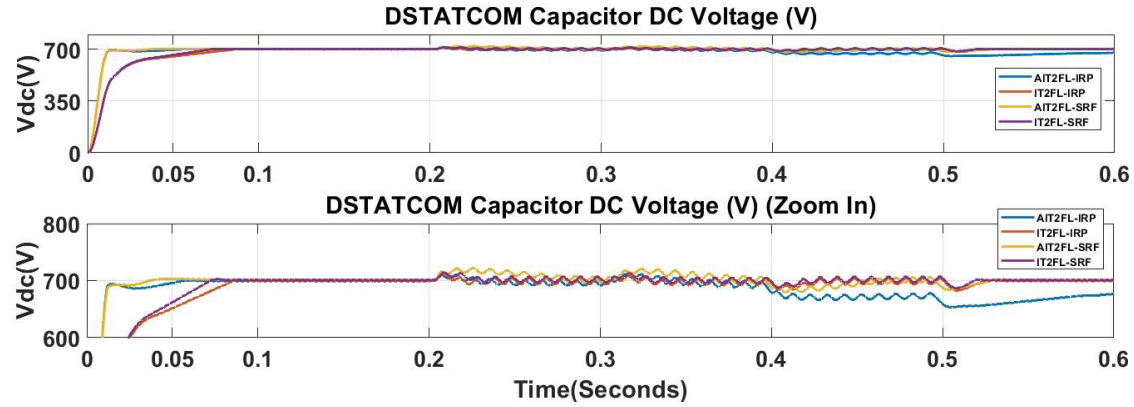

Fig. 20 Capacitor DC voltage response comparison at Rectified unbalanced load 14 kVA 0.7 PF

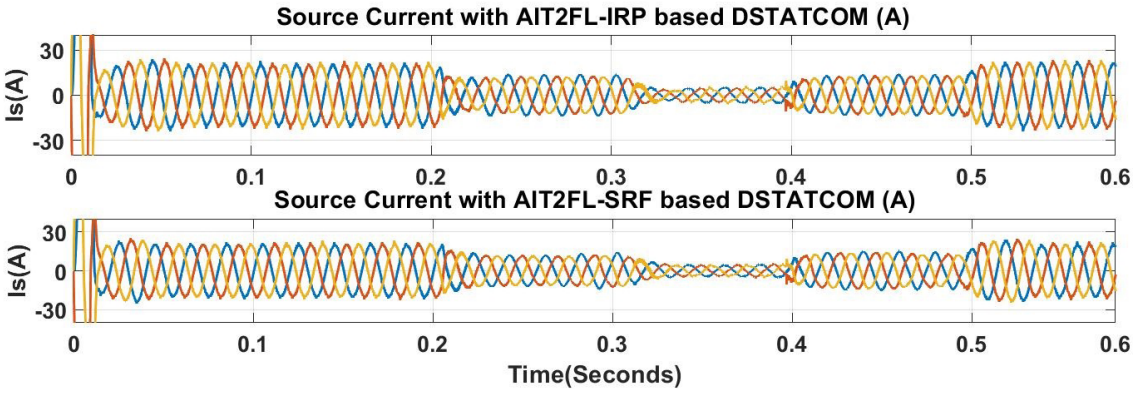

Fig. 21 Source current waveform comparison at Rectified unbalanced load 14 kVA 0.7 PF

Table 7 Source current THD and source PF comparison at changing rectified loads

Controller	Rectified load 14 kVA 0.7 PF Three load phases on 0–0.2 s and 0.5–0.6 s		Rectified load 14 kVA 0.7 PF One load phase off 0.2–0.3 s and 0.4–0.5 s		Rectified load 14 kVA 0.7 PF Two load phases off 0.3–0.4 s	
	I_s–THD	S–PF	I_s–THD	S–PF	I_s–THD	S–PF
AIT2FL_IRP	3.26%	0.98	4.87%	0.98	9.48%	0.98
IT2FL_IRP	3.30%	0.98	19.75%	0.98	32%	0.98
AIT2FL_SRF	3.26%	0.98	3.28%	0.98	5.89%	0.98
IT2FL_SRF	3.74%	0.98	14.27%	0.98	26.76%	0.98

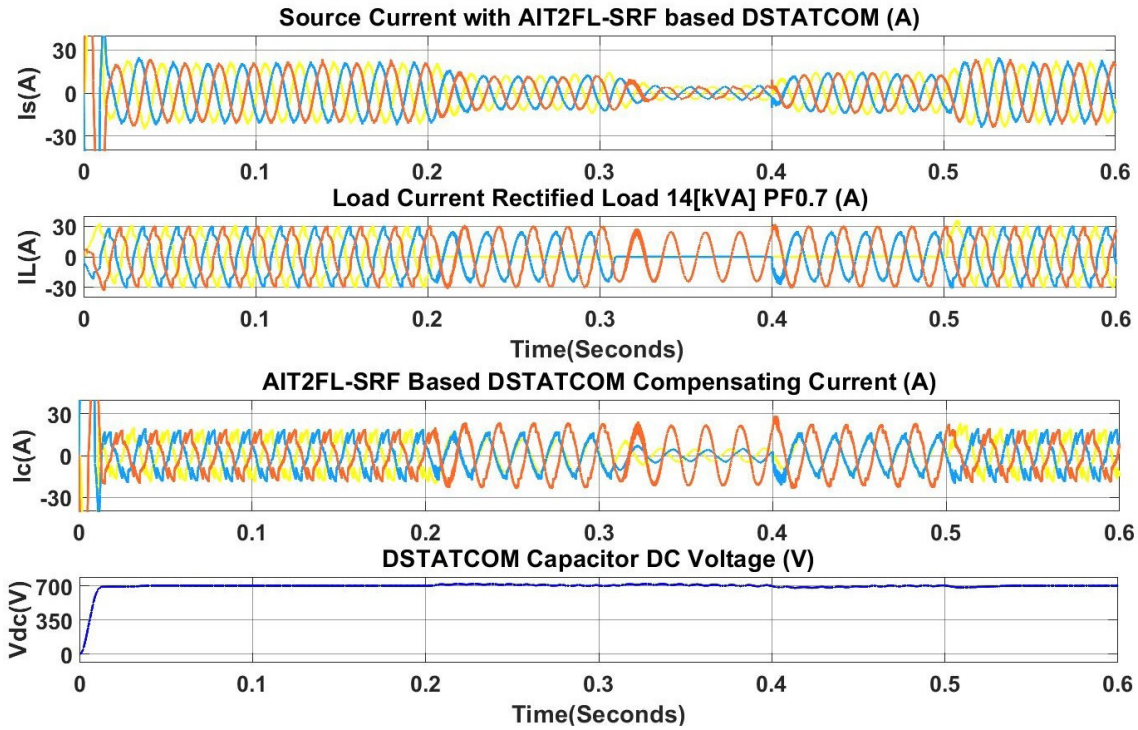

Fig. 22 Electrical grid waveforms at the rectified nonlinear unbalanced load of 14 kVA 0.7 PF while using AIT2FL-IIBPG-based SRF DSTATCOM device

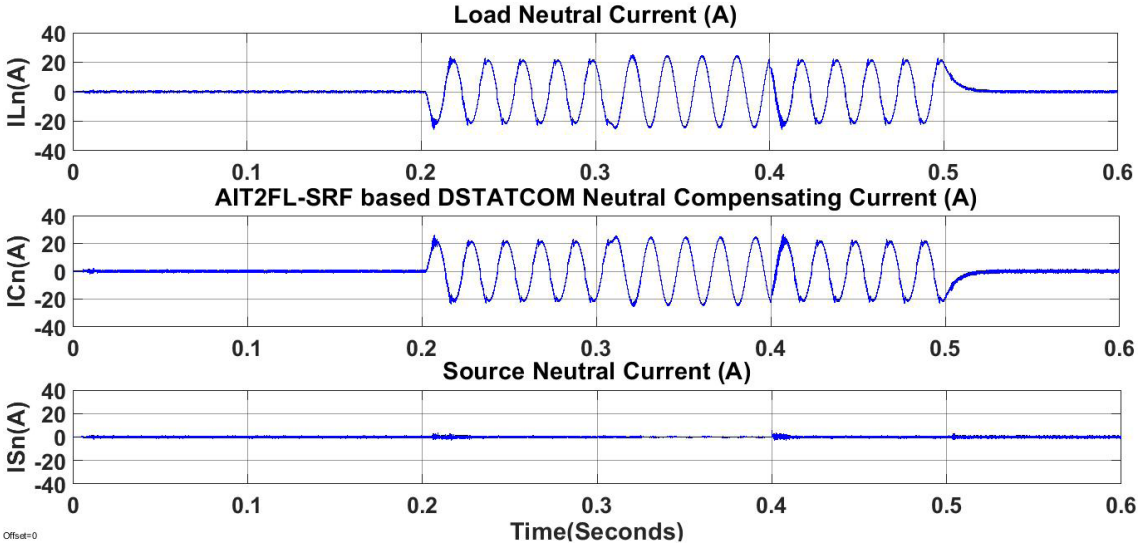

Fig. 23 Neutral currents at rectified nonlinear unbalanced load 14 kVA 0.7 PF while using AIT2FL-IIBPG-based SRF DSTATCOM device

4.4 Changing of pulse width modulation switching frequency

The pulse width modulation switching frequency is one of the important parameters should be taken into consideration while designing the DSTATCOM device. The desired high harmonics to be eliminated is playing an important role in defining the PWM switching frequency. The interface inductor should be calculated with respect to the PWM switching frequency. The common PWM switching frequency is 10 kHZ. The following PWM switching frequencies 1000, 5000, 10000, 20000 HZ at the constant rectified nonlinear load 14 kVA 0.7 PF are used to evaluate the adaptive interval type II fuzzy logic-based IRP and SRF-based DSTATCOM device. The parameters used for evaluation are as follows. First, electrical source parameters, source current THD and source power factor PF; Second, DC capacitor bus voltage response parameters, RT, PT, ST and OS%, as depicts in Tables 8 and 9. The PWM generator (2LEVEL) block is used in MATLAB for changing the switching frequency.

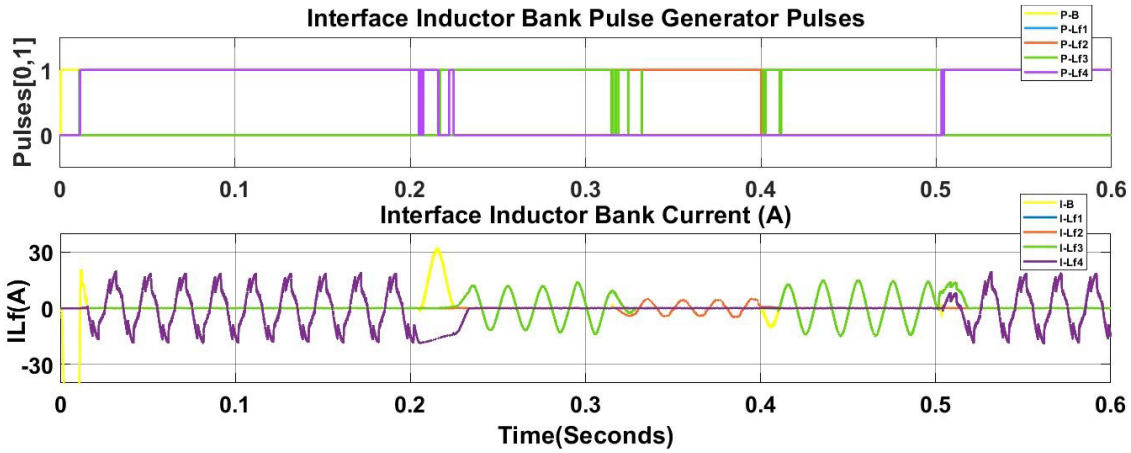

Fig. 24 Interface inductor bank pulse generator and the response of interface inductor bank groups during the rectified unbalanced load 14 kVA 0.7 PF while using AIT2FL-IIBPG-based SRF DSTATCOM

Table 8 Capacitor DC voltage signal response comparison at rectified nonlinear load 14 kVA 0.7 PF

Controller	Switching frequency (HZ)	V_{DC} parameter				
		RT (ms)	PT (ms)	ST (ms)	OS (%)	P (V)
AIT2FL_IRP	1000	7.4	13	55	0%	700
	5000	7.4	13	55	0%	700
	10000	7.4	13	55	0%	700
	20000	7.4	13	55	0%	700
AIT2FL_SRF	1000	7.4	13	40	0%	700
	5000	7.4	13	40	0%	700
	10000	7.4	13	40	0%	700
	20000	7.4	13	40	0%	700

Table 9 Source current THD and source PF comparison at rectified nonlinear load 14 kVA 0.7 PF

Controller	Switching frequency (HZ)	Electrical source parameter			
		I_s–THD	P_s (W)	Q_s (VAR)	S–PF
AIT2FL_IRP	1000	4.78%	9880	1800	0.983
	5000	3.99%	9880	1800	0.983
	10000	3.85%	9880	1800	0.983
	20000	3.80%	9880	1800	0.983
AIT2FL_SRF	1000	4.62%	9880	1800	0.983
	5000	3.90%	9880	1800	0.983
	10000	3.45%	9880	1800	0.983
	20000	3.40%	9880	1800	0.983

First, the changing of switching frequency affects the source current THD. The increasing of the switching frequency improves the source current THD with the same source power factor 0.983 as follows, the low switching frequency 1000 HZ gives the maximum source current THD at 4.78% 4.62% with AIT2FL-based IRP SRF respectively, the high switching frequency 20000 HZ gives the minimum source current THD at 3.80% 3.40% with AIT2FL-based IRP SRF respectively; it can be noted that the changing of switching frequency affects the source current THD in a small margin between 10000 HZ and 20000 HZ around 0.05%.

Second, the changing of switching frequency doesn't affect the DC capacitor bus voltage response parameters. All the parameters RT, PT, ST and OS% remains the same at all values of switching frequency as RT of 55 ms for AT2FL-based IRP and RT of 40 ms for AT2FL-based SRF (see Figs. 25 and 26).

The common switching frequency of 10 kHZ gives almost the same source electrical parameters and DC

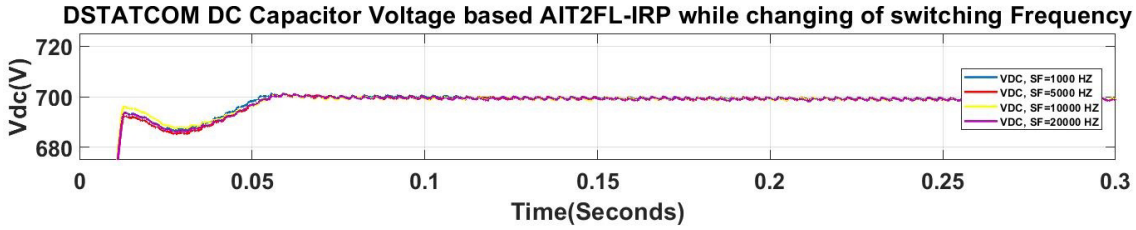

Fig. 25 The DSTATCOM capacitor DC voltage response to the AIT2FL_IRP with respect to changing of PWM switching frequency

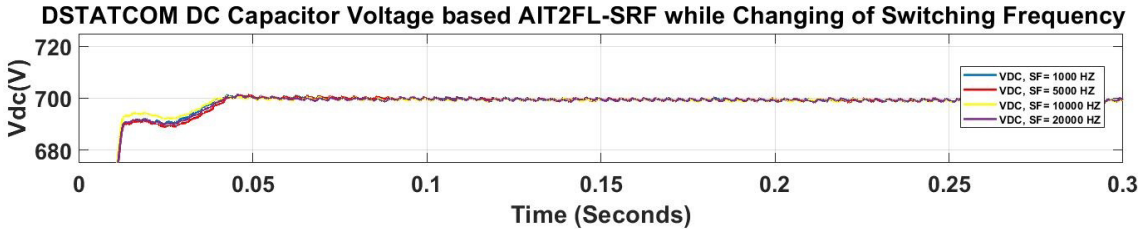

Fig. 26 The DSTATCOM capacitor DC voltage response to the AIT2FL_SRF with respect to changing of PWM switching frequency

capacitor voltage response parameters as the switching frequency of 20 kHZ. The common switching frequency 10 kHZ is the optimal PWM switching frequency to be applied and there is no need for increasing it over 10 kHZ.

5 Comparison with relevant studies

The interval type II fuzzy logic with recursive least square (RLS) is used to control the DSTATCOM device integrated to low voltage grid to improve the power quality for sensitive local load when the connecting and disconnecting process. The control algorithm used is somehow simple but it is not adaptive or self-tunning and it is tuned to suit a specific load. The capacitor of DSTATCOM used has a small capacity which suits the low voltage grid. The DSTATCOM device has one interface inductor for all type of loads. The DC capacitor bus voltage response is discussed and compared with the other controllers [8]. The interval type II fuzzy logic for controlling DSTATCOM device connected to the high voltage grid toimprove the power quality for the low voltage load and high voltage load at the same time. The control algorithm used is simple but it is not adaptive or self-tunning and it is tuned to suit a specific load. The capacitor of DSTATCOM device has a high value in comparison with the other studies to suit the high voltage grid. The DSTATCOM device has one interface inductor for all type of loads. The DC bus capacitor voltage response is not discussed [25].

The online trained wavelet Takagi-Sugeno-Kang fuzzy neural network (WTSKFNN) controller is used for controlling DSTATCOM device to keep the DC capacitor bus voltage constant during the variation of loads. The control algorithm used is complicated and adaptive to the load variations. The DC capacitor of DSTATCOM device has a low value to suit the low voltage grid. The DSTATCOM device has one interface inductor for all type of loads. The DC capacitor bus voltage response to the control system is not discussed or compared with the other controller [30].

An Interval type I fuzzy logic with new membership functions of the error signal is used for controlling DSTATCOM device to improve the power quality. The control algorithm used is somehow simple but it is not adaptive or self-tunning. The DC capacitor of DSTATCOM device has a low value to suit the low voltage grid. The DSTATCOM device has one interface inductor for all type of loads. The DC capacitor bus voltage response to the control system is not discussed or compared with the other controller [23].

A neuro fuzzy logic controller is used to control DSTATCOM device with training algorithm to improve the power quality in the situation of load variation. The control algorithm is somehow complicated and adaptive. The DC capacitor of DSTATCOM device has a low value to suit the low voltage grid. The DSTATCOM device has one interface inductor for all type of loads. The DC capacitor bus voltage response to the control system is not discussed or compared with the other controller [29].

In this study, adaptive interval type II fuzzy logic-based conventional controller is used to make the DSTATCOM device self-tunning. The control algorithm which used in this paper is somehow simple and adaptive to the load variation. The DC capacitor of DSTATCOM device has a low value to suit the low voltage grid. The DSTATCOM device has interface inductor bank which chooses the suitable interface inductor for each type of loads. The DC capacitor bus voltage response to the control system is studied and compared with the interval type II fuzzy logic. Table 10 depicts the comparison with the relevant studies.

Table 10 Comparison with relevant studies

Ref.	Control algorithm	Artificial intelligence	Type	MSF	Adaptive	DC capacitor capacity value	DC Capacitor voltage response comparison	THD comparison	Inductor bank with pulse generator
[8]	IT2FL	Yes	Simple	3	No	Low	Yes	Yes	No
[25]	IT2FL	Yes	Simple	7	No	High	No	No	No
[30]	WTSKFNN	Yes	Complicated	–	Yes	Low	No	Yes	No
[23]	IT1FL	Yes	Simple	7	No	Low	No	Yes	No
[29]	NFL	Yes	Complicated	–	Yes	Low	No	Yes	No
This study	**Adaptive IT2FL**	**Yes**	**Simple**	**3**	**Yes**	**Low**	**Yes**	**Yes**	**Yes**

6 Conclusions

The three-phase four-wire DSTATCOM device with interface inductor bank is used in this study for power quality improvement in the low voltage distribution grid. The normal interval type II fuzzy logic control algorithm tunes to a specific load and starts to lose its efficiency while it is integrated into a different load. According to the simulation results, the adaptive interval type II fuzzy logic control algorithm with the new interface pulse generator suits all types of loads. Therefore, the main contributions of this study are:

1. DSTATCOM device becomes a plug-and-play device within its apparent power rate by using simple and adaptive control algorithm;
2. the simple and adaptive type II fuzzy logic control algorithm succeeds in improving the source current harmonic distortion during the load changing;
3. the adaptive interface inductor bank succeeds in making fast DC capacitor bus voltage response with different types of loads.

Nomenclature

V_{DC}	The DC capacitor bus voltage
V_{DC1}	The minimum voltage level of DC bus
V^{*}_{DC}	The DC capacitor bus voltage reference
$V_{\mathrm{DC}(n)}$	The DC capacitor bus voltage at the n^{th} sampling instant
$E_{(n)}$	Error signal of the DC capacitor bus voltage at the n^{th} sampling instant
$E_{(n-1)}$	Error signal of the DC capacitor bus voltage at the $(n-1)^{\mathrm{th}}$ sampling instant
C_{DC}	The capacity of the DC capacitor
L_f	Interface inductor
$A\text{–}L_f$	Adaptive interface inductor
V_{LL}	The load voltage line to line
V	The load phase voltage
m	The modulation index
a	The over loading factor
I	The phase current
t	The time by which the DC bus voltage is to be recovered
$i_{cr(p-p)}$	Current ripple
f_s	Switching frequency
V_a, V_b, V_c	Three phase load voltage in abc format
V_α, V_β, V_0	Three phase load voltage in 0-α-β format
$\cos\theta$, $\sin\theta$	Cosine and sine of phase angle of three phase voltages.
I_{La}, I_{Lb}, I_{Lc}	Three phase load currents in abc format
I_α, I_β, I_0	Three phase load currents in 0-α-β format
I_0, I_d, I_q	Three phase load currents in 0-d-q format
$I_d^{\sim}$	The alternating load direct current component
I_{LdF}	The filtered load direct current component
$I_{LdF(n)}$	Filtered load direct current component at the n^{th} sampling instant
I_{dadj}	The direct current adjusting signal
$I_{dadj(n)}$	The direct current adjusting signal at the nth sampling instant
$I_{dadj\%(n)}$	The direct current adjusting percentage signal at the n^{th} sampling instant
I^{*}_{Sd}	The source direct current component reference
$I_q^{\sim}$	The alternating load quadrature current component
I_{qLF}	The filtered load quadrature current component
I^{*}_{Sq}	The source quadrature current component reference
$I^{*}_{S\alpha}$, $I^{*}_{S\beta}$, I^{*}_{S0}	Source current references in α-β-0 format
I^{*}_{Sa}, I^{*}_{Sb}, I^{*}_{Sc}	Source current references in a-b-c format
P	Load active power
$P^{\sim}$	Load active power *ac* component
P_{LF}	Filtered load active power component
$P_{LF(n)}$	Filtered load active power at the n^{th} sampling instant

P_{adj}	Adjusting active power
$P_{adj(n)}$	The active power adjusting signal at the n^{th} sampling instant
$P_{adj\%(n)}$	The active power adjusting percentage signal at the n^{th} sampling instant.
P_S^*	Source active power reference
q	Load reactive power
$q^{\sim}$	Load reactive power *ac* component
q_{LF}	Load reactive power filtered component
q_S^*	Source reactive power reference
$AK_{p(n)}$	Adaptive proportional constant at the n^{th} sampling instant
$Ak_{I(n)}$	Adaptive integral constant at the n^{th} sampling instant
Erra, *Errb*, *Errc*	Three error signals for pulse width modulation
RT	Rising time
PT	Peak time
ST	Settling time
OS	Over shoot
P	Peak value
THD	Total harmonic distortion
S-PF	Source power factor

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