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Flying Capacitor Voltage Balancing Control Strategy Based on Logic-equations in Five Level ANPC Inverter

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Abstract

This paper proposes a novel voltage balancing control approach for the flying capacitors in a five-level Active-Neutral-Point-Clamped inverter (ANPC). The projected method is based on the control signal of the flying capacitor (FC) voltage. A Staircase reference voltage-based Phase-Shifted PWM (PS-PWM) technique is used to generate the different levels and simple logic-equations. The proposed control can regulate the voltage of the FC at the requested reference value and generate the required five-level output voltage with fast dynamics. It requires fewer and simpler calculations and it has a fast execution time. The Simulations are performed using MATLAB and Simulink. The obtained results demonstrate the good performance of the FC voltage control and the high quality of the output voltages and current spectrum.

Keywords

capacitor voltage balancing, multilevel inverter, ANPC inverter, PS-PWM, logic-equations

1 Introduction

In recent years, multilevel converters have become more popular in high-power medium-voltage applications due to their numerous advantages, such as reduced voltage stress, low gradient dv/dt, low switching frequency, low harmonic distortion, and high-power quality [1–8]. However, these topologies encounter problems as the voltage level increases. Examples include the control complexity of the neutral-point voltage in NPC converters and the FC voltage in FC converters. Moreover, the number of clamping diodes in NPC converters and the flying capacitors present in FC converters increases. Therefore, in the case of the cascade H-bridge converters, more isolated DC sources are required [9, 10]. These problems make the converters more expensive and impact the reliability and efficiency of the converters. The active-neutral-point-clamped (5L-ANPC) converter is one of the new topologies of multilevel converters [11–14]. It has been introduced to overcome these problems. It's an attractive multilevel topology and the most commercialized [15, 16]. The 5L-ANPC converter is a combination of the 3L-NPC converter and the 3L-FC converter [17–19]. It contains two capacitors on the DC-link side, one floating capacitor, and eight switches per phase. Thus, the total volume, cost, and control complexity can be reduced [20]. Moreover, this topology has the advantage of being more robust and more flexible, with the size of the output filters being smaller and it has less power loss [21]. The main problem with this topology is that the capacitors and FCs in the intermediate circuit have different voltages [22].

Serval modulation methods have been presented in the literature to control the 5L-ANPC converter, such as phase disposition carrier-based PWM (PD-PWM) in [23]. It has good harmonic performance. The flying capacitor voltages are balanced by selecting the appropriate redundant switching states in each period, and the neutral point voltage is balanced by a zero-sequence voltage method. [24] proposes a traditional phase shifted carrier-based (PS-PWM), which naturally balances the DC-link capacitor and FCs voltage. However, in certain dynamic conditions, such as grid-tied, the capacitors voltages may diverge, leading to a decline in the converter's performance. [25] introduces a level shifted-phase shifted carrier-based (LS-PS-PWM) modulation method. It is based on two carriers shifted in phase and in magnitude to reduce output THD. In order

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to combine the advantages of the PD-PWM and PS-PWM methods, an optimized carrier-based PWM method is proposed in [15]. This strategy is based on modifying the shape of carriers. A phase-shifted PWM technique is proposed in [20]. The regulation of FCs voltage is achieved by adjusting the action time of two redundant switching states. Both methods utilize an optimum zero-sequence voltage to balance the neutral point voltage.

Elimination of common-mode voltage using modified SVPWM is proposed in [26]. This method employs 19 voltage vectors that produce a zero common-mode voltage among all the 125 voltage vectors. However, this method uses a limited number of voltage vectors resulting in an increase in THD. An SVPWM based on multispacer voltage vector mapping is proposed in [27]. It involves dividing the five-level voltage space vector into two-level voltage space vector subdivisions. Therefore, the calculation of the composite vector and its action time is simplified. The balance of the neutral point voltage is achieved by selecting the initial vectors appropriately, ensuring that the effect of the switching sequence on the neutral point voltage is equal in magnitude and opposite in direction in mutually symmetrical sectors [27]. Another SVPWM method based on line voltage coordinate is proposed in [28]. It simplifies the steps of determining the basic vector and its action time. [29] proposes a virtual coordinate-based optimized SVPWM. This strategy, avoids the dead-time effects by constraining transitions between different switching states. In [28] and [29], the neutral point voltage is balanced in each control period by selecting the appropriate switching sequence vector. All these methods exhibit good performance, but at higher voltage levels their complexity increases due to the to the growing number of voltage vectors and redundant switching states [22].

Due to the complexity of the five-level SVPWM algorithm, a hybrid modulation method is proposed in [21] in order to reduce the complexity and computation process. It combines between the three-level SVPWM and PS-PWM. The both modulation methods are used to control the 5L-ANPC converter. The neutral point voltage and the FCs voltage are balanced by using the well-developed three-level SVPWM and PS-PWM methods, respectively.

A Selective harmonic elimination PWM (SHE-PWM) method is proposed in [30]. It is based on offline computations in order to eliminate the harmonics distortion. The FCs voltage is balanced by changing the switching patterns of the switches based on the polarities of the FC voltage, fundamental phase voltage and the output current. This method requires storing the solutions and it is also challenging to calculate the appropriate angles in real time [15].

The main goal of the new control method presented in this paper is to overcome the problem of FCs unbalance voltage in the 5L-ANPC inverter. It's based on the control signal of the FCs voltage, a staircase reference voltage based on the PS-PWM technique, and simple logic-equations. The DC-link capacitor voltages are naturally balanced. The FCs voltage is regulated at its reference value along with producing the requested output voltage with fast dynamics. Moreover, this method uses fewer and simpler mathematical equations based on the binary system, resulting in execution time. The control method is simulated and verified using MATLAB/Simulink. This paper is organized as follows. Section 2 presents the operation principles of the 5L-ANPC converter. Section 3 introduces the proposed control method based on logic-equations. Simulation results are presented in Section 4. Finally, Section 5 concludes the paper.

2 Proposed method for capacitor voltage balancing control in 5L-ANPC converter

Fig. 1 presents the phase leg of the 5L-ANPC converter. It consists of two cells. The first cell contains two capacitors C_1 and C_2 forming the DC-link bus, and four line-frequency switches $(S_{x1},\ S'_{x1})$ and $(S_{x2},\ S'_{x2})$. The second cell contains one flying capacitor C_{fcx}, with four high-frequency switches $(S_{x3},\ S'_{x3})$ and $(S_{x4},\ S'_{x4})$. The voltage across the DC-link capacitors is assumed to be constant and equal

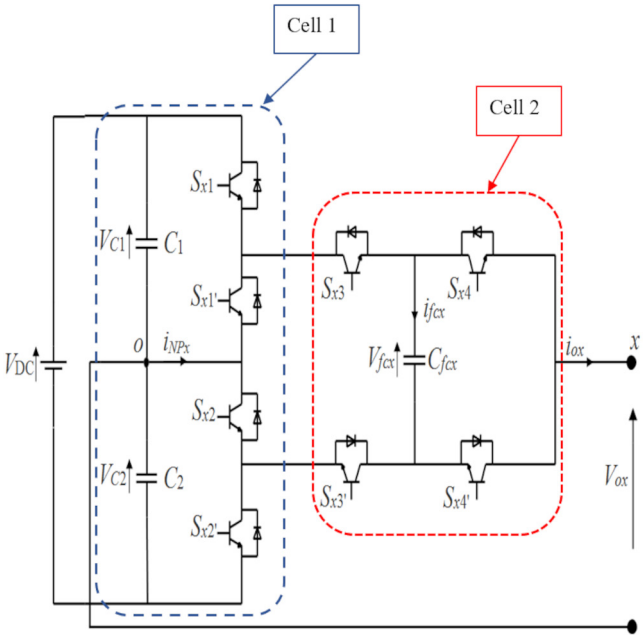


Fig. 1 Phase leg of the 5L-ANPC converter

to $V_{DC}/2$, then the voltage across the flying capacitor is equal to $V_{DC}/4$. All the switching states are summarized in Table 1, where the symbol x represents the phase number a, b, c, and i_{fcx}, i_{NPx} represent the corresponding FC current and NP current, respectively and i_{ox} is the phase output current.

Looking at the following Table 1, we can assume that the operation of the switch pairs $(S_{x1},\ S'_{x1})$, $(S_{x2},\ S'_{x2})$, $(S_{x3},\ S'_{x3})$ and $(S_{x4},\ S'_{x4})$ are complementary.

Moreover, the flying capacitor voltage depends only on the redundant switching states V_1, V_2, V_5 and V_6, and is not affected by the switching states V_0, V_3, V_4 and V_7. For example, the voltage level $V_{DC}/4$ and $-V_{DC}/4$ are generated by the switching states V_1 or V_2 and V_5 or V_6 respectively.

The redundant switching states of the 5L-ANPC converter are used to control the FCs voltages. At first, the variation of the flying capacitor voltage is given in [26]:

$$\Delta V_{fcx} = V_{fcx} - V_{DC}/4, \tag{1}$$

where V_{fcx} is the flying capacitor voltage of phase x.

The charging and discharging of the flying capacitor depends on the switching states and the phase current polarity. Then, the control signal of the flying capacitor voltage is given as follows [26]:

$$Sig_{Fly_x} = \Delta V_{fcx} \times i_{ox}, \tag{2}$$

where i_{ox} is the output current of phase x.

The redundant switching states of the converter are selected based on the control signal of the flying capacitor voltage. When the value of Sig_{Fly_x} is positive, which means that ΔV_{fcx} and i_{ox} are both positive or negative, the switching states V_1 and V_5 are chosen. For negative value of Sig_{Fly_x}, this means that one of ΔV_{fcx} or i_{ox} is positive and the other one is negative, the switching states V_2 and V_6 are chosen. These details are shown in Table 2.

3 New control method contribution

In order to reduce the calculations, we assume that $\gamma_x(t)$ is the logic-variable that expresses the charging or discharging state of the flying capacitor. This last variable is given as follows:

$$\gamma_x(t) = \begin{cases} 1, & Sig_{Fly_x} > 0 \\ 0, & Sig_{Fly_x} < 0 \end{cases}. \tag{3}$$

If the control signal of the flying capacitor voltage is greater than 0, $\gamma_x(t)$ equates 1. The FC requires to be discharged through redundant switching states V_2 or V_6.

If the control signal of the flying capacitor voltage is smaller than 0, $\gamma_x(t)$ becomes 0. Then, the FC needs to be charged using the available redundant switching states V_1 and V_5.

Table 1 Switching states of the 5L-ANPC converter

S_{x1}	S_{x2}	S_{x3}	S_{x4}	V_{ox}	i_{fx}	i_{NPx}	$\Delta E_{C_{fcx}}$	Switching states
1	1	1	1	$+V_{DC}/2$	0	0	Not affected	V_0
1	1	1	0	$+V_{DC}/4$	i_{ox}	0	Charge	V_1
1	1	0	1	$+V_{DC}/4$	$-i_{ox}$	i_{ox}	Discharge	V_2
1	1	0	0	0	0	i_{ox}	Not affected	V_3
0	0	1	1	0	0	i_{ox}	Not affected	V_4
0	0	1	0	$-V_{DC}/4$	i_{ox}	i_{ox}	Charge	V_5
0	0	0	1	$-V_{DC}/4$	$-i_{ox}$	0	Discharge	V_6
0	0	0	0	$-V_{DC}/2$	0	0	Not affected	V_7

Table 2 Selected switching states for flying capacitor voltage control

Flying capacitor voltage control signal	Switching states
$Sig_{Fly_x} > 0$	V_1, V_5
$Sig_{Fly_x} < 0$	V_2, V_6

3.1 The staircase reference voltage

The 5L-ANPC converter produces at the output side five voltage levels in the form of a staircase, $\pm V_{DC}/2$, $\pm V_{DC}/4$, 0 V_{DC}. As shown in Table 1, the FC voltage is affected by the redundant levels, $+V_{DC}/4$ and $-V_{DC}/4$. To control the FC voltage at its operating level. Firstly, it's necessary to generate a staircase five-level reference voltage, then, studies the logic-variable $\gamma_x(t)$ in each level.

Fig. 2 shows the staircase reference voltage generation block diagram based PS-PWM technique. In fact, the switch-

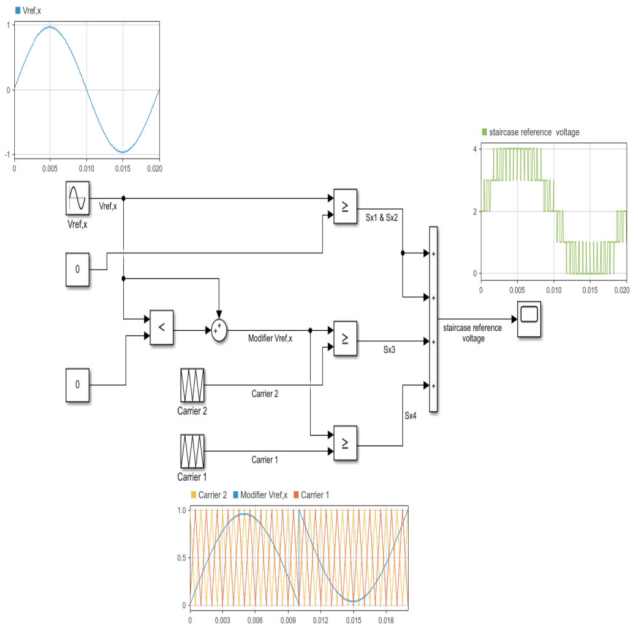


Fig. 2 Staircase reference voltage generation block diagram-based PS-PWM

es (S_{x1}, S_{x2}) and (S_{x3}, S_{x4}) can be controlled directly by the output of the three comparators. But, this control method is used in this paper to generate the staircase reference voltage by the summing of the outputs of the comparators.

The staircase reference voltage $V_{staircase,ref}$ drawn in Fig. 3, is in (p.u). The voltage levels are set by $V_{staircase,ref}$ as follows (Eqs. (4)–(8)):

$$\delta_{P2}(t)=\begin{cases}1, & V_{staircase,ref}=4\\ 0, & V_{staircase,ref}\neq 4\end{cases}\left(\frac{V_{DC}}{2}\equiv 4\ \text{p.u}\right), \tag{4}$$

$$\delta_{P1}(t)=\begin{cases}1, & V_{staircase,ref}=3\\ 0, & V_{staircase,ref}\neq 3\end{cases}\left(\frac{V_{DC}}{4}\equiv 3\ \text{p.u}\right), \tag{5}$$

$$\delta_{0}(t)=\begin{cases}1, & V_{staircase,ref}=2\\ 0, & V_{staircase,ref}\neq 2\end{cases}\left(0\times V_{DC}\equiv 2\ \text{p.u}\right), \tag{6}$$

$$\delta_{N1}(t)=\begin{cases}1, & V_{staircase,ref}=1\\ 0, & V_{staircase,ref}\neq 1\end{cases}\left(-\frac{V_{DC}}{4}\equiv 1\ \text{p.u}\right), \tag{7}$$

$$\delta_{N2}(t)=\begin{cases}1, & V_{staircase,ref}=0\\ 0, & V_{staircase,ref}\neq 0\end{cases}\left(-\frac{V_{DC}}{2}\equiv 0\ \text{p.u}\right). \tag{8}$$

3.2 Studies the logic-variable $\gamma_x(t)$ and generating the control signals

From Table 1, the 5L-ANPC converter generates three voltage levels, $\delta_{P2}(t)$, $\delta_{P1}(t)$ and $\delta_0(t)$ during positive half-cycle. If the switching functions of (S_{x1}, S_{x2}) are (T_{x1}, T_{x2}).

3.2.1 Generating voltage level $\delta_{P2}(t)$: $+V_{DC}/2$

The level voltage δ_{P2} is generated, when the switching state is V_0 which corresponds to the switches configuration (1, 1, 1, 1). Regardless of the output current polarity, the instantaneous voltage of the FC is not affected by this switching state. Thus, T_{x1}, T_{x2}, S_{x3} and S_{x4} obtain the logic coefficient of 1:

$$\begin{aligned}T_{x1}(t)&=1\times\delta_{P2}(t)\\ T_{x2}(t)&=1\times\delta_{P2}(t)\\ S_{x3}(t)&=1\times\delta_{P2}(t)\\ S_{x4}(t)&=1\times\delta_{P2}(t).\end{aligned} \tag{9}$$

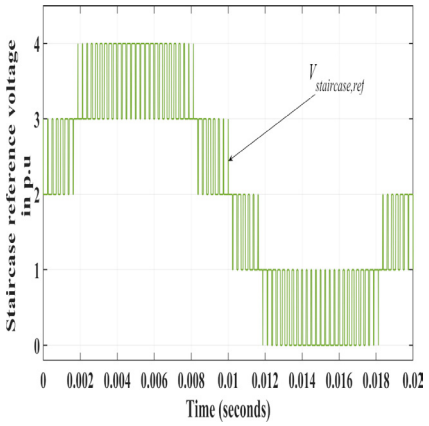


Fig. 3 Staircase reference voltage

3.2.2 Generating voltage level $\delta_{P1}(t)$: $+V_{DC}/4$

The level voltage δ_{P1} is generated, when the switching states are V_1 or V_2, which correspond to the switches configuration (1, 1, 1, 0) or (1, 1, 0, 1) respectively. The FC charges in the switching state V_1, γ_x is equal to 1. Therefore, T_{x1}, T_{x2} obtain the logic coefficient of 1, S_{x3} obtains the logic coefficient of $\gamma_x(t)$, and S_{x4} gets $\overline{\gamma_x(t)}$. The FC discharges in the switching state V_2, γ_x is equal to 0. Therefore, T_{x1}, T_{x2} obtain the logic coefficient of 1, S_{x3} obtains the logic coefficient of $\gamma_x(t)$, and S_{x4} gets $\overline{\gamma_x(t)}$:

$$\begin{aligned}T_{x1}(t)&=1\times\delta_{P1}(t)\\ T_{x2}(t)&=1\times\delta_{P1}(t)\\ S_{x3}(t)&=\gamma_x(t)\times\delta_{P1}(t)\\ S_{x4}(t)&=\overline{\gamma_x(t)}\times\delta_{P1}(t).\end{aligned} \tag{10}$$

3.2.3 Generating voltage level $\delta_0(t)$: 0 V_{DC}

The level voltage δ_0 is generated, when the switching states are V_3 or V_4, which correspond to the switches configuration (1, 1, 0, 0) or (0, 0, 1, 1) respectively. Regardless of the output current polarity, the instantaneous voltage of the FC is not affected by these switching states. In order to activate the switching states V_3 and V_4 separately the switching functions (T_{x1}, T_{x2}) are used. According to Table 1, the switching state selected to generate the voltage level δ_0 during the positive half-cycle is V_3 (1, 1, 0, 0). Therefore, T_{x1}, T_{x2} obtain the logic coefficient of 1 and the switches S_{x3} and S_{x4} obtains the logic coefficient of the product of the switches $\overline{T_{x1}}$ and $\overline{T_{x2}}$:

$$\begin{aligned}T_{x1}(t)&=1\times\delta_{0}(t)\\ T_{x2}(t)&=1\times\delta_{0}(t)\\ S_{x3}(t)&=\overline{T_{x1}}\times\overline{T_{x2}}\times\delta_{0}(t)\\ S_{x4}(t)&=\overline{T_{x1}}\times\overline{T_{x2}}\times\delta_{0}(t).\end{aligned} \tag{11}$$

A comparable explanation may also be developed for the voltage-levels of $\delta_{N2}(t)$, $\delta_{N1}(t)$ and $\delta_0(t)$. The logic-equations control of switches (S_{x1}, S_{x2}) and (S_{x3}, S_{x4}) during all the positive half cycle are given as follows (Eq. (12)):

$$
\begin{aligned}
&S_{x1}(t)=\delta_{P1}(t)+\delta_{P1}(t)+\delta_{P2}(t)\\
&S_{x2}(t)=\delta_{P1}(t)+\delta_{P1}(t)+\delta_{P2}(t)\\
&S_{x3}(t)=\delta_{P2}(t)+\gamma_x(t)\times\left(\delta_{P1}(t)+\delta_{N1}(t)\right)\\
&+\delta_0\times\overline{T_{x1}}(t)\times\overline{T_{x2}}(t)\\
&S_{x4}(t)=\delta_{P2}(t)+\overline{\gamma_x(t)}\times\left(\delta_{P1}(t)+\delta_{N1}(t)\right)\\
&+\delta_0\times\overline{T_{x1}}(t)\times\overline{T_{x2}}(t).
\end{aligned}
\tag{12}
$$

From Eq. (12) the switches (S_{x1}, S_{x2}) operate during all the positive half-cycle. As shown in Fig. 3, the levels of the staircase reference voltage are chopped, which means that we have switching losses in the switches (S_{x1}, S_{x2}). In order to reduce them, we controlled the two switches directly from the reference voltage as follows (Eq. (13)):

$$
S_{x1}=S_{x2}=\begin{cases}1, & V_{ref_x}\geq 0\\ 0, & V_{ref_x}<0\end{cases},
\tag{13}
$$

where V_{ref_x} is the reference voltage of phase x. Fig. 4 shows the diagram of the proposed control method.

The advantages of the proposed control method can be summarized in being applicable to all modulation techniques, simple mathematical calculations, simple implementation, reducing the size of the control circuit. It has a fast execution time, fast dynamic and it restricts FCs voltage ripples. Moreover, the switches (S_{x3}, S_{x4}) and $\left(S'_{x3},\ S'_{x4}\right)$ have equal switching frequency, equal losses by using the PS-PWM technique [15]. It can be implemented in real time. Table 3 shows a comparison of different modulation strategies.

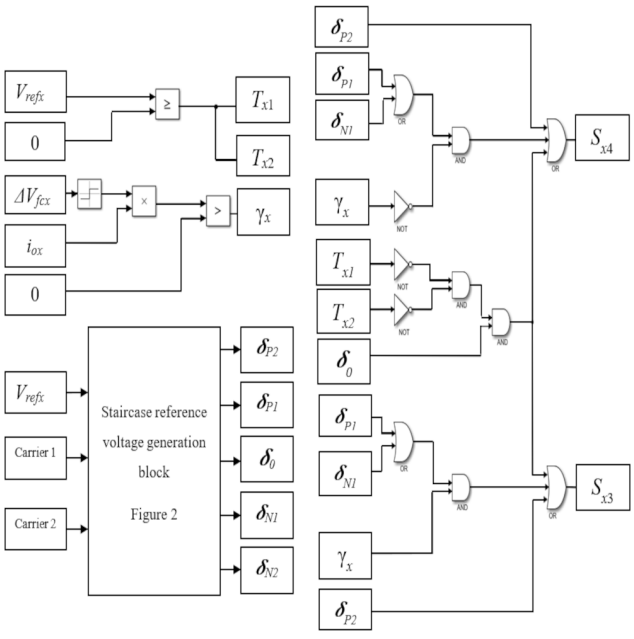


Fig. 4 The proposed control method diagram

4 Results and discussion

Simulation is carried out to verify the proposed voltage balancing control method of the flying capacitor in the 5L-ANPC converter. The specification of the simulation is given in Table 4.

Fig. 5, shows the transient and steady-state dynamics of the different voltages under ideal conditions , with a modulation index of m = 1. From Fig. 5 (c), it can be observed that the DC-link capacitors voltages C_1 and C_2 are naturally balanced and the capacitances unbalanced voltages decrease, reaching the desired operational value at 230 V. Fig. 5 (d) demonstrates that the flying capacitors voltages are well balanced at their reference value of 115 V. Moreover, the proposed control method exhibits fast dynamic, enabling rapid charging of the FCs and restricting their voltage fluctuations. Fig. 5 (a) and (b), Fig. 6 (a) and (b) display the high quality waveforms and harmonic spectrums of the phase voltage and phase current respectively. The first switching harmonic of the output voltage and current is shifted to $f_{\text{1st, switching}}=2\times f_s=10$ KHz.

In order to verify the robustness of this new control method, we carried out a test consisting in varying the DC bus voltage and thus monitoring the responses of the different variables of the system.

In Fig. 7, we can see the transient dynamics of the different voltages, when the input voltage V_{DC} changes at time

Table 3 Comparison of different modulation strategies

Modulation strategy	Computation	Complexity	Response speed	Harmonic distortion
Proposed method	Low	Low	High	Medium
Optimized PWM [15]	Medium	Medium	High	Medium
Hybrid SVPWM [21]	Medium	Medium	High	Medium
SVPWM [26]	Medium	High	High	High
SVPWM [27–29]	High	High	High	Medium
SHE [30]	High	Medium	Low	Low

Table 4 Simulation parameters

Parameter	Value
DC-link voltage	V_{DC} = 460 V
Upper/Lower DC-link capacitor	$C_1 = C_2$ =1200 μF
Flying capacitor	C_{fc} = 560 μF
Line frequency	f = 50 Hz
Switching frequency	f_s = 5 KHz
Load	R = 20 Ω, L = 2 mH

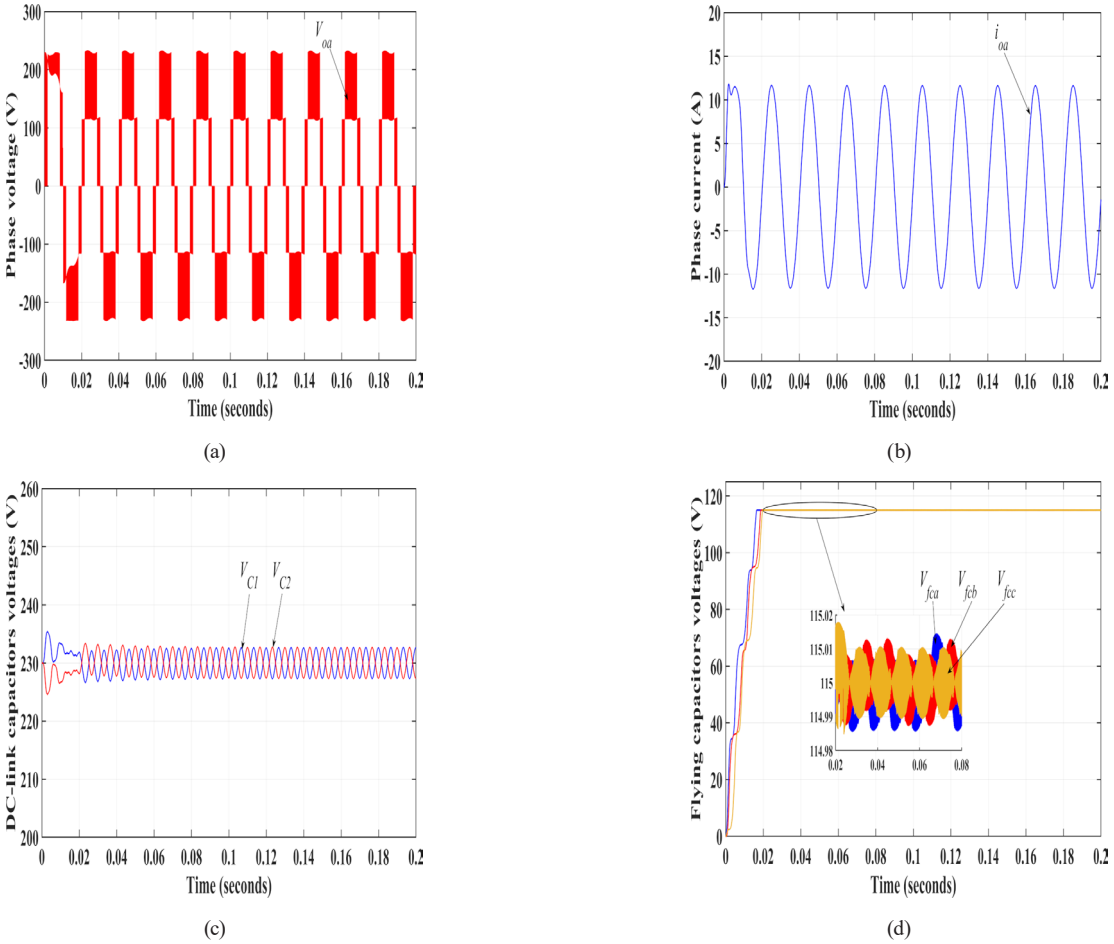


Fig. 5 Simulation result of: (a) phase voltage, (b) phase current, (c) DC-link capacitor voltages, (d) flying capacitor voltages

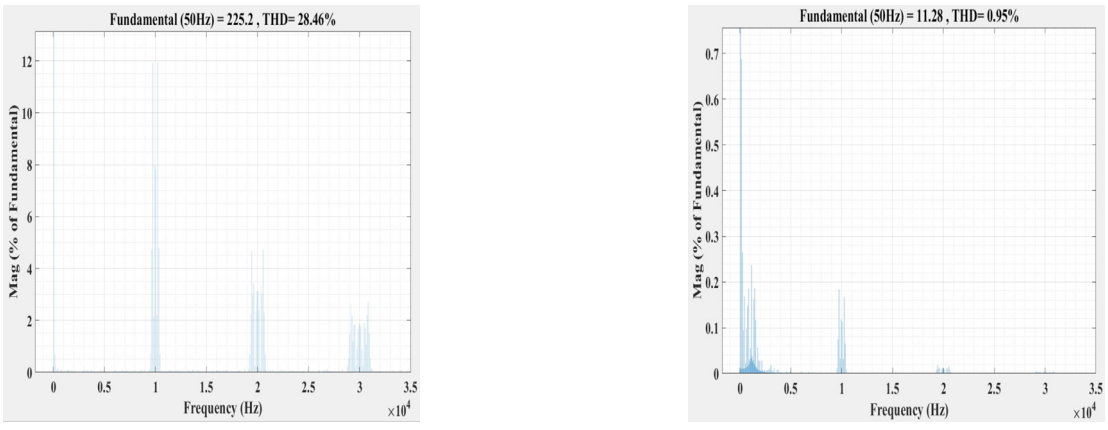
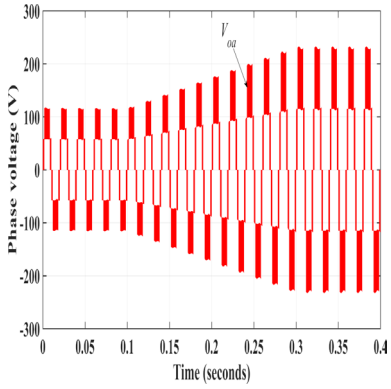


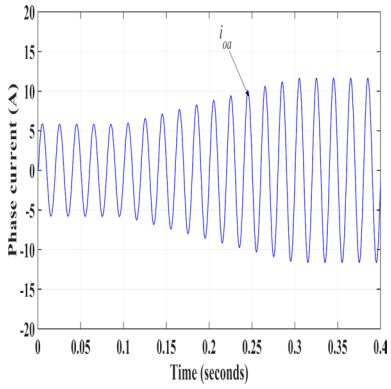
Fig. 6 Harmonic spectrums of: (a) phase voltage, (b) phase current

0.1 s from 230 V to 460 V. Fig. 7 (a) and (b), display high quality waveforms of the phase voltage and phase current respectively. Fig. 7 (c), shows that the DC-link capacitors voltages C_1 and C_2 are naturally balanced during the disturbance, the capacitances voltages are balanced at the desired operation value at 230 V. From Fig. 7 (d), it can be observed that the flying capacitors voltages charge and regulate at their reference value which is 115 V at 0.1 s. The proposed control method exhibits a fast dynamic response during the perturbation, enabling rapid charging of the FCs and restricting their voltage fluctuations.

The same test, as previously, was carried out considering a negative variation of the DC bus voltage in the present case. The input voltage V_{DC} changes at time 0.1 s from



(a)



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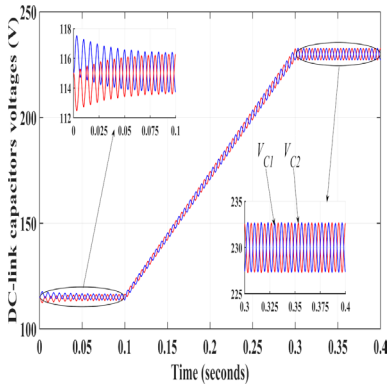
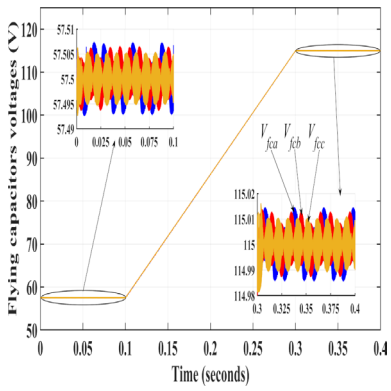
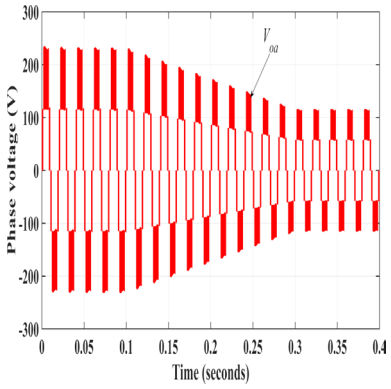


(c)

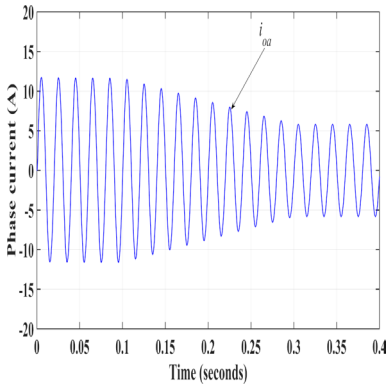


(d)

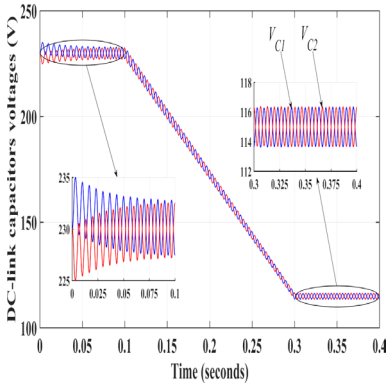
Fig. 7 Simulation result of transient dynamics when V_{DC} changes from 230 V to 460 V of: (a) phase voltage, (b) phase current, (c) DC-link capacitor voltages, (d) flying capacitor voltages



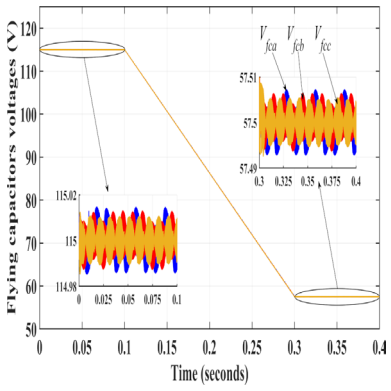
(a)



(b)



(c)



(d)

Fig. 8 Simulation result of transient dynamics when V_{DC} changes from 460 V to 230 V of: (a) phase voltage, (b) phase current, (c) DC-link capacitor voltages, (d) flying capacitor voltages

460 V to 230 V. Fig. 8 shows the transient dynamics of the different voltages. We can also see in this case and note the following observations:

- Fig. 8 (a) and (b), show the high quality waveforms of the phase voltage and phase current respectively.
- Fig. 8 (c) shows that the DC-link capacitors voltages C_1 and C_2 are naturally balanced during the disturbance. The convergence is perfectly ensured.
- From Fig. 8 (d), we can observe that the proposed control method makes the FCs discharge fastly and restricts their voltage fluctuation.

A final test was carried out to verify the relevance of the control method. It consisted in varying the modulation index at different times during the operating process.

In Fig. 9, we can see the variation of modulation index: m = 0.5, 0.75 and 1, at times 0 s, 0.3 s and 0.6 s respectively.

This method ensures the stability of the system and allows us to satisfy the same objectives with a better-quality output voltage and out pout current with smaller filter inductance. The floating capacitors voltages remain well balanced in all operation modes.

Two of the most frequent modulation schemes for multilevel converters are PD-PWM and PS-PWM [31]. In order to compare the performances of the 5L-ANPC inverter with the proposed control method based PS-PWM and PD-PWM. A simulation was made with the same parameters, the results are summarized in Table 5.

The total harmonic distortion (THD) of the phase voltage is nearly equal for the proposed method based PS-PWM and PD-PWM under different modulation index. However, in the line voltage, the proposed method-based PD-PWM exhibits much better harmonic performance. This is because the PD-PWM line voltage increases and decreases gradually in voltage levels, whereas the PS-PWM line voltage increases and decreases two levels successively in many zones as shown in Fig. 10.

Fig. 11 (a) shows that the switches (S_{x3}, S_{x4}) and $\left(S_{x3}^{'}, S_{x4}^{'}\right)$ have equal switching frequency and equal losses under PS-PWM strategy due to the phase shift of

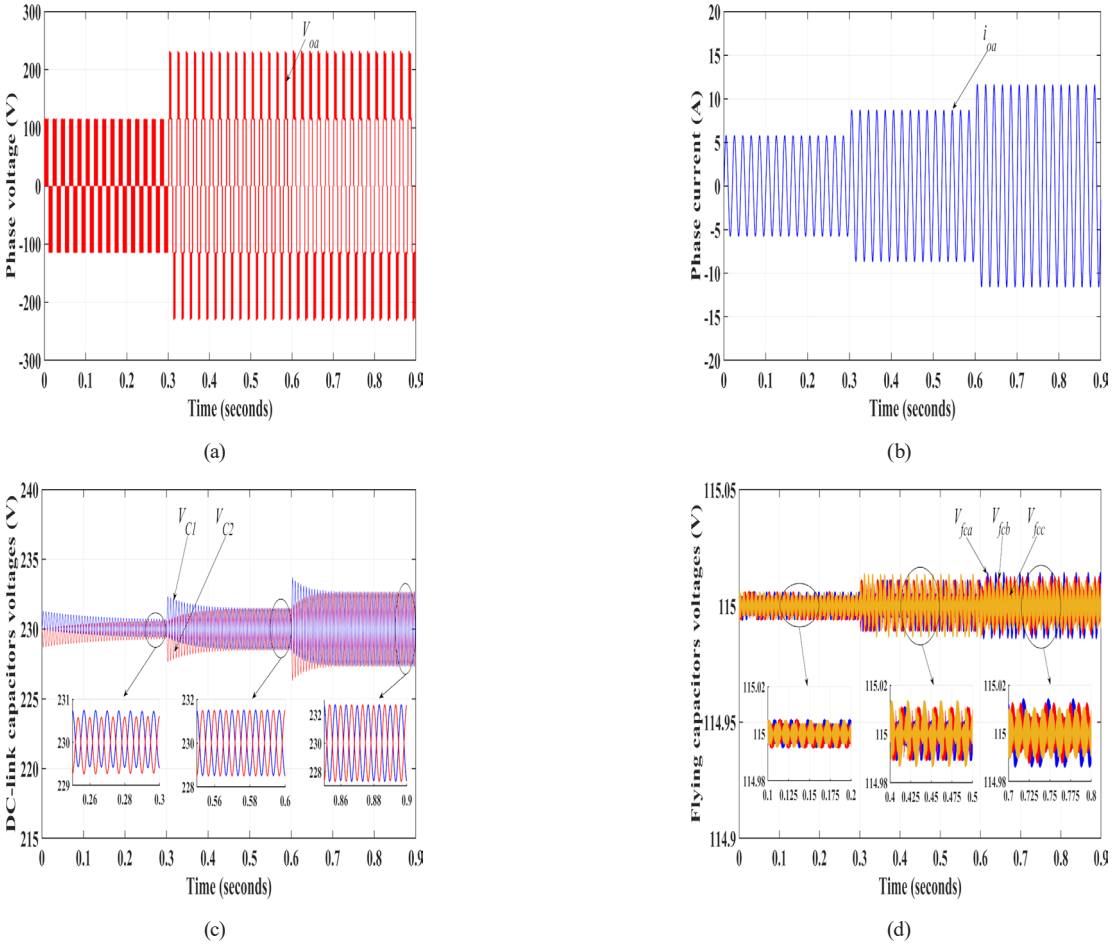
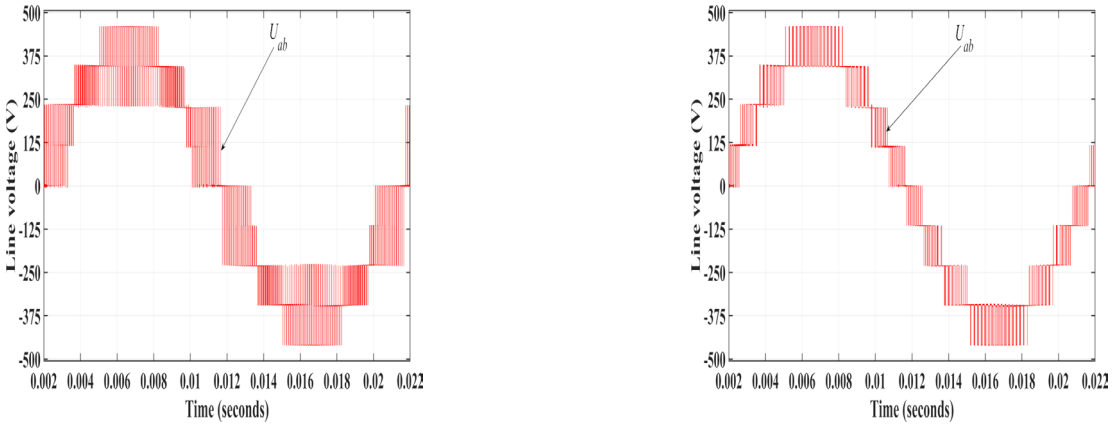


Fig. 9 Simulation result under different modulation indexes m = 0.5, 0.75, 1 of: (a) phase voltage, (b) phase current, (c) DC-link capacitor voltages, (d) flying capacitor voltages

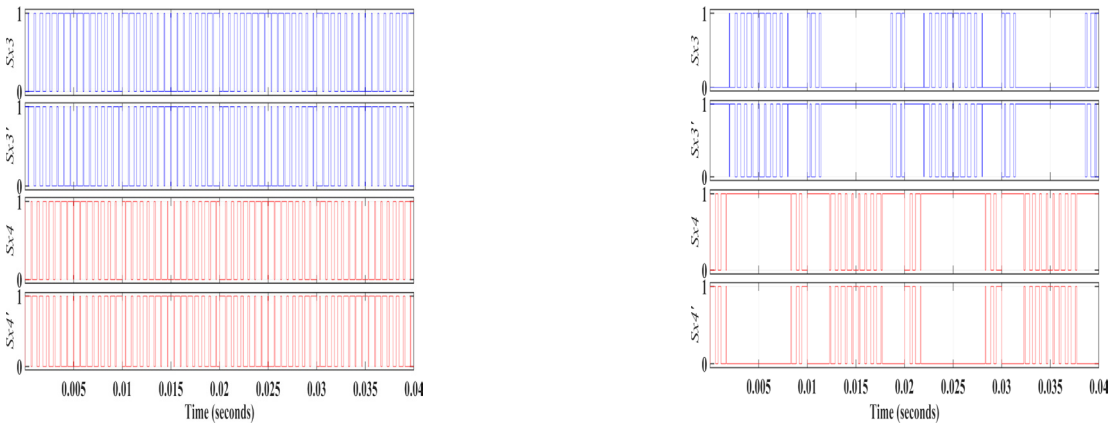
Table 5 Performance of the proposed method-based PS-PWM and PD-PWM

Modulation index	Proposed method-based PS-PWM		Proposed-method based PD-PWM	
	Phase voltage THD (%)	Line voltage THD (%)	Phase voltage THD (%)	Line voltage THD (%)
0.1	233.51	221.44	232.39	164.05
0.2	148.33	138.49	148	91.73
0.3	106.22	96.89	105.97	49.31
0.4	77.14	67.29	77	42.06
0.5	52.57	40.24	52.34	35.36
0.6	44.53	25.82	44.41	25.56
0.7	41.88	28.04	41.8	24.24
0.8	38.42	29.69	38.3	21.71
0.9	33.53	28.71	33.47	17.41
1	28.46	25.66	26.95	17.08



(a) (b)

Fig. 10 Line voltage U_{ab} under (a) PS-PWM, (b) PD-PWM



(a) (b)

Fig. 11 Switching pulses of switches S_{x3}, S'_{x3}, S_{x4}, S'_{x4} under (a) PS-PWM, (b) PD-PWM

the carriers in the angle. Unlike PD-PWM, where the switching frequency of the switches is unequal as shown in Fig. 11 (b), which means unequal conduction time and unequal losses. Because the carrier's magnitude is shifted. Since the second cell is like to a three level FC converter. Therefore, is suitable to use PS-PWM modulation in order to balance the losses in the four switches.

5 Conclusion

The 5L-ANPC converter is an attractive multilevel topology that has gained attention from both industry and academics. The notable drawback of this topology is the unbalanced voltages of the flying capacitors. To overcome this problem, this paper proposes a simple control strategy to regulate the flying capacitor voltages and generate the required output voltage levels with high performance. Simulation results demonstrate that the proposed control method effectively enhances the performance of the 5L-APNC converter by regulating the flying capacitor voltages at their reference value while also generating correctly at the output side the same voltage levels as the staircase reference voltage. This control approach facilitates rapid charging and discharging of the flying capacitors while minimizing their voltage fluctuations. Moreover, it ensures the stability of the 5L-ANPC converter during perturbations such as variations of modulation index and input voltage. This control technique exhibits fast execution time due to its simple equations and reduced number of calculations. Consequently, ANPC multilevel converters can be used for applications involving renewable energy and motor drives.

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