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Fault-resilient Control Strategy for Cascaded Multilevel Inverters in Grid-connected PV Systems

Sabrina Nacef[1*], Rabah Babouri[1], Kaci Ghedamsi[1], Azzedine Houari[2]

[1] Université de Bejaia, Faculté de Technologie, Laboratoire de Maîtrise des Énergies Renouvelables (LMER), 06000 Bejaia, Algeria
[2] Institut de Recherche en Energie Electrique de Nantes (IREENA), Nantes Université, 37, boulevard de l'université, 44600 Saint Nazaire, France
[*] Corresponding author, e-mail: Sabrina.nacef@univ-bejaia.dz

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Abstract

This paper presents a fault-tolerant control strategy for a three-phase, seven-level Cascaded Multilevel Inverter (CMI) in grid-connected photovoltaic (PV) systems. The proposed approach enhances state-of-the-art CMI fault-tolerant control by integrating advanced compensation techniques, combining fault isolation and compensation, and conducting a comprehensive system analysis under fault conditions. The study focuses on improving power quality and system robustness, making it particularly suitable for modern grid-tied renewable energy applications. Compared to previous works, this research offers notable advances in power quality, system reliability, and fault resilience. Key innovations include optimizing the use of renewable energy in large-scale solar installations through multilevel inverter technology and addressing operational faults to ensure uninterrupted power delivery. The findings underscore the significance of robust fault-tolerant strategies in improving the performance and stability of renewable energy systems.

Keywords

fault-resilient, multilevel inverters, cascade h-bridge, grid-tied inverters, PV systems, renewable energy

1 Introduction

In 2024, the growth of global electricity generation continued to slow down, largely due to ongoing economic pressures and disruptions in energy markets [1]. Despite this, renewable energy sources like wind and solar kept growing, making up a larger share of the global energy mix [2]. Solar power, in particular, saw strong growth, thanks to falling costs, supportive policies, and the worldwide push to reduce carbon emissions [2, 3]. Wind power also saw significant gains, powered by advancements in technology [2]. Together, wind and solar overtook nuclear power as a major source of electricity generation [1].

By 2024, renewable energy capacity continued to expand, driven by increasing investments in wind and solar [2]. These renewables accounted for most of the new power added, further highlighting their growing importance in reducing reliance on fossil fuels and meeting global sustainability goals [2–4]. The ongoing rise of renewables is proving just how competitive these technologies have become in the global energy market [3].

Solar power plants are a very important source of electricity. It is an inexhaustible resource, providing a reliable source of energy without depleting natural resources. Does not produce greenhouse gases or air pollutants, helping to clean up the environment and reduce climate change [5]. Recent advances have significantly reduced the cost of solar panels and installation, making solar energy increasingly affordable and accessible for residential, commercial, and community applications [6]. Solar panels require minimal maintenance and have a long lifespan, providing a reliable source of electricity with minimal upkeep. By generating electricity on-site using solar panels, individuals and organizations can reduce their reliance on the conventional grid and potentially reduce their energy costs [7].

Photovoltaic (PV) modules convert solar energy into electrical energy, using interconnected PV cells to provide practical voltage and current, and protect the cells. Recently, control of PV systems has gained significant attention, with two main objectives emerging: maximizing power output through maximum power point tracking (MPPT) and utilizing PV power to meet load demand or inject into the electrical grid [8, 9].

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In order to effectively harness and integrate the increasing energy capacity derived from solar power; grid-tied inverters prove to be of crucial importance. A grid-tied inverter represents a key component in the process of converting direct current (DC) generated by PV panels into alternating current (AC), which is compatible with the electrical grid. This conversion is of critical importance, given that the majority of electrical grids operate on alternating current power. In contrast to off-grid systems, whose energy storage is dependent on batteries [10, 11], grid-tied inverters facilitate the seamless integration of renewable energy into the grid. This optimizes the use of solar power while ensuring grid stability and reliability [12].

Among the various types of grid-tied inverters, multilevel inverters (MIs) have emerged as an innovative solution to produce a smoother output waveform, reducing harmonic distortion and improving overall power quality [13]. The ability of multilevel inverters to provide higher voltage outputs with lower switching losses makes them particularly advantageous for large-scale solar installations.

The MIs offers several advantages over a conventional two-level inverter such as: The generation of output voltages with minimal distortion and lower voltage variation, drawing of input current with minimal distortion, generation of smaller common mode (CM) voltages and the ability to operate with a lower switching frequency [14].

Among the various types of multilevel inverters, the cascaded H-bridge (CHB) [15] is another notable topology. It consists of multiple H-bridge inverters connected in series, offering a promising solution for a number of applications. This configuration allows for modular design, scalability, and high efficiency. It is particularly well-suited for large-scale solar power plants, where higher voltage levels are required to interface directly with the grid without the need for bulky transformers. However, due to their complex structures, these inverters are also susceptible to various operational faults. It is therefore essential to address such faults in order to maintain the efficiency and reliability of both the inverter and the grid.

Over the past decade, significant advancements have been made in the field of fault-tolerant multilevel inverters Starting with fault-tolerant reconfiguration techniques introduced in early works, such as in [16] on asymmetric multilevel converters, the focus was on maintaining operational continuity even in the face of faults. This foundational research laid the groundwork for subsequent studies that emphasized modularity and redundancy. As seen in [17], the author proposed a control strategy allowing $N + 1$ redundancy in Cascaded H-Bridge converters. The emphasis on redundancy reflects a growing recognition of the need for reliability in applications where uninterrupted power is critical, such as in hospitals and renewable energy systems. Also, in [18] a modified space vector modulation (SVM) technique further advanced this area by presenting a method to sustain balanced output voltages despite faults was presented. This work, along with the [19, 20] authors investigate into the operation of Cascaded H-Bridge converters in photovoltaic systems, underscored the importance of robust control strategies that can adapt to various fault scenarios while ensuring consistent power delivery to the grid. In [21], an expanded scope was added by addressing reliability in quasi-Z-source inverters and proposing a novel control algorithm for enhancing post-fault performance. The emphasis on renewable energy applications reflects a growing trend toward integrating fault-tolerant capabilities in systems that connect to the grid, ensuring a stable energy supply even during component failures. In subsequent works, including [22, 23], designs of fault-tolerant topologies have focused on simplifying implementations and reducing the component count without compromising reliability. These designs emphasize the need for cost-effective solutions, addressing the economic concerns associated with traditional fault-tolerant approaches that often require complex control schemes and additional hardware. Additionally, authors in [24] introduced the X-CHB inverter design, which incorporates self-voltage balancing, and the authors in [25] presented Kalman filter-based fault diagnosis for H6 inverters. These efforts represent the culmination of advancements, demonstrating how advanced algorithms and hybrid configurations can effectively tackle reliability challenges in high-power applications.

The more recent studies [26] have consolidated these advancements by investigating reduced-device multilevel inverters and their fault-tolerant capabilities, specifically for aviation applications. This reflects a growing interest in optimizing inverter performance for critical systems. These studies reiterate the central theme of maintaining operational performance under fault conditions, whether in aircraft or renewable energy contexts, thus reinforcing the necessity for reliable inverter technologies.

While significant progress has been made in fault-tolerant control strategies for multilevel inverters, gaps remain, especially for grid-connected PV systems. Previous studies [16–18] have focused on fault reconfiguration and redundancy, but often lack integrated approaches that combine fault isolation and compensation. Many solutions still

address specific inverter types or fault scenarios without considering the complexities of real-world, large-scale PV systems. Additionally, while research on cascaded multilevel inverters (CMIs) has been explored [19–21], there is a need for more comprehensive strategies that ensure both fault tolerance and consistent power delivery to the grid.

This study aims to address these gaps by proposing a fault-tolerant control strategy for a three-phase, seven-level CMI in grid-connected PV systems. By integrating fault isolation with compensation techniques, this approach offers a more robust solution to enhance system stability, reliability, and power quality in renewable energy applications.

This paper is structured as follows: Section I provides an overview of the system description; Section II describes the system; Section III focuses on the system modeling and the control strategies; Section IV presents simulation results to validate the control methods; and finally, the concluding section summarizes the findings.

2 Systeme description

Fig. 1 depicts a PV plant connected to the grid with a multilevel inverter. The structure of the inverters composed of a three-phase cascade multilevel inverter with n submodules (SM) each SM is composed of an H half bridge with different DC buses.

Each PV plant used is identical and provides the same voltage, which is elevated using a DC/DC converter to a higher voltage value; the system operates at the maximum power point of the PV array due to the use of a P&O (perturb and observe) MPPT algorithm to maximize energy production.

3 System modeling

3.1 Cascade multilevel inverter modeling

Fig. 2 shows the structure of an N-level cascade multilevel inverter. It consists of three arms, each of which has N identical SMs connected in series.

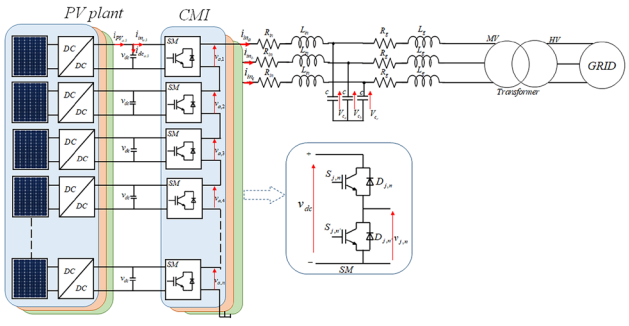

Fig. 1 Grid-tied PV system

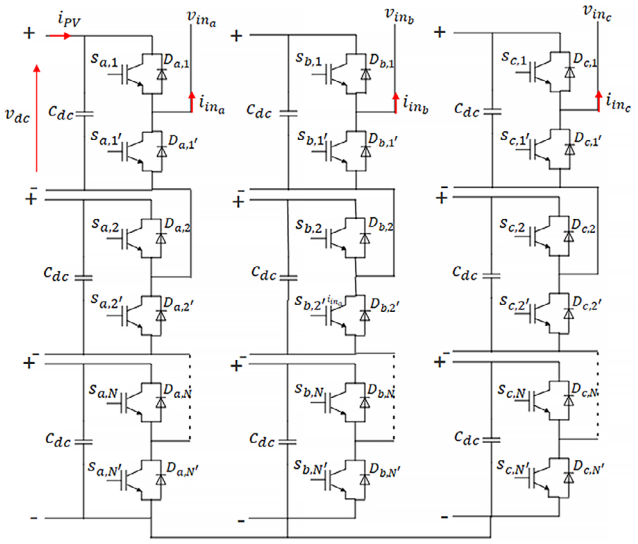

Fig. 2 N-level cascade multilevel inverter

Each SM includes a half-bridge; a DC capacitor and two IGBTs with antiparallel diodes. These allow the output voltage of the SM to be set to either zero or to $\pm V_{dc}$ as shown in Table 1.

A three-phase multilevel inverter with N sub-modules in each arm produces a voltage waveform of $N - 1$ Levels. The sum of the voltages of each SM in each phase is always equal to the DC bus voltage v_{dc}, and the number of active SMs in each phase is equal to N. Thus, the three-phase inverter instantaneous voltage can be represented:

$$v_{in,j} = n \cdot \sum_{1}^{N} v_{dc,j}. \tag{1}$$

n is the insertion indices of the inverter where $n = 0$ means that all sub-modules in the arm are bypassed, on the other side $n = 1$ means that all the sub-modules in the arm are inserted. It can be calculated from the modulation technique.

$\sum_{1}^{N} v_{dc}$ represents, the total capacitor voltage and N represent the number of SM.

The relation between the PV current, the inverter current and the DC bus current can be given by:

$$i_{PV,j} = i_{in,j} + i_{dc,j}. \tag{2}$$

Table 1 Different states of a SM

S_j,N	S_j,N'	D_j,N	D_j,N'	Current	Output voltage
1	0	0	0	$i_{in} < 0$	v_{dc}
0	1	0	0	$i_{in} > 0$	0
0	0	1	0	$i_{in} > 0$	$-v_{dc}$
0	0	0	1	$i_{in} < 0$	0

The total current of the DC bus side is given by Eq. (3):

$$i_{dc,j} = C_{dc,j} \cdot \frac{d\left(\sum_1^N v_{dc,j}\right)}{dt}, \tag{3}$$

where $C_{dc,j}$ is the applicable capacity of active SM per arm.

From Eqs. (2) and (3) the output current of the inverter can be expressed by:

$$i_{in,j} = i_{PV,j} - C_{dc,j} \cdot \frac{d\left(\sum_1^N v_{dc,j}\right)}{dt}, \tag{4}$$

where the index j represents the phase ($j = a, b, c$)

By applying Kirchhoff's law on the output of the inverter in Fig. 1 we find:

$$V_{in,j} - V_{c,j} = L_{in} \frac{di_{in,j}}{dt} + R_{in} \cdot i_{in,j}, \tag{5}$$

where, L_{in}, R_{in} and $V_{c,j}$ are the inductance the resistance, and the capacity voltage of the LC filter used in the system to reduce the voltage ripple.

Replacing the value of $V_{in,j}$ from Eq. (1) in Eq. (5) we will find:

$$\frac{di_{in,j}}{dt} = -\frac{R_{in}}{L_{in}} \cdot i_{in,j} + \frac{n}{L_{in}} \sum_1^N v_{dc,j} - \frac{V_{c,j}}{L_{in}}. \tag{6}$$

Using the expression of the output current found in 7 we will have:

$$\frac{d\left(\sum_1^N v_{dc,j}\right)}{dt} = -\frac{1}{C_{dc,j}} i_{in,j} + \frac{1}{C_{dc,j}} i_{PV,j}. \tag{7}$$

Using Eqs. (6) and (7) we obtain a continuous model of a phase j in Eq. (8):

$$\begin{bmatrix} \frac{di_{in,j}}{dt} \\ \frac{d\left(\sum_1^N v_{dc,j}\right)}{dt} \end{bmatrix} = \begin{bmatrix} -\frac{R_{in}}{L_{in}} & \frac{n}{L_{in}} \\ -\frac{1}{C_{dc,j}} & 0 \end{bmatrix} \begin{bmatrix} i_{in,j} \\ \sum_1^N v_{dc,j} \end{bmatrix} + \begin{bmatrix} -\frac{V_{c,j}}{L_{in}} \\ \frac{i_{PV,j}}{C_{dc,j}} \end{bmatrix}. \tag{8}$$

3.2 Control strategy

3.2.1 Faultless mode

The control strategy used in the system is shown in Fig. 3, it's based on two controller loops, the current loop controller and the voltage loop controller.

The current loop controller controls the output current of the inverter. The voltage loop feeds the current references to the inner loop in order to maintain adequate voltage references for the CMI and it controls the output voltage of the capacitor filter used.

- Current control loop

By applying Kirchhoff's voltage law in Fig. 3, the relationship between the output current i_{in}, the output voltage of the converter AC side v_{in} and the voltage of the capacitor filter v_c, is:

$$v_{in} - v_c = L_{in} \frac{di_{in}}{dt} + R_{in} \cdot i_{in}. \tag{9}$$

Considering a balanced three-phase system, the equation above is transformed into a rotating $dq0$ reference frame, using the Park-Clarke transformation, in steady state:

$$\left\{ \begin{array}{l} v_d - v_{cd} = R_{in} i_d + w L_{in} i_q \\ v_q - v_{cq} = R_{in} i_q + w L_{in} i_d \end{array} \right\}. \tag{10}$$

The vector-current control is usually used on variable speed drives as illustrated in [27]. Another approach detailed in [28] is the deadbeat-current control design, based on this, Eq. (10) become:

$$\left\{ \begin{array}{l} v_d = L_{in} \frac{di_d}{dt} + R_{in} i_d + w L_{in} i_q + v_{cd} \\ v_q = L_{in} \frac{di_q}{dt} + R_{in} i_q - w L_{in} i_d + v_{cq} \end{array} \right\}, \tag{11}$$

where w is the angular frequency, L_{in} is the filter inductance and R_{in} is the filter resistance of the system. In high voltage, the resistance is usually neglected [29]. Therefore, the approximation of v decoupled components are:

$$\left\{ \begin{array}{l} v_d = L_{in} \frac{di_d}{dt} + w L_{in} i_q + v_{cd} \\ v_q = L_{in} \frac{di_q}{dt} - w L_{in} i_d + v_{cq} \end{array} \right\}. \tag{12}$$

The inverter's output current can be controlled by two internal loops using PI controllers to convert the current errors into voltage signals. The structure of the current control loop is illustrated in Fig. 4.

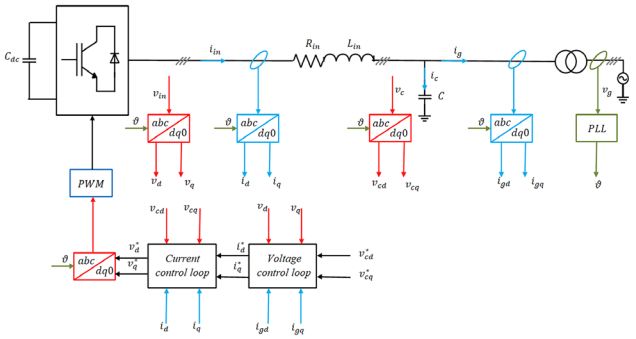

Fig. 3 Control strategy of the CMI

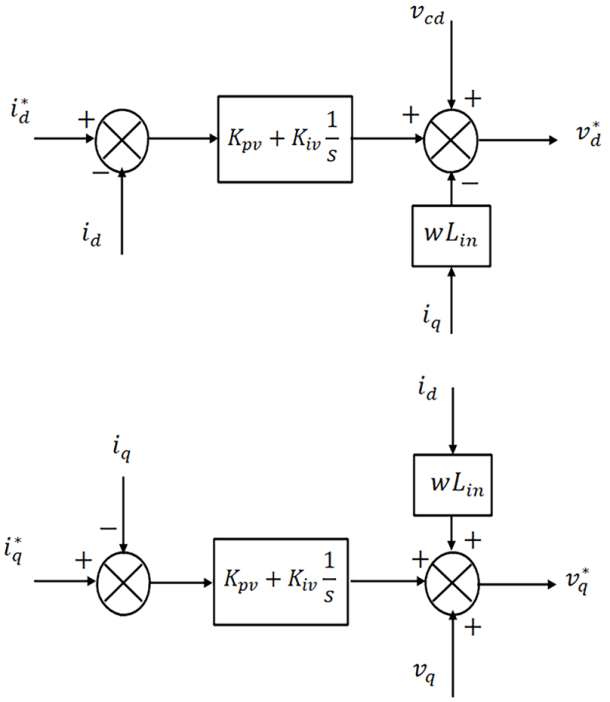

Fig. 4 Current control loop

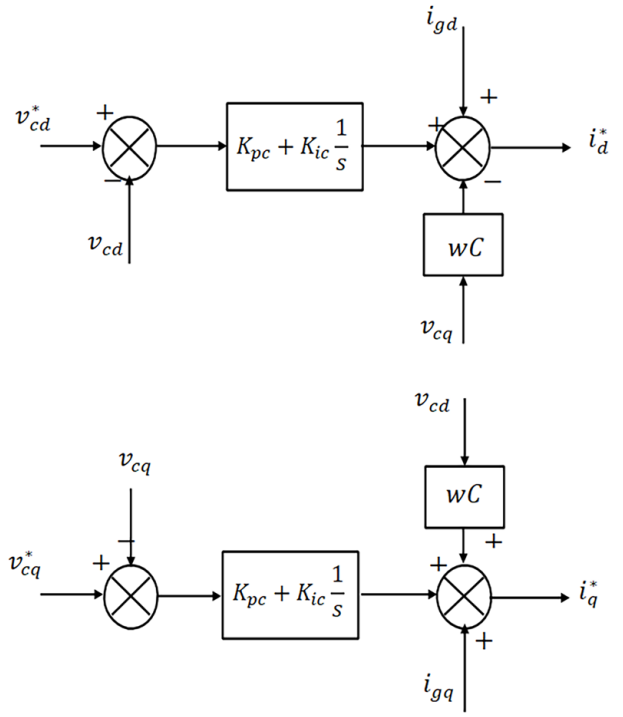

Fig. 5 Voltage control loop

$$\left\{\begin{array}{l} v_d^* = \left[i_d^* - i_d\right]\left[K_{pv} + K_{iv}\dfrac{1}{s}\right] + v_{cd} + wL_{in}i_q \\ v_q^* = \left[i_q^* - i_q\right]\left[K_{pv} + K_{iv}\dfrac{1}{s}\right] + v_{cq} + wL_{in}i_d \end{array}\right\}. \tag{13}$$

- Voltage control loop

By applying the Kirchhoff's current law in Fig. 3 we found:

$$i_{in} = i_c + i_g, \tag{14}$$

where is the filter capacitor current expressed by:

$$i_c = C\frac{dv_c}{dt}. \tag{15}$$

Replacing Eq. (15) in Eq. (14) we'll have:

$$i_{in} = C\frac{dv_c}{dt} + i_g. \tag{16}$$

Eq. (16) then transformed into a rotating $dq0$ reference frame, using the Park-Clarke transformation, in steady state:

$$\left\{\begin{array}{l} i_d = C\dfrac{dv_{cd}}{dt} + wCv_q + i_{gd} \\ i_q = C\dfrac{dv_{cq}}{dt} - wCv_d + i_{gq} \end{array}\right\}. \tag{17}$$

Using PI controllers to convert the voltage errors into current signals. The structure of the voltage control loop is illustrated in Fig. 5.

$$\left\{\begin{array}{l} i_d^* = \left[v_{cd}^* - v_{cd}\right]\left[K_p + K_i\dfrac{1}{s}\right] + i_{gd} - wCv_q \\ i_q^* = \left[v_{cq}^* - v_{cq}\right]\left[K_{pc} + K_{ic}\dfrac{1}{s}\right] + i_{gq} + wCv_d \end{array}\right\}. \tag{18}$$

The output voltage of the inverter is aligned with the d axis ($V_{cq}^* = 0$).

3.2.2 Under fault

CMI inverters use a significant number of semiconductors switching devices, commonly MOSFETs or IGBTs. As a result, the probability of failures in such semiconductors will increase. Specifically, an open circuit switch fault manifests when a semiconductor switch's electrical continuity is compromised. This fault condition results in a reduction of both the output voltage and current.

These switch faults in CMI inverters can have a range of negative consequences, including power quality degradation, system disturbances, equipment downtime, and economic losses. So, when a fault occurs in a system, it should continue operating as it did before the fault, if possible. To achieve this, two main strategies are used: first the isolation and reconfiguration then the compensation.

- Isolation and reconfiguration

This method involves identifying and isolating the fault, and then modifying the system's structure to bypass the faulty SM.

If one of the SMs semiconductors fails, it will impact the current of the inverter, leading to decreased functionality and energy efficiency. The control process in place, which is sensitive to sudden current fluctuations, triggers the closure of switches as shown in Fig. 6. In this case, the affected sub-module will be isolated, allowing the inverter to continue operating in a quasi-normal mode with reduced efficiency. We must then implement a compensation algorithm, as explained below.

- Compensation

This method involves altering the control used in the normal mode to compensate for the effects of the fault.

Once the fault is isolated and the sub-module is reconfigured, the control system adjusts the *d* and *q* axis control voltages using the compensation voltages to minimize the impact of the fault as shown in Fig. 7.

$$\left\{\begin{matrix} v^*_{d\_c} = v^*_d - v_{d\_c} \\ v^*_{q\_c} = v^*_q - v_{q\_c} \end{matrix}\right\}. \tag{19}$$

By adjusting these voltages, the inverter can compensate for the loss of a sub-module and reduce the unwanted harmonics and homopolar components that arise from the fault.

- Fault conditions in the CMI and impact on voltage and current

In a three-phase inverter system, when a fault occurs in one of the inverter sub-modules, it leads to imbalanced voltage and current waveforms. This imbalance generates zero-sequence components in the system. The voltage Eqs. (10) and (11) of the *dq*0 axes then becomes:

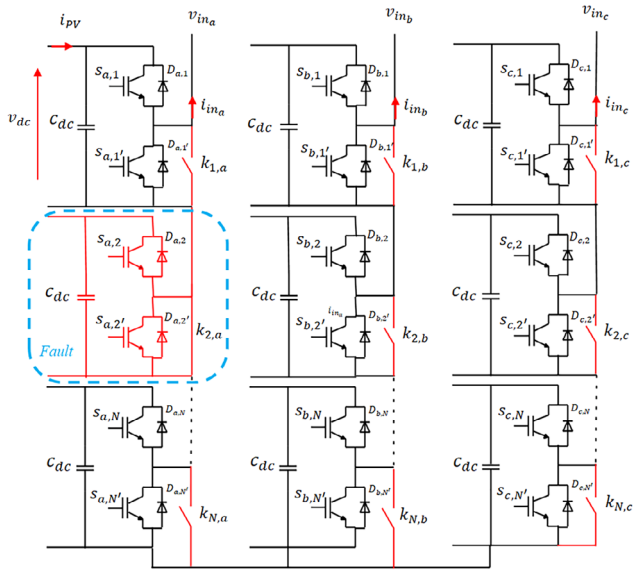

Fig. 6 CMI reconfiguration

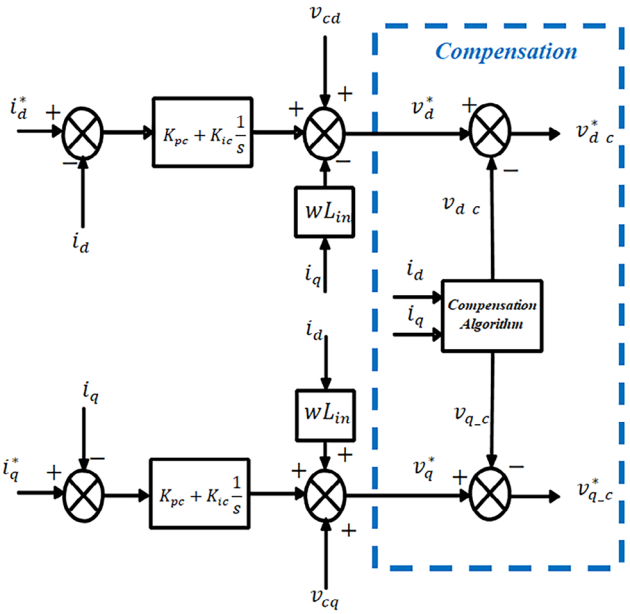

Fig. 7 Compensation algorithm

$$\left\{\begin{matrix} v_d - v_{cd} = R_{in} i_d + wL_{in} i_q + R_{in} i_0 \\ v_q - v_{cq} = R_{in} i_q + wL_{in} i_d + R_{in} i_0 \\ v_0 - v_{c0} = R_{in} i_0 \end{matrix}\right\}. \tag{20}$$

These equations lay the foundation for controlling the currents i_d, i_q and i_0 with corresponding voltage references, typically through PI control.

- Current control with PI controllers

To control the output currents, the system uses PI controllers to minimize the error between the actual and desired currents. The controllers adjust the voltage references V^*_d, V^*_q and V^*_0 based on the current error.

The PI controller equations are:

$$\left\{\begin{matrix} v^*_d = \left[i^*_d - i_d\right]\left[K_{pv} + K_{iv}\frac{1}{s}\right] + v_{cd} + wL_{in} i_q + R_{in} i_0 \\ v^*_q = \left[i^*_q - i_q\right]\left[K_{pv} + K_{iv}\frac{1}{s}\right] + v_{cq} - wL_{in} i_d + R_{in} i_0 \\ v^*_0 = \left[i^*_0 - i_0\right]\left[K_{pv} + K_{iv}\frac{1}{s}\right] + v_{c0} \end{matrix}\right\}. \tag{21}$$

- Butterworth filter for harmonic mitigation

To mitigate unwanted harmonics, particularly zero-sequence components and other high-frequency components caused by faults, we use a Butterworth filter. The Butterworth filter is designed to attenuate harmonics without introducing significant phase shift in the passband, which is critical for the stability of the system.

the Butterworth filter depends on its order and its form factor and is defined as:

$$G(\omega)=\left|H(j\omega)\right|=\frac{1}{\sqrt{1+\varepsilon^{2}\left(\frac{\omega_a}{\omega_p}\right)^{2m}}}, \tag{22}$$

the filter order and the form factor are given by:

$$m\geq\frac{A_a-A_p}{20\left(\log(\omega_a)-\log(\omega_p)\right)}, \tag{23}$$

$$\varepsilon=\sqrt{10^{\frac{A_p}{10}}-1}, \tag{24}$$

where ω_p, ω_a, A_p and A_a represent the angular frequencies and amplitudes of the passband and cut-off band, respectively.

The transfer function $H(p)$ of the Butterworth filter has the form:

$$H(p)=\prod_{k=1}^{m}\frac{1}{\left(1-\frac{P}{z_k}\right)}. \tag{25}$$

With z_k the roots with negative real parts expressed by:

$$1+(-1)^{m}\varepsilon^{2}z^{2m}=0. \tag{26}$$

If the filter order is pair, then:

$$z_k=\varepsilon^{\frac{-1}{m}}e^{i\frac{\pi(1+2k)}{2m}}. \tag{27}$$

If the filter order is impair, then:

$$z_k=\varepsilon^{\frac{-1}{m}}e^{i\frac{k\pi}{m}}. \tag{28}$$

- Compensation block for *d* and *q* axis control

To include the effect of the Butterworth filter in the for *d* and *q* axis control, we introduce additional compensation terms. These terms adjust the voltage references by subtracting the filtered harmonic components.

The compensation terms are:

$$\begin{Bmatrix} v_{d\_c}=R_{in}(i_d-i_d\left[H(p)\right]) \\ v_{q\_c}=R_{in}(i_q-i_q\left[H(p)\right]) \end{Bmatrix}, \tag{29}$$

where the filtered values $i_d[H(p)]$ and $i_q[H(p)]$ are the Butterworth-filtered currents and they are used to modify the reference voltages to suppress the zero-sequence components.

The parameters of the compensation filter used in this paper are described in Table 2.

Table 2 Filter parameters

Parameters	value
A_a	–90 dB
A_p	0 dB
ω_a	18850 rad/s
ω_p	75398 rad/s
Filter order	4
Filter transfer function	$\frac{6.0881}{s^4+4.1047\ s^3+8.424\ s^2\ 10.1279\ s+6.0881}$

4 Simulation results and interpretations

To validate the propose *d* control strategy, a simulation of a photovoltaic (PV) system connected to the grid through a three-phase seven-level Cascaded Multilevel Inverter (CMI) was developed using MATLAB/Simulink [30]. The parameters used in the simulation are detailed in Table 3. The Simulink block diagram of the studied PV system illustrates its operation under three different conditions: before the fault, during the fault, and after fault compensation.

The simulation employs the SimPowerSystems library to model the power system components, including the PV arrays, the three-phase seven-level CMI, a passive filter, and the grid transformer. The control system comprises current control, voltage control, a Phase-Locked Loop (PLL), and the proposed fault compensation controller.

To assess the impact of open-circuit faults in the inverter modules, two faults were intentionally introduced at different time intervals. The first fault occurred at 0.1 s, targeting the second module of the inverter. The *s* fault was triggered at 0.25 s in the seventh module of the inverter. At 0.4 s, the fault compensation control mechanism was activated to mitigate the adverse effects of the faults.

Fig. 8 illustrate a seven-level output voltage generated by CMI. In this instance, the inverter produces a phase-to-phase output voltage of 10 kV. This results in a high-quality

Table 3 Simulation parameters

Parameters	value
Maximum power plant $P_{\max}$	450 MW
DC bus voltage per module V_{dc}	1500 V
Fundamental frequency f	50 Hz
Filter inductance L_{in}	17.3 µH
Filter inductance L_g	10.4 µH
Filter resistance R_{in}	0.6 Ω
Filter resistance R_g	0.0348 Ω
Filter capacity C	596.83 µF

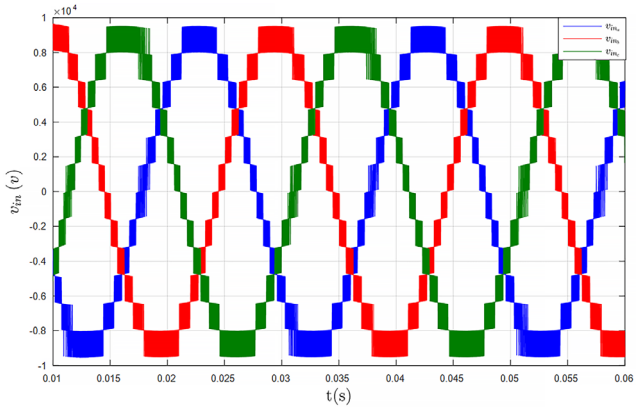

Fig. 8 Inverter output voltage

and balanced sinusoidal waveform. The ability of the CMI to achieve such a waveform with minimal distortion highlights its effectiveness in applications that require precise voltage control and harmonic reduction.

Fig. 9 presents the dynamic response of the PI controller under fault conditions. Before the fault, the system is stable, with the currents i_d and i_q closely following their reference values, indicating efficient control with minimal overshoot and a fast rise time.

At t = 0.1 s, when the fault occurs, there is a significant disturbance. The currents exhibit noticeable overshoot, particularly in i_q, which can be seen in the sharp peak immediately following the fault. The rise time also increases during this period, as the currents take longer to stabilize around their new values. Between t = 0.1 s and t = 0.4 s, oscillations in the currents highlight the instability and reduced performance of the controller in the presence of the fault.

After t = 0.4 s, the Butterworth filter is applied, which effectively reduces the oscillations and overshoot in the current waveforms. This action helps the system regain stability, as observed in the smooth settling of i_d and i_q.

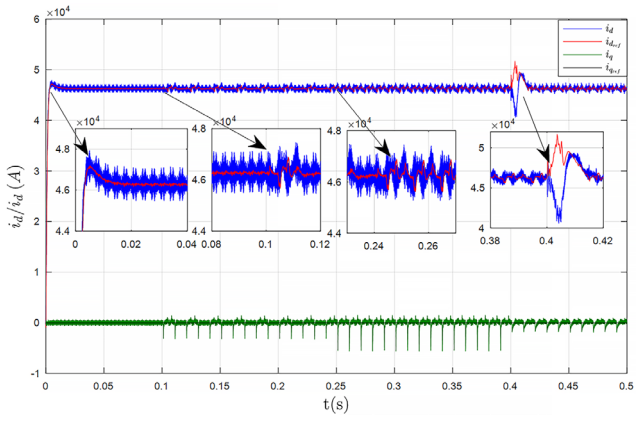

Fig. 9 Direct and quadratic inverter output current

The currents gradually return to tracking their reference values, with reduced rise time and overshoot, thereby restoring the dynamic performance of the PI controller.

Fig. 10 illustrates the instantaneous active and reactive power flow on the grid side and at the inverter output. It is evident that the instantaneous power from the inverter exhibits oscillations, primarily caused by harmonic distortion and switching transients. Additionally, during fault conditions, the power flow on the grid side was notably impacted, leading to increased oscillations. However, the implementation of the compensation system effectively mitigated these disturbances, reducing their impact on the grid power quality.

As illustrated in Figs. 11 and 12, the occurrence of the first fault caused a slight imbalance in both the grid current and voltage. Before the fault, the THD was 0.04%, as shown in Fig. 13 (a). This fault-induced disturbance resulted in notable waveform distortion, increasing the total harmonic distortion (THD) of the grid current to 2.83%, as shown in Fig. 13 (b). Although the fault did not immediately disrupt the overall stability of the system, the elevated THD indicates deterioration in waveform quality due to the module failure. The second open-circuit fault further exacerbated

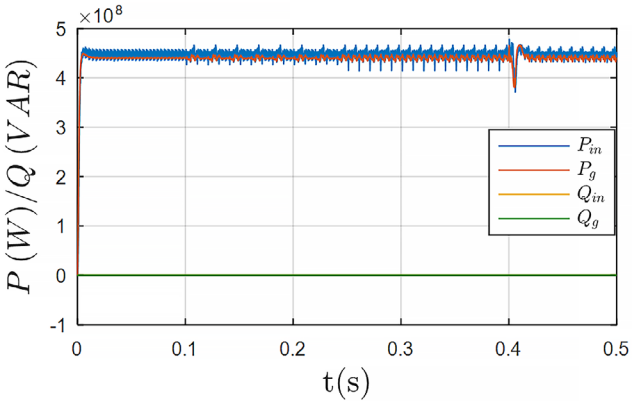

Fig. 10 Active and reactive power

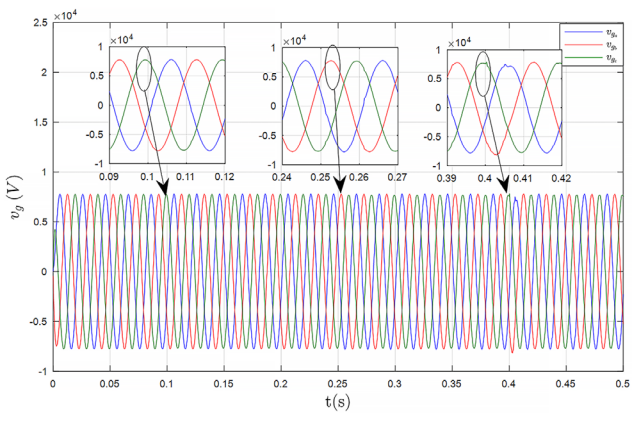

Fig. 11 Grid voltage

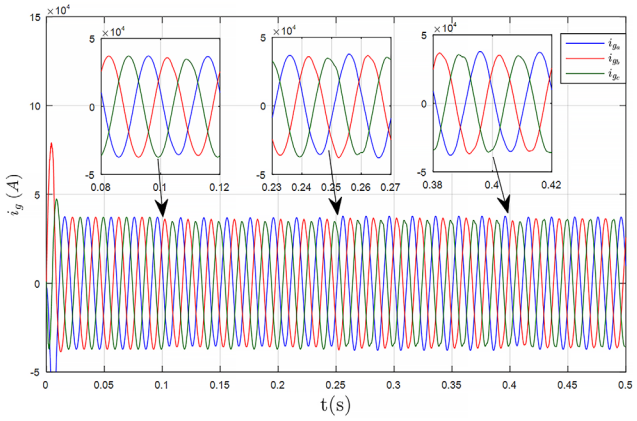

Fig. 12 Grid current

residual imbalance remained in the current due to the lasting impact of the faults, the compensation control significantly reduced the THD to 1.64%, as shown in Fig. 13 (d). This demonstrates the fault-tolerant control mechanism's capability to improve waveform quality and restore operational stability, ensuring the system's reliability under fault conditions.

5 Conclusions

The proposed fault-tolerant control strategy for a PV system using a three-phase, seven-level Cascaded Multilevel Inverter effectively improves system reliability and power

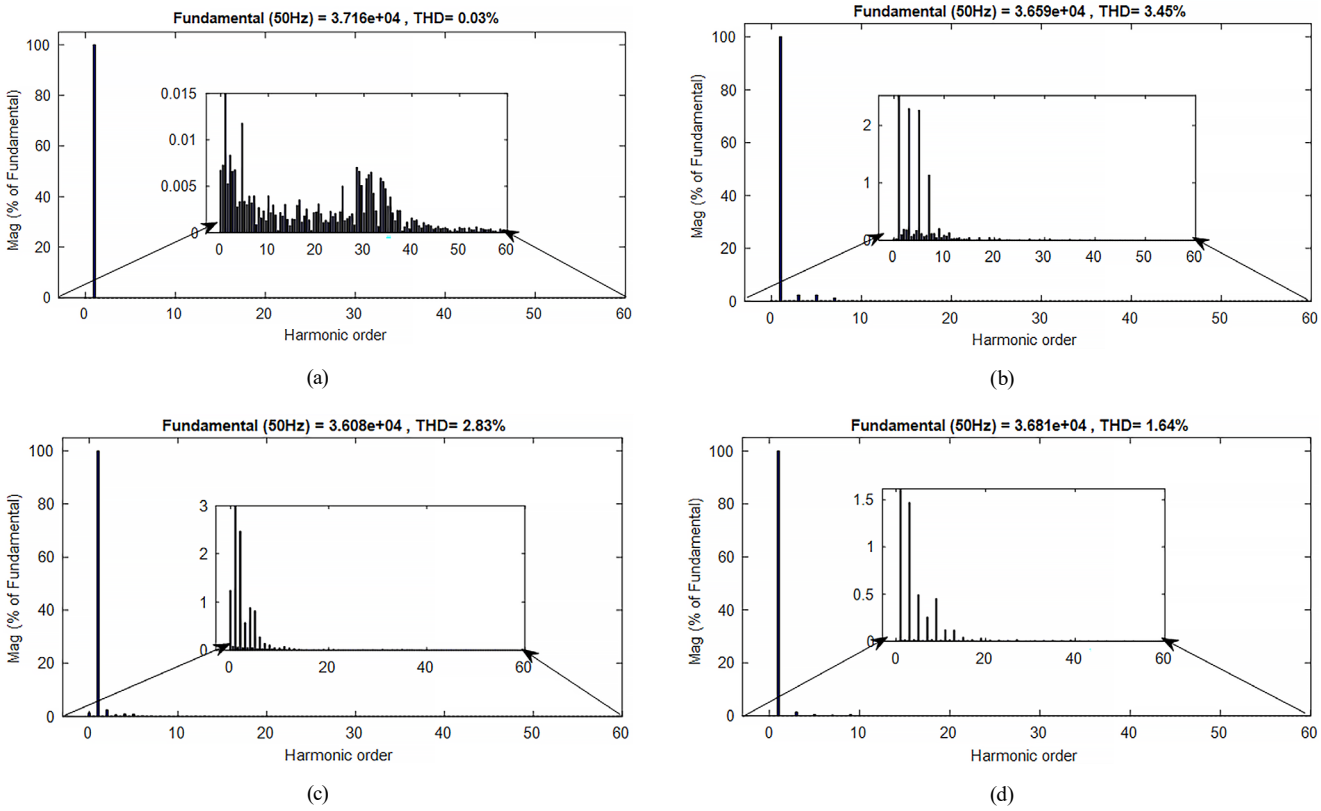

Fig. 13 Grid current THD (a) before faulted mode, (b) after first fault, (c) after second fault, (d) after compensation

the imbalance in grid parameters, leading to a significant increase in distortion and raisin g the THD to 3.45%, as depicted in Fig. 13 (c). This additional fault imposed greater stress on the inverter, impairing its ability to maintain the desired voltage and current regulation. The degradation of waveform integrity poses a considerable risk to system performance, particularly in grid-tied applications requiring low harmonic content and precise control. However, upon activating the compensation control mechanism to mitigate the effects of these faults, the strategy effectively restored the balance of the inverter's output voltage. While a slight

quality. The simulation results confirm that the CMI produces a high-quality sinusoidal output under normal conditions, with minimal harmonic distortion. When open-circuit faults were intentionally introduced into the system, the inverter's performance was adversely affected, leading to increased waveform distortion and imbalances in grid voltage and current.

The fault compensation mechanism was able to restore stability by adjusting the inverter's output and reducing harmonic distortions, demonstrating the system's capacity to recover from disturbances. The PI controller's response

showed resilience, but the addition of a Butterworth filter significantly enhanced the dynamic behavior during fault recovery, minimizing oscillations and restoring stable current regulation.

The analysis of instantaneous power flow revealed that harmonic distortions and switching transients contributed to power oscillations, particularly during fault conditions. The implementation of the fault-tolerant strategy effectively mitigated these disturbances, thereby improving the overall power quality and ensuring reliable operation of the grid-tied PV system. This approach underscores the potential of advanced control strategies to support the integration of renewable energy sources by enhancing the robustness and efficiency of inverter-based systems.

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