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RESEARCH ARTICLE

Compensation of Assembly Tolerances in Magnetic Current Sensors with External Conductor

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Abstract

Small-sized SMD current sensor ICs offer a cost effective solution for several current sensing applications utilizing standard printed circuit board (PCB) technology. The key to measurement-range scalability is to use a current rail external to the sensor package instead of being an integral part of the package. However, state of the art PCB mounting processes show assembly tolerances, which may cause several percent of error in the sensitivity. Such level of errors is usually not tolerable by the electronics manufacturers, so the best they can do is a final End-Of-Line (EOL) calibration after mounting, where specific current levels need to be set accurately and forced through the device. This paper presents the idea of compensation of assembly tolerances as a potential counteraction already on IC-level. The method itself is based on additional sensing-elements integrated onto the die beside the main ones: their signals are combined with the main sensor signals to get the compensated current signal. Adopting this principle, the costly and time-consuming EOL calibration can be abandoned resulting in increased IC-product value.

Keywords

assembly tolerance, current rail, current sensor, electromagnetic immunity, gain compensation, Hall device, insertion resistance, magnetic sensitivity

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1 Introduction

The measurement of electric current is a technical problem that emerges in various applications from battery management to electric machine control, or in safety critical subsystems as over current monitoring. Two main kinds of current sensing methods exist:

The direct method is based on Ohm`s law, and converts the current into a voltage value using a shunt resistor in the current path. In [1] a basic system on chip architecture with integrated shunt and ADC is introduced.

Indirect current sensing makes use of the magnetic field of the current. Hall-effect sensors and magnetoresistive sensors can be applied to produce a voltage signal proportional to the magnetic field of the current, and this way to the current itself (Ampere`s law, Biot-Savart law). If the magnetic field of the current is directly measured, we speak of open-loop current sensing, and if this field is zeroed by a compensation feedback loop, the current sensor is called closed-loop. While the technics mentioned up to now are all capable of measuring both AC- and DC-currents, current transformers like the classical Rogowski-coil, work only with AC-currents, being sensitive to the change of the field over time (Faraday`s law). Only the indirect current measurement methods offer the advantage of galvanic isolation between the application circuit and the sensing circuit, which is very important in case of high voltage applications. To increase the magnetic field amplitude crucial for the indirect current sensing methods usually magnetic concentrators or cores are applied. One can find a good summary of the afore-mentioned methods in [2].

Coreless Hall-based magnetic current sensor-ICs have become widespread in several application fields like power metering, electric power steering, motor control, industrial and consumer inverters. They require a primary current conductor, i.e. a current rail either as the part of their leadframe or the PCB and one or more Hall-effect sensing elements fabricated on the Si-chip together with a signal processing circuit. Having the Hall-probes on both sides of the current rail, makes it possible to eliminate the homogen part of the external background magnetic field by signal difference building. Advanced spinning and

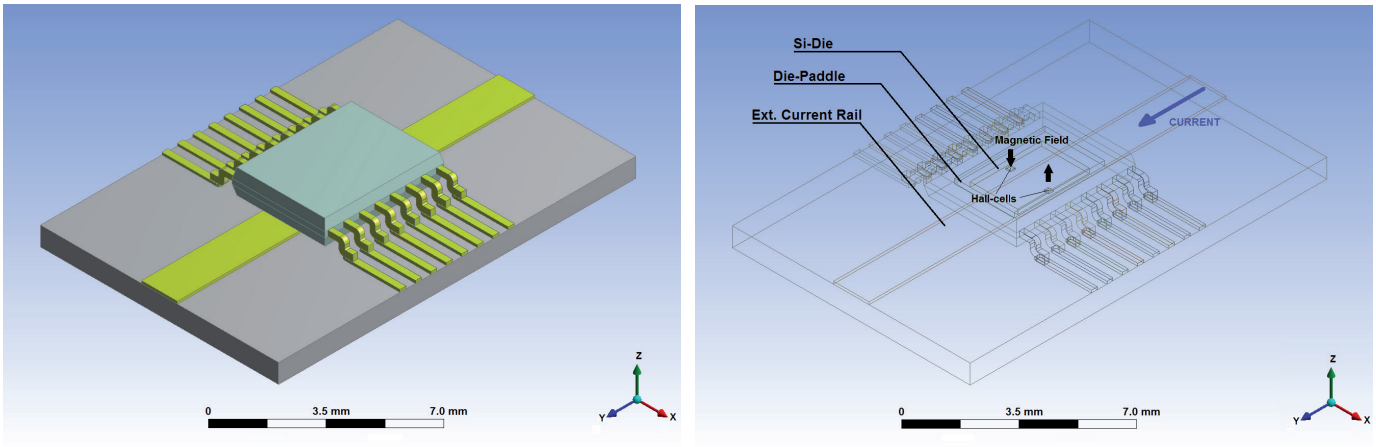

Fig. 1 a) Example arrangement of a differential current sensor IC with external current conductor on a PCB; b) Main parts and quantities in the model

chopping techniques are used to minimize measurement offset. Since the sensitivity of Hall-devices is strongly temperature dependent, on-chip temperature compensation is necessary. The chip is typically isolated from the current rail, the potential of which might reach several kV-s [3]. Unlike current sensors with field concentrators, they offer the advantages of reduced cost and size, which are critical factors in the automotive arena, and since lacking all kinds of soft-magnetic cores, they show virtually no hysteresis-effects. The effective measurement range of current sensor-ICs is primarily limited by the current rail:

$$\Delta T_j = R_{th} \cdot R_{CR} \cdot I_{eff}^2 \tag{1}$$

where $\Delta T_j\,[K]$ is the junction-temperature difference relative to the ambience caused by self-heating of the current rail, $R_{th}\,[K/W]$ is the thermal resistance between the hot spot and the ambience, $R_{CR}\,[\Omega]$ is the current rail resistance and $I_{eff}\,[A]$ is the effective value of the primary current flowing through the current rail, which we want to measure. On the other hand, to reach an acceptable signal to noise ratio beside a specific current range, the current rail is narrowed down in the proximity of the sensing element(s) to maximize the magnetic field. According to the Biot-Savart Law:

$$\boldsymbol{B}(\boldsymbol{r}) = \frac{\mu_0}{4\pi}\int_V \boldsymbol{J}(\boldsymbol{r}') \times \frac{\boldsymbol{r}-\boldsymbol{r}'}{|\boldsymbol{r}-\boldsymbol{r}'|^3}\,dV' \tag{2}$$

where $\boldsymbol{B}(\boldsymbol{r})[T]$ is the magnetic induction vector in the point defined by the $\boldsymbol{r}[m]$ position vector, $\mu_0[Tm/A]$ is the vacuum permeability and $\boldsymbol{J}(\boldsymbol{r'})[A/m^2]$ is the current density vector at position $\boldsymbol{r'}$. Consequently the sensor designer faces a typical trade-off scenario, normally leading to lower resistance values for higher current ranges. In case of internal current rail solutions, the package already determines the available current handling capability. Exclusively the concept of an external current rail enables the scalability in measurement range. In practice it means, that the sensor-IC is soldered onto the PCB, while the external current rail is realized as Cu-traces of the PCB on the top Cu-layer, and depending on the range, additionally in the internal Cu-layers, underneath the sensor-package. Standard PCB technology is applicable up to 50 A_{rms}, while above 100 A_{rms} power PCBs or other kinds of high current boards with copper thicknesses up to several mm-s come into play.

The remainder of the paper is structured as follows: Section 2 describes the technical problem to be solved, i.e. the sensitivity error sources. In Section 3 the general idea of the compensation of vertical tolerances using vertical Hall-cells is shown assuming the example geometry in Section 2. In Section 4 we present the effectiveness of such compensation by carrying out a numerical optimum search, considering both lateral- and vertical tolerances. Section 5 proposes two different implementation alternatives fitting to different application scenarios.

2 Effect of assembly tolerances on sensitivity

Let`s consider the following current sensing arrangement of Figs. 1a, 1b: The external current conductor is a long, straight, w=1.7 mm wide, h=0.1 mm thick current trace of copper on a PCB. Two Hall-plates are located on the surface of a silicon die in a lateral distance of d_{Hall}=2.3 mm from each other. The die is attached to the bottom of a die-paddle with orientation face-down in a TDSO-16 plastic encapsulated package. This package is soldered onto the PCB so, that the Hall-plates are positioned symmetrically left and right above the edges of the current trace. The nominal vertical distance between the Halls and the current rail`s middle layer is z_{Hall}=0.25 mm (Table 1). Since the vertical differential magnetic field is measured, the homogeneous portion of the external magnetic disturbances is suppressed [3]. At low frequency for the vertical component of the magnetic field in the test point (x,y,z), assuming x_{trace}=z_{trace}=0 conductor position, and neglecting the effect of the trace thickness, we get:

$$B_z(x,z) = \int dB_z(x',z) = \frac{\mu_0 I}{2\pi w}\cdot\int_{x-\frac{w}{2}}^{x+\frac{w}{2}} \frac{x'}{x'^2+z^2}\,dx' = \frac{\mu_0 I}{4\pi w}\cdot\ln\left(\frac{\left(x+\frac{w}{2}\right)^2+z^2}{\left(x-\frac{w}{2}\right)^2+z^2}\right) \tag{3}$$

where $B_z(x,z)[mT]$ is the vertical magnetic field component at coordinates $x[mm]$ and $z[mm]$, $I[A]$ is the primary current, $w[mm]$ is the width of the current rail.

Table 1 Model Parameters

Description of parameter	Symbol	Value
Width of current trace on the PCB	w	1.7 mm
Thickness of current trace on the PCB	h	0.1 mm
Spacing of Hall-plates on sensor chip	d_{Hall}	2.3 mm
Vertical distance between Hall-plates and the middle layer of the current trace	z_{Hall}	0.25 mm

The differential Hall-signal assuming nominal sensor-IC position is given by:

$$U_{z,diff}^{nom} = \frac{S_{Hall}^{lat}}{2} \cdot \left(B_z\left(\frac{d_{Hall}}{2}, z_{Hall} \right) - B_z\left(-\frac{d_{Hall}}{2}, z_{Hall} \right) \right) = S_{Hall}^{lat} \cdot B_{z,diff}^{nom} \tag{4}$$

where $U_{z,diff}^{nom}\,[mV]$ is the nominal differential lateral-Hall voltage signal, $S_{Hall}^{lat}\left[\frac{mV}{mT}\right]$ denotes the sensitivity of a lateral Hall device related to the magnetic field including preamplification, and $B_{z,diff}^{nom}\,[mT]$ is the nominal differential vertical magnetic field. In reality the positioning suffers from several tolerance issues. Package manufacturing tolerances, like chip attach positioning errors, have no effect on measurement sensitivity, because each sensor receives a basic calibration at the sensor IC manufacturer EOL. Note also that Hall plates exhibit an amount of mismatch due to standard deviation in thickness, temperature gradient across the chip and mechanical stress gradient across the chip. It is possible to compensate for this mismatch by a wire-on-chip (WOC) at the electronics manufacturer.

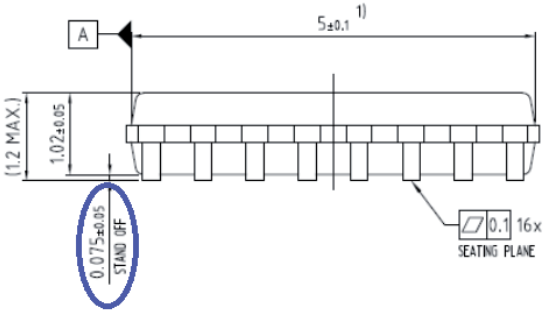

Fig. 2 Side-view drawing of a package with gull-wing interconnects showing ±50 µm co-planarity error due to varying lead stand off

Main tolerance aspects originate from pick & place accuracy of standard SMD mounting equipment, co-planarity of package interconnects to board (e.g. gull-wing leads), solder amount during package mounting onto PCB causing stand-off tolerances, and depending on PCB design, potential Cu-layer versus solder-resist offsets. Additionally these tolerances can be caused by package movement during soldering process. In total the mounting tolerances sum up to state of the art ±50 µm position accuracy in all three directions and ±1.0° rotational tolerance around all three axes as typical scenario. Let`s consider now each of these six potential positioning errors one-by-one.

Due to the symmetry in the nominal position $\frac{\partial U_{z,diff}}{\partial x} = 0$ and $\forall n \in Z^+ : \frac{\partial^n U_{z,diff}}{\partial y^n} = 0$ as well, or simply put, a Δy shift has no influence on the signal. There might be a significant contribution from position-uncertainties along the *x*-axis, i.e. laterally perpendicular to the current rail, because $\frac{\partial^2 U_{z,diff}}{\partial^2 x} \neq 0$, this must be analyzed later numerically. On the other hand, the $\frac{\partial U_{z,diff}}{\partial z}$ gradient is clearly and strongly negative. This effect is relatively easy to understand intuitively: by elevating the Hall-elements away from the trace, with the height they sense smaller fields, which additionally point more to the *x*-direction, so the *z*-component shrinks quickly.

Next we take the α, β and γ rotational tolerances around the x, y and z axes respectively.

A worst case rotation of α=±1° around the x-axis doesn`t change the position of the lateral Hall-elements, only their orientation, and since $B_y = 0$, such a rotation decreases the sensed magnetic field component normal to the chip surface with a factor of $\cos\alpha = 0.99985$, i.e. with a negligible 0.015%.

A γ rotation around the z-axis is equivalent to a suitable Δd_γ change of the Hall-spacing. A typical worst case rotational tolerance of $\gamma = \pm 1.0°$ results in $\Delta d_\gamma = d_{Hall} \cdot (\cos\gamma - 1) = -0.35\,\mu m$, which is also negligible.

A β rotation decreases the Hall-spacing in the same way as γ, and the sensed portion of B_z similarly to α. Additionally due to a β rotational tolerance, the B_x lateral fields are also seen by the single lateral Hall-cells, but their effect gets cancelled by the differential measurement. Finally the vertical movements of the two Hall-plates caused by β are opposite, so there is no change in the differential signal in the first order to that end either, as long as perfectly matched Hall-cells are considered. Consequently we can focus on the effect of two translational tolerances in the following, namely that of Δx and Δz:

$$U_{z,diff}(\Delta x, \Delta z) = \frac{S_{Hall}^{lat} \cdot \left(B_z\left(\Delta x + \frac{d_{Hall}}{2}, z_0 + \Delta z \right) - B_z\left(\Delta x - \frac{d_{Hall}}{2}, z_0 + \Delta z \right) \right)}{2}$$
$$U_{z,diff}(\Delta x, \Delta z) = S_{Hall}^{lat} \cdot B_{z,diff}(\Delta x, \Delta z) \tag{5}$$

where $U_{z,diff}[mV]$ is the differential lateral-Hall voltage signal, and $B_{z,diff}[mT]$ is the differential vertical magnetic field.

Numerically evaluating (5) based on (3) we get *±4.78% sensitivity change for ±50 µm vertical and lateral tolerance* relative to nominal position, or $2.81\%_{RMS}$ assuming uniform probability distribution of the tolerances. (Fig. 5) The dominant portion of the sensitivity change is associated with the vertical tolerance as shown by the results, while the second order effect of lateral movements looks negligible for the first glance, but later they will prove to be significant.

Such levels of sensitivity errors are unacceptable in most current sensing applications, let alone other sensitivity error contributors like temperature, stress and lifetime drifts. Since the standard deviation in sensitivity is caused by the PCB-mounting`s process variations, as a fundamental consequence,

the compensation must be based on measurements after the assembly. State of the art solution to this problem is EOL customer-calibration, as highlighted by official IC-manufacturer recommendations in [4] and [5]. The calibration procedure means increased production time and costs to the customer.

3 Compensation principle of vertical position tolerances

As discussed by [6], the magnetic sensitivity of such devices shows a dependence on the direction of the sensitive plane relative to the crystal orientation and field amplitude. However, this anisotropy is only significant over 100 mT, well beyond the typical 20-30 mT full scale range of coreless Hall-based current sensors.

In [7] the authors describe vertical Hall devices and state of the art techniques to minimize offset and 1/f noise (spinning and chopping), optimize SNR by current biasing (stacking) and analog precompensation of the sensitivity`s stress dependence due to the Piezo-Hall effect.

In [8], the performance of vertical Halls in series is analyzed. With such connections higher SNR and a lower residual offset and current consumption is achievable.

In [9] the authors discuss symmetrizing circuit-techniques to reduce the relatively large raw offset, and at the same time the residual offset (after-spinning) of vertical Halls.

Two of the vertical Halls shall be located directly next to the original two differential-bridge Hall-cells on the left and right side of the current rail, the third one in the center.

The basis of the compensation scheme for vertical position tolerances is to measure the lateral B_x magnetic field components in specific points, in addition to the vertical B_z components, to gain information regarding the actual height. To that end we fabricate additionally three matched vertical Hall-plates on the same die, which are sensitive to magnetic fields in the lateral x-direction.

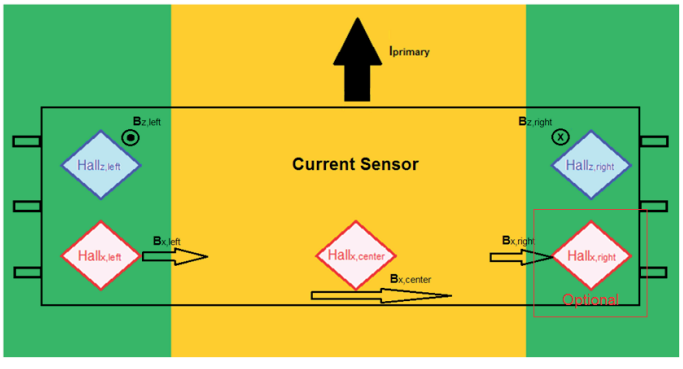

Fig. 3 Additional vertical Halls to compensate for Δz tolerances

Based on (3) and (4) one can show that $U_{z,diff}$ is background field compensated and with a good approximation a linear function of Δz:

$$U_{z,diff}(0,\Delta z) = S^{lat}_{Hall} \cdot B_{z,diff}(0,\Delta z) \approx S^{lat}_{Hall} \cdot (1 - c_1 \cdot \Delta z) \cdot k_{CR,z} \cdot I_P \quad (6)$$

where $I_P[A]$ is the actual value of the primary current, $k_{CR,z}$ [μT/A] and c_1[1/m] are geometry constants of the whole arrangement representing the linear decline of $B_{z,diff}$ over Δz. Further assembly tolerances like α, β, γ, Δx and Hall-plate magnetic sensitivity mismatch do not affect c_1 up to the first order.

For $\Delta z = 50$ μm one gets $c_1 \cdot \Delta z = 4.78\%$ and $k_{CR,z} = 193.0\ \mu T/A$ for the system according to Table 1. In the following we look for a method how to reduce this error of about 5% down to a few tenths of a percent.

The lateral magnetic field component for low frequency currents is given by:

$$B_x(x,z) = \int dB_x(x',z) = \frac{\mu_0 I}{2\pi w} \cdot \int_{x-\frac{w}{2}}^{x+\frac{w}{2}} \frac{z}{x'^2 + z^2} dx'$$
$$B_x(x,z) = \frac{\mu_0 I}{2\pi w} \cdot \left(\operatorname{arctg}\left(\frac{x + \frac{w}{2}}{z} \right) - \operatorname{arctg}\left(\frac{x - \frac{w}{2}}{z} \right) \right) \quad (7)$$

where $B_x(x, z)\ [mT]$ is the lateral magnetic field component at coordinates $x[mm]$ and $z[mm]$. The signal representing the difference of the lateral magnetic field in the center and at the sides is:

$$U_{x,diff}(0,\Delta z) = S^{ver}_{Hall} \cdot \left(B_{x,center} - \frac{B_{x,left} + B_{x,right}}{2} \right)$$
$$U_{x,diff}(0,\Delta z) \approx S^{ver}_{Hall} \cdot (1 - c_2 \cdot \Delta z) \cdot k_{CR,x} \cdot I_P \quad (8)$$

where $U_{x,diff}[mV]$ is the differential vertical-Hall voltage signal, $S^{ver}_{Hall}\left[\frac{mV}{mT}\right]$ is the sensitivity of a vertical-Hall device related to the magnetic field including preamplification, $B_{x,center}\ [mT]$, $B_{x,left}\ [mT]$, $B_{x,right}\ [mT]$ are the lateral magnetic induction vectors above the center of, left, and right to the current rail respectively (see Fig. 3), $k_{CR,x}\ [\mu T/A]$ and c_2[1/m] are geometry constants of the whole arrangement representing the linear decline of $B_{x,diff}$ over Δz. c_2 is independent of other assembly tolerances and magnetic sensitivity mismatches with a good approximation.

Considering $\Delta z = 50\ \mu m$, one gets $c_2 \cdot \Delta z = 9.10\%$ and $k_{CR,x} = 235.6\ \mu T/A$ for a system described in Table 1. So $U_{x,diff}$ is roughly double as sensitive to variations in vertical spacing than $U_{z,diff}$.

Consequently it shall be possible to construct a practically Δz-invariant linear combination of the two background-independent signals, which is obviously still a proportional representative of the primary current:

$$U_{comp}(0,\Delta z) = m \cdot U_{z,diff}(0,\Delta z) - U_{x,diff}(0,\Delta z) \quad (9)$$

Based on (6) and (8) we can write:

$$\frac{U_{comp}(0,\Delta z)}{I_P} = \left(m \cdot S^{lat}_{Hall} \cdot k_{CR,z} - S^{ver}_{Hall} \cdot k_{CR,x} \right)$$
$$+ \Delta z \cdot \left(c_2 \cdot S^{ver}_{Hall} \cdot k_{CR,x} - m \cdot c_1 \cdot S^{lat}_{Hall} \cdot k_{CR,z} \right) \quad (10)$$

We can assume $S_{Hall}^{ver} = S_{Hall}^{lat}$ for simplicity, since both channels include an amplification stage. (On the other hand the exact ratio of the two sensitivity values doesn`t influence the compensation method in essence, only a scaling factor needs to be applied.) The required m multiplication factor to eliminate the Δz-dependence neglecting second order effects will be:

$$m = \frac{c_2 \cdot S_{Hall}^{ver} \cdot k_{CR,x}}{c_1 \cdot S_{Hall}^{lat} \cdot k_{CR,z}} = \frac{c_2 \cdot k_{CR,x}}{c_1 \cdot k_{CR,z}} = 2.31 \qquad (11)$$

$$U_{comp}(0,\Delta z) \approx S_{Hall}^{ver} \cdot k_{CR,x} \cdot \left(\frac{c_2}{c_1} - 1\right) \cdot I_P = S_{Hall}^{ver} \cdot k_{CR,comp} \cdot I_P \qquad (12)$$

where $U_{comp}[mV]$ is the compensated differential Hall voltage signal, $k_{CR,comp}[\mu T/A]$ is the compensated transfer rate. It is important to note, that with our example arrangement described in Table 1. the signal will correspond to $k_{CR,comp} = k_{CR,x} \cdot \left(\frac{c_2}{c_1} - 1\right) = 210.3\,\mu T/A$, which means we do not lose, but gain sensitivity compared to the vertical differential measurement principle, as $k_{CR,comp} > k_{CR,z}$ (See Fig. 4)

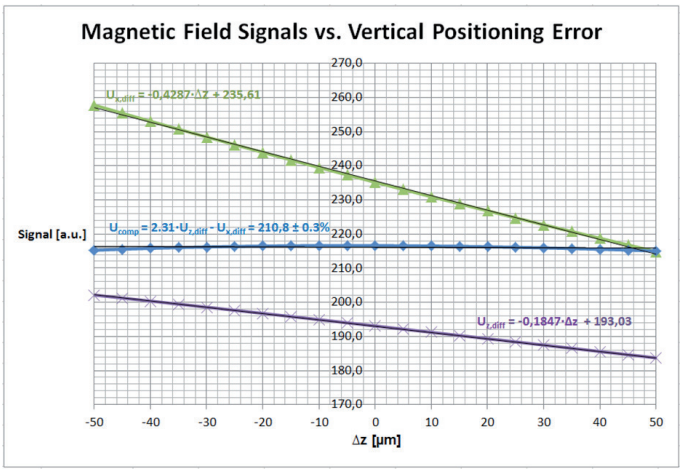

Fig. 4 Compensation of the vertical positioning error by linear combination of the x- and z-differential signals

4 Numerical evaluation of the compensation principle

In Figure 5 we see the initial sensitivity error in the function of the Δz and Δx tolerances, discussed already in Section 2.

Next we check the accuracy of the compensation precisely. One can evaluate the above described method using the following formula:

$$U_{comp}(\Delta x,\Delta z) = m \cdot U_{z,diff}(\Delta x,\Delta z) - U_{x,diff}(\Delta x,\Delta z) \qquad (13)$$

In the exact calculation (3), (5), (7) and (8) are applied. The optimal $m = 2.31$ compensation coefficient was found by numerical optimum search in Matlab, targeting the smallest possible RMS-error of sensitivity for our model case. This is the same result as in (11), although this time second order effects both over the x- and z-axis were also considered. The sensitivity error after compensation decreases to an acceptable level of $0.30\%_{RMS}$ spreading between −0.78% and 0.72% over the ±50 µm tolerance ranges which is shown by Fig. 6. Although the Δx-dependence of the initial error is seemingly negligible (see Fig. 5), in the residual error it plays an equal role compared to the Δz-dependence.

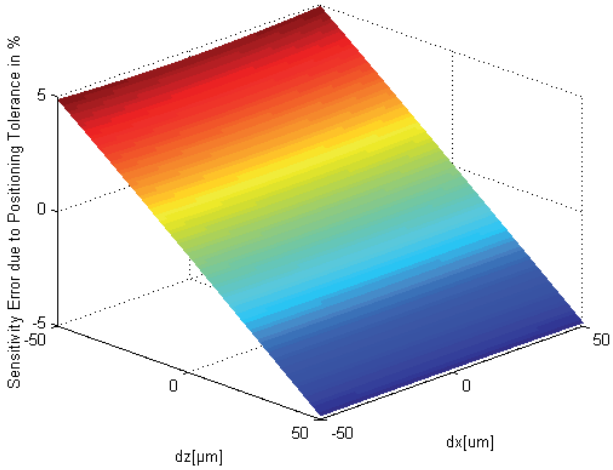

Fig. 5 Initial sensitivity error for $\Delta x = \Delta z = \pm 50$ µm

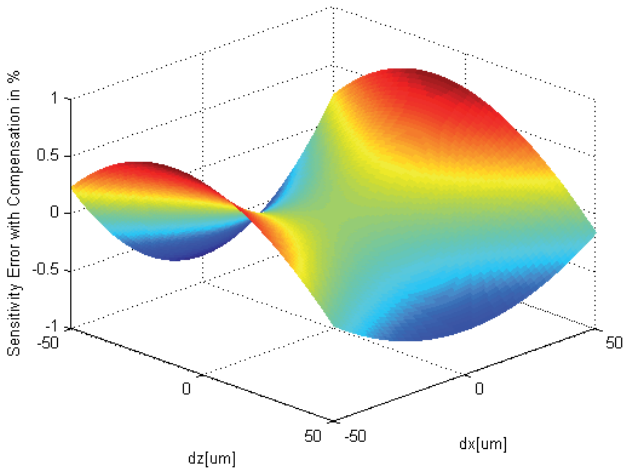

Fig. 6 Residual sensitivity error for $\Delta x = \Delta z = \pm 50$ µm

This error comes from the fact that the compensation is purely linear and the nonlinearity of the signals versus vertical distance lead to additional errors, just like the signal dependence on lateral displacements. Anyhow at the end we can speak of a roughly 6-fold error reduction.

Moreover it is important to note, that unlike the initial error the residual sensitivity error doesn`t scale linearly with the tolerance range enabled by the mounting process, but decreases in a quadratic way in accordance with the saddle-surface characteristic when the positioning precision is improved. In case of an enhanced ±25 µm positioning precision we get an initial ±2.42% error (Fig. 7), while after compensation the residual error will be as low as ±0.18% (Fig. 8). This corresponds to an improvement of factor 13.

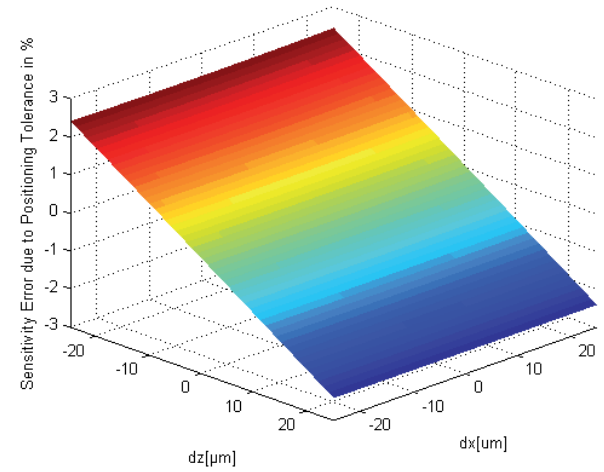

Fig. 7 Initial sensitivity error for Δx=Δz=±25 µm

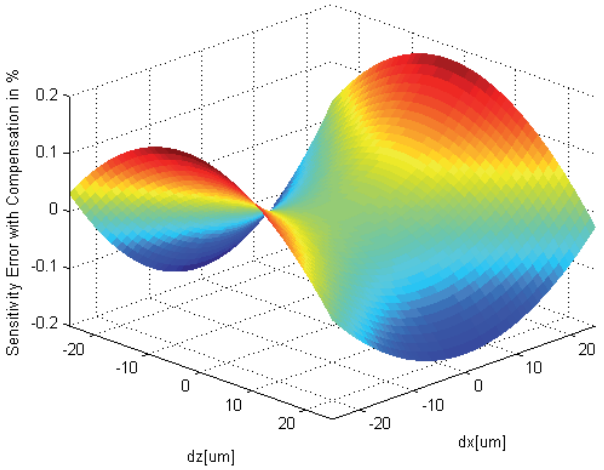

Fig. 8 Residual sensitivity error for Δx=Δz=±25 µm

5 Implementation alternatives

There are two possible approaches to exploit the above described principle. For both implementation alternatives the auxiliary vertical Hall devices need to be integrated onto the silicon, as depicted by Fig. 3. The difference signals defined by (6) and (8) are best to synthesize in the analog domain, using amplifiers preceding the A to D conversion. The linear combination of the vertical- and lateral difference signals in (9) and (13) shall be realized by a DSP, while the compensation-factor is a tunable EEPROM-parameter and fits the specific application layout. It is important to note, that the sensitivity mismatches between the Hall-elements, and their offsets must be calibrated for at 0 hour by the IC-manufacturer.

In the *first variant* the compensation happens continuously, *"in situ"* during operation over the lifetime of the IC. In this case, should any change in the vertical position happen after assembly, due to swelling from humidity or mechanical deformation, their effect on the sensitivity gets immediately compensated. The sensitivity- and offset drifts over lifetime especially that of the vertical Halls might limit the accuracy of the compensation. A typical +1% drift in the sensitivity to the B_x fields for instance, turns into −1.1% drift in the combined signal. Another disadvantage of this method is the additional current consumption of the vertical Halls.

Consequently a *second approach* might be also desirable for several practical cases. Here U_{comp} is measured at "*0 hour*" only along with $U_{z,diff}$ right after the assembly process at the PCB-manufacturer, by applying an arbitrary current level. At this time point the lifetime drifts of the Hall-cells shall be negligible, so U_{comp} really reflects the expected sensitivity times the applied current. After storing the $r = U_{comp}/U_{z,diff} = m - U_{x,diff}/U_{z,diff}$ ratio in an EEPROM, it can be used as a simple multiplicative correction factor to $U_{z,diff}$ by the DSP later on, while the vertical Halls can be switched off for the remaining lifetime of the product. With this technique we eliminate the undesirable effects of the vertical Halls` lifetime drifts on the compensated signal, as well as their current consumption. Note that bears the required position correction information regarding the vertical signal right after the soldering, and no further displacements will be tracked afterwards.

6 Conclusion and outlook

In case of internal current rail current sensors the current handling capability is fundamentally limited by the package itself. On the other hand external current rail current sensing offers the flexibility with respect to the current measurement range of the sensor. For a typical differential Hall-based current sensor IC application with external current rail, an approximately 5% assembly tolerance related sensitivity error can be decreased below 1% based on the above described compensation principle. The compensation method has a vertical position invariant combination of vertical- and lateral magnetic field signals in its focus. The solution doesn`t come free and costs of course additional chip area, complexity and, on top for the first variant, more current consumption. In case of a practical implementation the errors inherent to the compensation circuit, as offset- and sensitivity drifts over lifetime, must be carefully analyzed, just like the possible chip displacements over lifetime. In the present article two ways of realization were proposed to effectively tackle these challenges.

Nomenclature

$\boldsymbol{r}$	position vector [mm]
x,y,z	Descartes-coordinates [mm]
ΔT_j	junction-temperature difference relative to ambience [K]
R_{th}	thermal resistance between hot spot and ambience [K/W]
R_{CR}	current rail resistance [Ω]
I_{eff}	effective primary current [A]
I_P, I	actual primary current [A]
$\boldsymbol{J}$	current density vector [A/m^2]
μ_0	vacuum magnetic permeability [Tm/A]
$\boldsymbol{B}$	magnetic induction vector [T]

B_x	x-component of the magnetic induction vector $[mT]$
$B_{x,center}$	x-component of $\boldsymbol{B}$ above the center of the current rail $[mT]$
$B_{x,left}$	x-component of $\boldsymbol{B}$ on the left side of the current rail $[mT]$
$B_{x,right}$	x-component of $\boldsymbol{B}$ on the right side of the current rail $[mT]$
B_y	y-component of the magnetic induction vector $[mT]$
B_z	z-component of the magnetic induction vector $[mT]$
$B_{x,diff}^{nom}$	nominal differential lateral magnetic field $[mT]$
$B_{z,diff}^{nom}$	nominal differential vertical magnetic field $[mT]$
$B_{x,diff}$	differential lateral magnetic field $[mT]$
$B_{z,diff}$	differential vertical magnetic field $[mT]$
S_{Hall}^{lat}	sensitivity of a lateral Hall device related to the magnetic field including preamplification $[mV/mT]$
S_{Hall}^{ver}	sensitivity of a vertical Hall device related to the magnetic field including preamplification $[mV/mT]$
$U_{z,diff}^{nom}$	nominal differential lateral-Hall voltage signal $[mV]$
$U_{x,diff}$	differential vertical-Hall voltage signal $[mV]$
$U_{z,diff}$	differential lateral-Hall voltage signal $[mV]$
U_{diff}^{comp}	compensated differential Hall voltage signal $[mV]$
$k_{CR,x}$	lateral magnetic field transfer rate $[\mu T/A]$
$k_{CR,z}$	vertical magnetic field transfer rate $[\mu T/A]$
$k_{CR,comp}$	compensated magnetic field transfer rate $[\mu T/A]$
c_1, c_2	geometry factors without unit

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